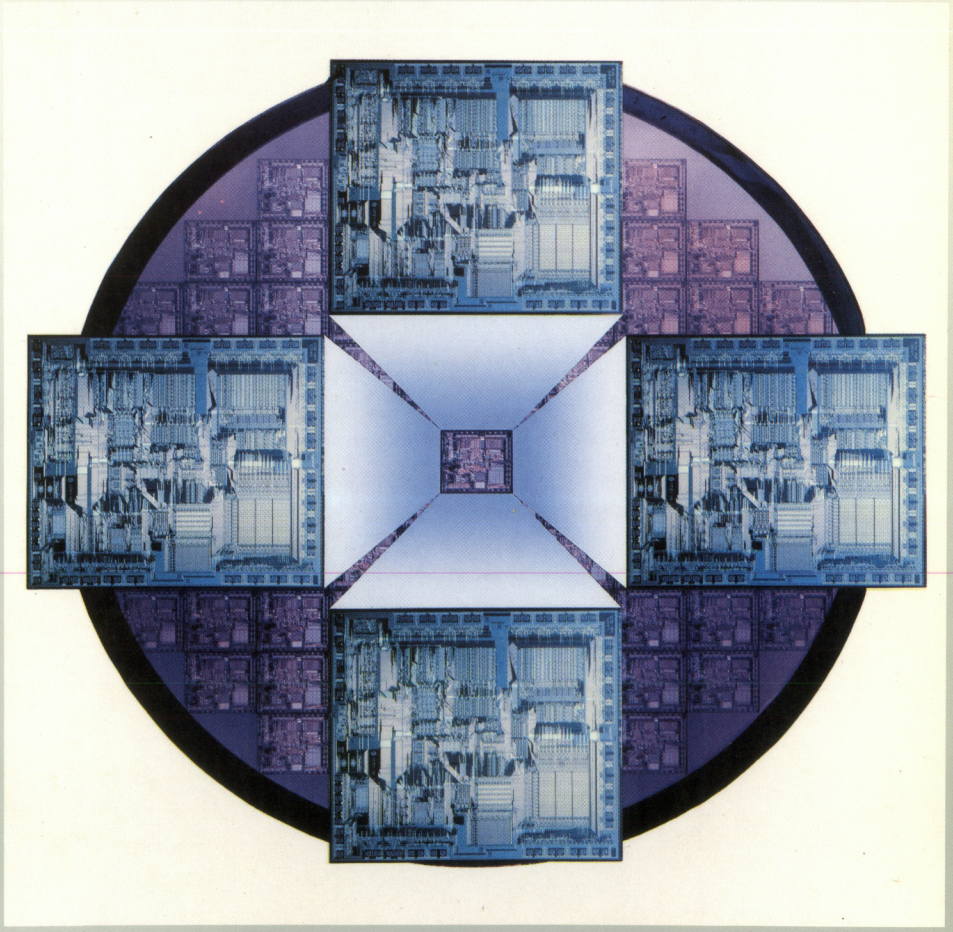
SIEMENS

Microcomputer Components

Microprocessors, System and Support Components

Data Catalog 1988



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Siemens Aktiengesellschaft

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SAB 80C52/80C32	Microcontroller, 256 × 8-bit RAM, 8K × 8-bit ROM, 32 I/O lines, SAB 80C32 without ROM, CMOS technology
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SAB 80512K	Microcontroller, 128 × 8-bit RAM, 48 I/O lines, A/D converter, ROM-less version
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SAB 8052A/8032A	Microcontroller, −40 to +85°C and −40 to +110°C
SAB 80512/80532	Microcontroller, −40 to +85°C
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Type Survey for Data Catalog Peripheral Components and Memories

Type Survey for Data Catalog
Peripheral Components and Memories

Peripheral Components

SAB 2793B/2797B	Floppy-disk controller
SAB 7201A	Multi-protocol serial communications controller
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SAB 8276	Small system CRT controller
SAB 82510	Token bus controller
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SAB 41256-10/-12/-15	RAM, dyn., 262,144 × 1-bit
SAB 511000-85/-10/-12	RAM, dyn., CMOS, 1 048,576 × 1-bit
SAB 514256-85/-10/-12	RAM, dyn., CMOS, 262,144 × 4-bit
SAB 81C80	RAM, stat., CMOS, 504 byte

General Information

General Information

Type designation code for ICs

IC type designations are based on the European Pro Electron sytem. The code system is explained in the Pro Electron brochure D 15, edition 1985, available at:

Pro Electron, Avenue Louise, 430 (B. 12)
B-1060 Brussels, Belgium

Mounting instructions

Plastic package

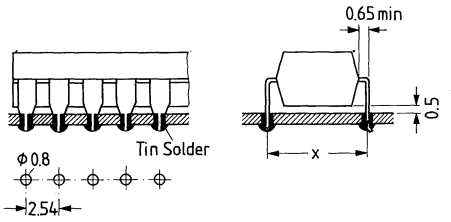
The 90° pins fit into holes with a diameter of 0.7 to 0.9 mm, spaced 2.54 mm apart. See spacing x in figure 1.

The bottom of the package will not touch the PC board after insertion because the pins have shoulders just below the package **(see figure 1)**.

After insertion of the package into the PC board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. Plastic packages are soldered on that side of the PCB facing away from the package.

The maximum permissible soldering temperature is 350 °C (max. 3 s) for hand soldering and 260°C (max. 10 s) for dip soldering and wave soldering.

Figure 1



Dimensions in mm

Plastic packages (SO and PLCC) for surface mounting (SMD)

Iron soldering:	soldering temperature 350 °C for max. 3 s; minimum distance between package and soldering point 1.5 mm package temperature max. 150 °C; no mechanical stress on the pins
Vapor phase soldering:	soldering temperature 215 °C, max. soldering time 40 s
Wave soldering: (pins and package are dipped into the tin bath)	soldering temperature 260 °C, max. soldering time 8 s

Storage, pretreatment before processing

The components are to be stored in a dry environment. When solder methods causing solder heat shock stresses are used (reflow soldering where the component is dipped into the solder bath, vapor-phase soldering) it is recommendable to subject IC's in plastic packages to a 24-hour drying phase at 125°C.

Other points to note

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.
When the pins are being prepared and inserted in a PCB, circuits should be protected against static charging. Under no circumstances should the components be removed or inserted while the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensitivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through the switching of inductances on magnetic chutes, etc.

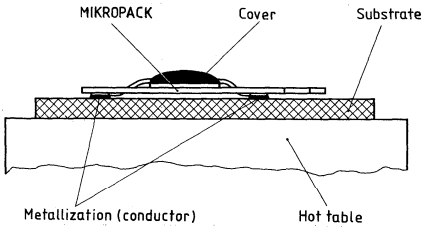
MIKROPACK (SMD)

MIKROPACK components are delivered on film reels.

Mounting suggestions

a) We recommend vapor phase soldering: soldering temperature 215°C, soldering time max. 30 s
b) For prototypes and small quantities (up to approximately 50.0 items/y), the hot table soldering method can also be used (**see figure 2**).

Figure 2



Required equipment and accessories

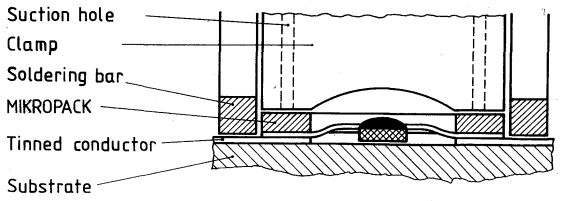
- cutting device
- hot table, temperature regulated (e.g. Weld-Equip, Unitek)
- stereo microscope (e.g. Wild, Zeiss, magnification 6 · · · 40 times)
- substrate material: epoxy resin; hard paper; ceramic (thick thin film)

Soldering data

- soldering temperature: 210 °C max.
- solder coating on substrate: Pb/Sn (e.g. 60/40) wave-tinned or electro-deposited
- soldering time: approx. 10 s
- flux: e.g. colophony, dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

c) For large quantities (e.g. more than 50.0 items/y) bar soldering is also suitable.

Figure 3



Required equipment

- soldering equipment (e.g. Weld-Equip, Farco, Jade)
- substrate material: epoxy resin; hard paper; flexible materials, e.g. polyamide

Soldering data

- soldering temperature: 210 °C max.
- solder coating on the substrate: Pb/Sn (e.g. 60/40), wave-tinned or electro-deposited
- soldering time: approx. 2 s
- flux: e.g. colophony dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

Processing guidelines for ICs

Integrated circuits (ICs) are **e**lectro**s**tatic-**s**ensitive (**ESS**) devices. The requirement for greater packing density has led to increasingly small structures on semiconductor chips with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is hardly possible any more for them to be destroyed by purely static electricity. On the other hand, there is acute danger from **e**lectro**s**tatic **d**ischarges (**ESD**).

Of the multiple of possible sources of discharge, charged devices should be mentioned in addition to charged persons. With low-resistive discharges it is possible for peak power amounting to kilowatts to be produced.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
   Means which are effective here are an increase in relative humidity to $\geq$ 60% and the replacement of highly charging plastics by antistatic materials.
b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to $10^8\ \Omega$).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification

The packing of ESS devices is provided with the following label by the manufacturer:

Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

Handling of devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to $10^9\ \Omega$/cm.
3. With humidity of >50% a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 to 100 kΩ.

4. If conductive floors, $R = 5 \times 10^4$ to $10^7\ \Omega$ are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to $10^7\ \Omega$).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to $10^8\ \Omega$.
6. When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g. machine parts.

   Example 1) Conductive (black) tubes.
   The devices may be destroyed in the tube by charged persons or come out of the tube charged if this is emptied by a charged person.
   Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

   Example 2) Anti-static (transparent) tubes.
   The devices cannot be destroyed by charged persons in the tube (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be endangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

   In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material ($\approx 10^6$ to $10^8\ \Omega$/cm) between the tube and the machine.

   The use of metal tubes – especially of anodized aluminum – is not advisable because of the danger of low-resistance device discharge.

Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 60 °C.

Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of high-charging plastic or very low-resistance materials are likewise unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6\ \Omega$). Sliding contacts and grounding chains will not reliably eliminate charges.

Incoming inspection

In incoming inspection the above guidelines should be observed. Otherwise any right for refund or replacement if devices fail inspection may be lost.

Material and mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control cannot be used. Siemens EMI-suppression capacitors of the type B 81711-B31...-B36 have proven very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

Electrical tests

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting rings.
2. Test sockets must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works' specifications state otherwise. Ensure that the test devices do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. Signal voltages may only be applied to the inputs of ICs when or after the supply voltage is turned on. They must be disconnected before or when the supply voltage is turned off.
4. Observe any notes and instructions in the respective data books.

Packing of assembled PC boards or flatpack units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/cm < \rho < 10^{10}\ \Omega/cm$.

In most cases – especially with humidity of > 40% – this requirement is fulfilled using simple currugated board. Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

It must always be ensured that boards do not touch.

In special cases it may be necessary to provide potection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminum foil is recommended, although direct contact between the film and the PCB must be avoided. Cardboard boxes with an aluminum-foil lining, such as those used for shipping of our devices, are available from Laber of Munich.

Ultrasonic cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	$f > 40$ kHz
exposure	$t < 2$ min
alternating sound pressure	$p < 0.29$ bar
sound power	$N < 0.5$ W/cm^2/liter

Data classification

Maximum ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at $T_A = 25$ °C and for the given supply voltage.

Operating range

In the operating range the functions given in the circuit description will be fulfilled.

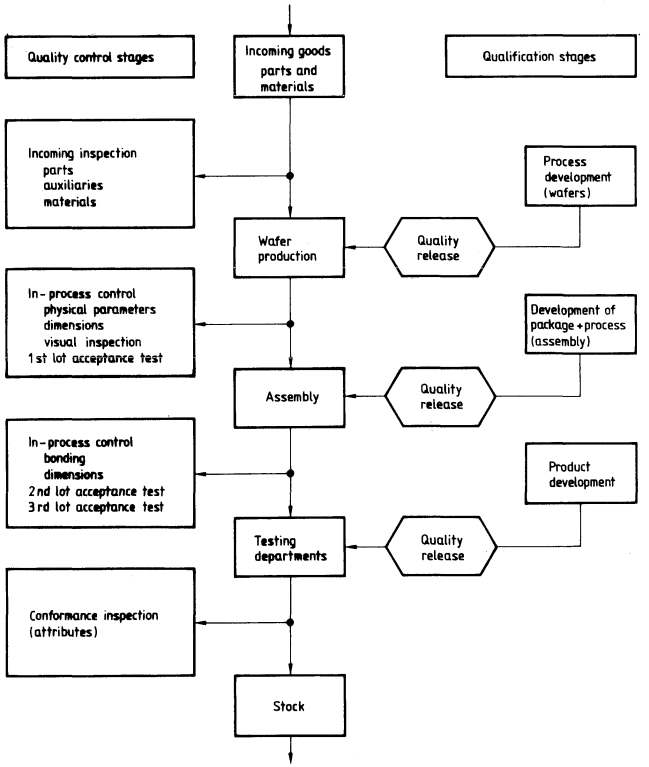
Quality assurance system

The high quality and reliability of integrated circuits from Siemens is the result of a carefully arranged production which is systematically checked and controlled at each production stage.

The procedures are subject to a quality assurance system; full details are given in the brochure "Siemens Quality Assurance System – Integrated Circuits" (SQS-IC).

Figure 4 shows the most important stages of the "SQS-IC". A quality assurance (QA) department which is independent of production and development, is responsible for the selected control measures, acceptance procedures, and information feedback loops. This department has state-of-the-art test and measuring equipment at its disposal, works according to approved methods of statistical quality control, and is provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.

Figure 4



The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These tests are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as of the identical MIL-STD-105 or IEC 410.

The table shows the results of such sampling inspections performed with hundreds of thousands of ICs in 1985. These results correspond to the average outgoing quality (AOQ), and are specified as defectives per million (DPM).

	Inoperatives AOQ (DPM)	Sum of electrical defectives AOQ (DPM)	Sum of mechanical defectives AOQ (DPM)
SSI/MSI $\leq$ 1000 gate functions	40	200	100
LSI/VLSI $\geq$ 1000 gate functions	120	400	200

Reliability

Measures taken during development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, specifying e.g. minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these design standards.

In-process control during production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged such that the individual process steps can be reproduced continuously.

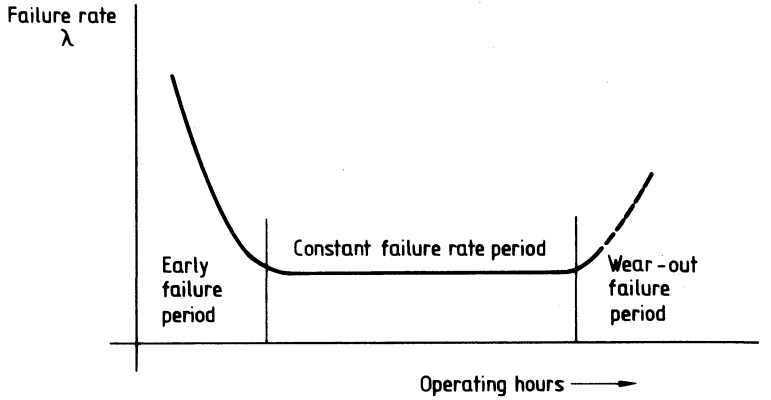
The decreasing failure rates reflect the never ending effort in this direction; they have been reduced considerably despite an immense rise in the IC's complexity.

So in 1985 the typical random failure rates estimated for accelerated life tests with almost 2 million ICs of all complexities are found to be around 80 fit.

Reliability monitoring

The general course of the IC's failure rate versus time is shown by a so-called "bathtub" curve (**figure 5**). The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Figure 5



Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius equation

$$B = \exp \quad \frac{E_A}{k} \left[\frac{1}{T_1} - \frac{1}{T_2}\right]$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for individual failure mechanisms.

For all Siemens ICs, the reliability data from life tests is converted to an operating temperature of $T_A = 40\,°C$, assuming an average activation energy of 0.4 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behavior. This method considers also failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line – this is described in the brochure "SQS-IC". Such tests are e.g. humidity test at 85 °C and 85% relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

Summary of Types (incl. ordering codes)

Summary of Types (incl. ordering codes)

Type	Ordering code	Package	Description	Page
8-Bit Microprocessors				
SAB 8085AH-P	Q67120-C122	P-DIP-40	Microprocessor, 3 MHz	41
SAB 8085AH-2-P	Q67120-C124	P-DIP-40	Microprocessor, 5 MHz	41
SAB 8088-N	Q67120-C301	PL-CC-44	Microprocessor, 5 MHz	69
SAB 8088-P	Q67120-C106	P-DIP-40	Microprocessor, 5 MHz	69
SAB 8088-1-P	Q67120-C249	P-DIP-40	Microprocessor, 10 MHz	69
SAB 8088-2-N	Q67120-C302	PL-CC-44	Microprocessor, 8 MHz	69
SAB 8088-2-P	Q67120-C213	P-DIP-40	Microprocessor, 8 MHz	69
SAB 80188-N	Q67120-C252	PL-CC-68	Microprocessor, 8 MHz	109
SAB 80188-R	Q67120-C168	C-CC-68	Microprocessor, 8 MHz	109
SAB 80188-1-N	Q67120-C299	PL-CC-68	Microprocessor, 10 MHz	109
SAB 80188-1-R	Q67120-C303	C-CC-68	Microprocessor, 10 MHz	109

SMD = Surface Mounted Device

Type	Ordering code	Package	Description	Page
16-Bit Microprocessors				
SAB 8086-C	Q67120-C45	C-DIP-40	Microprocessor, 5 MHz	165
S SAB 8086-P	Q67120-C116	P-DIP-40	Microprocessor, 5 MHz	165
SAB 8086-1-C	Q67120-C104	C-DIP-40	Microprocessor, 10 MHz	165
S SAB 8086-1-P	Q67120-C141	P-DIP-40	Microprocessor, 10 MHz	165
SAB 8086-2-C	Q67120-C60	C-DIP-40	Microprocessor, 8 MHz	165
S SAB 8086-2-P	Q67120-C142	P-DIP-40	Microprocessor, 8 MHz	165
S SAB 80186-N	Q67120-C250	PL-CC-68	Microprocessor, 8 MHz	205
S SAB 80186-R	Q67120-C150	C-CC-68	Microprocessor, 8 MHz	205
S SAB 80186-1-N	Q67120-C306	PL-CC-68	Microprocessors, 10 MHz	205
S SAB 80186-1-R	Q67120-C291	C-CC-68	Microprocessor, 10 MHz	205
SAB 80199	Q67100-A1961	P-DIP-40	Terminal processor, 20 MHz	259
S SAB 80286-A	Q67120-C204	C-PGA-68	Microprocessors, 8 MHz	261
S SAB 80286-N	Q67120-C330	PL-CC-68	Microprocessor, 8 MHz	261
S SAB 80286-R	Q67120-C151	C-CC-68	Microprocessor, 8 MHz	261
S SAB 80286-1-A	Q67120-C270	C-PGA-68	Microprocessor, 10 MHz	261
S SAB 80286-1-N	Q67120-C269	PL-CC-68	Microprocessor, 10 MHz	261
S SAB 80286-1-R	Q67120-C268	C-CC-68	Microprocessor, 10 MHz	261
SAB 80286-12-A	Q67120-C380	C-PGA-68	Microprocessor, 12.5 MHz	261
SAB 80286-12-N	Q67120-C381	PL-CC-68	Microprocessor, 12.5 MHz	261
SAB 80286-12-R	Q67120-C382	C-CC-68	Microprocessor, 12.5 MHz	261

S = Surface Mounted Device

Type	Ordering code	Package	Description	Page
System and Support Components				
SAB 8237A-P	Q67120-Y49	P-DIP-40	Programmable DMA controller, 3 MHz	331
S SAB 8237A-5-P	Q67120-Y72	P-DIP-40	Programmable DMA controller, 5 MHz	331
S SAB 82C37A-5-P	Q67120-P215	P-DIP-40	Programmable DMA controller, 5 MHz, CMOS	349
S SAB 82C37A-8-P	Q67120-P239	P-DIP-40	Programmable DMA controller, 8 MHz, CMOS	349
S SAB 82C37B-5-P	Q67120-P243	P-DIP-40	Programmable DMA controller, 5 MHz, CMOS	367
S SAB 82C37B-8-P	Q67120-P244	P-DIP-40	Programmable DMA controller, 8 MHz, CMOS	367
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S SAB 8287A-P	Q67020-Y154	P-DIP-20	Octal bus transceiver, inverting	435
S SAB 8288A-P	Q67020-Y155	P-DIP-20	Bus controller	443
S SAB 8289-P	Q67020-Y74	P-DIP-20	Bus arbiter, 8 MHz	455
S SAB 8289-1-P	Q67120-Y85	P-DIP-20	Bus arbiter, 10 MHz	455

S = Surface Mounted Device

Type	Ordering code	Package	Description	Page
System and Support Components (cont'd)				
SAB 82200-P	Q67020-Y171	P-DIP-22	Local bus arbiter	467
SAB 82C206-N	Q67120-P286	PL-CC-84	Integrated peripheral controller, CMOS	493
SAB 82220-N	Q67120-Y139	PL-CC-68	Bus interface controller	541
S SAB 82257-N	Q67120-P176	PL-CC-68	High-performance DMA controller, 8 MHz	635
S SAB 82257-6-N	Q67120-P179	PL-CC-68	High-performance DMA controller, 6 MHz	635
SAB 82258A-A	Q67120-P248	C-PGA-68	Advanced DMA controller, 8 MHz	691
SAB 82258A-N	Q67120-P246	PL-CC-68	Advanced DMA controller, 8 MHz	691
SAB 82258A-R	Q67120-P250	C-CC-68	Advanced DMA controller, 8 MHz	691
SAB 82258A-1-A	Q67120-P247	C-PGA-68	Advanced DMA controller, 10 MHz	691
SAB 82258A-1-N	Q67120-P245	PL-CC-68	Advanced DMA controller, 10 MHz	691
SAB 82258A-1-R	Q67120-P249	C-CC-68	Advanced DMA controller, 10 MHz	691
S SAB 82284-P	Q67020-Y162	P-DIP-18	Clock generator up to 16 MHz	753
S SAB 82284-1-P	Q67020-Y167	P-DIP-18	Clock generator up to 20 MHz	753
SAB 82C284-1-P	Q67120-P261	P-DIP-18	Clock generator and ready interface up to 20 MHz, CMOS	767
SAB 82C284-12-P	Q67120-P262	P-DIP-18	Clock generator and ready interface up to 25 MHz, CMOS	767
S SAB 82288-P	Q67120-Y75	P-DIP-20	Bus controller, up to 16 MHz	781
S SAB 82288-1-P	Q67120-Y69	P-DIP-20	Bus controller, up to 20 MHz	781
SAB 82288-6-P	Q67120-Y110	P-DIP-20	Bus controller, up to 12 MHz	781

SMD – Surface Mounted Device

Type	Ordering code	Package	Description	Page
System and Support Components (cont'd)				
SAB 82C288-P	Q67120-Y138	P-DIP-20	Bus controller up to 16 MHz, CMOS	813
SAB 82C288-1-P	Q67120-P258	P-DIP-20	Bus controller up to 20 MHz, CMOS	813
SAB 82C288-12-P	Q67120-P259	P-DIP-20	Bus controller up to 25 MHz, CMOS	813
S SAB 82289-P	Q67120-Y77	P-DIP-20	Bus arbiter, 16 MHz	845
SAB 82289-6-P	Q67120-Y111	P-DIP-20	Bus arbiter, 12 MHz	845

SMD = Surface Mounted Device

8-Bit Microprocessors

SAB 8085AH
8-Bit Microprocessor

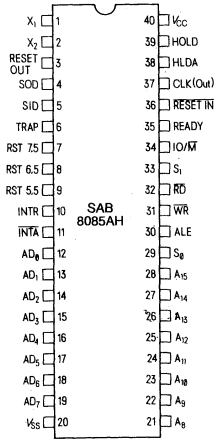
SAB 8085AH (3 MHz)

- Single +5V Power Supply with ±10% Voltage Margins
- 30% Less I_{CC} than SAB 8085A
- 100% Software Compatible with SAB 8080A
- 1.3 µs Instruction Cycle (SAB 8085AH); 0.8 µs (SAB 8085AH-2)
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control

SAB 8085AH-2 (5 MHz)

- Four Vectored Interrupt Inputs (one is Non-Maskable) Plus an SAB 8080A Compatible Interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory

Pin Diagram



Pin Names

A_8–A_{15}	Address Bus	$\overline{INTA}$	Interrupt Acknowledge
AD_0–AD_7	Mux. Address/ Data Bus	RST 5.5, 6.5, 7.5	Restart Interrupts
ALE	Address Latch Enable	TRAP	Trap
S_0, S_1, IO/$\overline{M}$	Machine Cycle Status	$\overline{RESET\ IN}$	Reset in
		RESET OUT	Reset out
$\overline{RD}$	Read Control		
$\overline{WR}$	Write Control	X_1, X_2	Crystal/Clock Input
READY	Ready	CLK	Clock Output
HOLD	Hold	SID	Serial Input Data
HLDA	Hold Acknowledge	SOD	Serial Output Data
INTR	Interrupt Request	V_{CC}	+5V
		V_{SS}	Ground (OV)

SAB 8085AH is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the SAB 8080A microprocessor. Its high level of system integration allows a minimum of three IC's [SAB 8085AH (CPU), SAB 8156 (RAM/IO) and SAB 8355/SAB 8755A (ROM/PROM/IO)] while maintaining total system expandability. The SAB 8085AH-2 is a faster version of the SAB 8085AH.

The SAB 8085AH incorporates all of the features that the SAB 8224 (clock generator) and SAB 8228 (system controller) provided for the SAB 8080A, thereby offering a high level of system integration.

The SAB 8085AH uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of SAB 8155/SAB 8156/SAB 8355/SAB 8755A memory products allow a direct interface with the SAB 8085AH.

SAB 8085AH is implemented in +5V advanced N-channel, silicon gate Siemens MYMOS technology and is a selected version of the standard SAB 8085A.

8.85

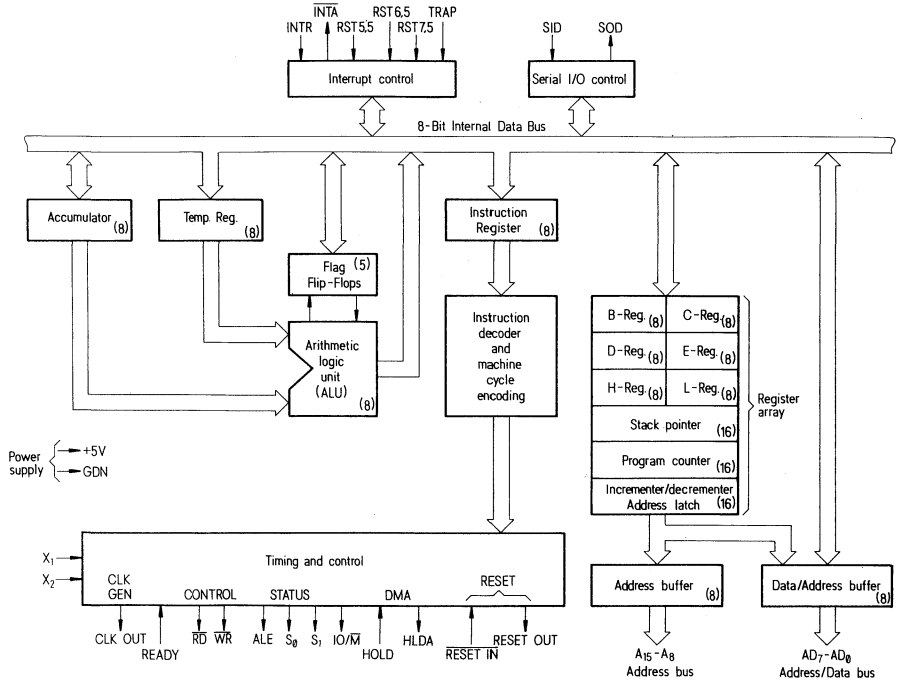
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
X_1, X_2	1, 2	I	X_1 AND X_2 – Are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
RESET OUT	3	O	RESET OUT – Reset Out indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
SOD	4	O	SERIAL OUTPUT DATA LINE – The output SOD is set or reset as specified by the SIM instruction.
SID	5	I	SERIAL INPUT DATA LINE – The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
TRAP	6	I	TRAP – Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt (see following table).
RST 5.5 RST 6.5 RST 7.5	9 8 7	I	RESTART INTERRUPTS – These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in the following table. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
INTR	10	I	INTERRUPT REQUEST – Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{\text{INTA}}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{\text{INTA}}$	11	O	INTERRUPT ACKNOWLEDGE – Is used instead of (and has the same timing as) $\overline{\text{RD}}$ during the instruction cycle after an INTR is accepted. It can be used to activate an SAB 8259A Interrupt chip or some other interrupt port.
AD_0–AD_7	12–19	I/O	MULTIPLEXED ADDRESS/DATA BUS – Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
A_8–A_{15}	21–28	O	ADDRESS BUS – The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

<table>
<tr><th>Symbol</th><th>Number</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$S_\emptyset$, S_1, and IO/$\overline{M}$</td><td>29, 33
34</td><td>O</td><td>MACHINE CYCLE STATUS –
<table>
<tr><th>IO/$\overline{M}$</th><th>S_1</th><th>$S_\emptyset$</th><th>Status</th></tr>
<tr><td>$\emptyset$</td><td>$\emptyset$</td><td>1</td><td>Memory write</td></tr>
<tr><td>$\emptyset$</td><td>1</td><td>$\emptyset$</td><td>Memory read</td></tr>
<tr><td>1</td><td>$\emptyset$</td><td>1</td><td>I/O write</td></tr>
<tr><td>1</td><td>1</td><td>$\emptyset$</td><td>I/O read</td></tr>
<tr><td>$\emptyset$</td><td>1</td><td>1</td><td>Opcode fetch</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Opcode fetch</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Interrupt Acknowledge</td></tr>
<tr><td>*</td><td>$\emptyset$</td><td>$\emptyset$</td><td>Halt</td></tr>
<tr><td>*</td><td>X</td><td>X</td><td>Hold</td></tr>
<tr><td>*</td><td>X</td><td>X</td><td>Reset</td></tr>
</table>
* = 3-state (high impedance)
X = unspecified
S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, $S_\emptyset$ and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.</td></tr>
<tr><td>ALE</td><td>30</td><td>O</td><td>ADDRESS LATCH ENABLE – It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.</td></tr>
<tr><td>$\overline{WR}$</td><td>31</td><td>O</td><td>WRITE CONTROL – A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.</td></tr>
<tr><td>$\overline{RD}$</td><td>32</td><td>O</td><td>READ CONTROL – A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.</td></tr>
<tr><td>READY</td><td>35</td><td>I</td><td>READY – If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.</td></tr>
<tr><td>$\overline{RESET\ IN}$</td><td>36</td><td>I</td><td>RESET IN – Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{RESET\ IN}$ is a Schmitt-triggered input, allowing connection to an RC network for power-on RESET delay. The CPU is held in the reset condition as long as $\overline{RESET\ IN}$ is applied.</td></tr>
<tr><td>CLK</td><td>37</td><td>O</td><td>CLOCK – Clock output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.</td></tr>
</table>

Symbol	Number	Input (I) Output (O)	Function
HLDA	38	O	HOLD ACKNOWLEDGE – Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one half clock cycle after HLDA goes low.
HOLD	39	I	HOLD – Indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
V_{CC}	40		POWER SUPPLY (+5V)
V_{SS}	20		GROUND (OV)

Functional Block Diagram



Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address Branched To[1] When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled
RST 7.5	2	3CH	Rising edge (latched)
RST 6.5	3	34H	High level until sampled
RST 5.5	4	2CH	High level until sampled
INTR	5	see Note 2	High level until sampled

NOTES
1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the CPU when the interrupt is acknowledged.

Functional Description

The SAB 8085AH is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz (SAB 8085AH) or 5 MHz (SAB 8085AH-2), thus improving on SAB 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU (SAB 8085AH), a RAM/IO (SAB 8156), and a ROM or EPROM/IO chip (SAB 8355 or SAB 8755A).

The SAB 8085AH has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The SAB 8085AH register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers; data pointer (HL)	8 bits × 6 or 16 bits × 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The SAB 8085AH uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The SAB 8085AH provides $\overline{RD}$, $\overline{WR}$, $S_\emptyset$, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The SAB 8085AH also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the SAB 8085AH has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

Interrupt and Serial I/O

The SAB 8085AH has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the SAB 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The non-maskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks (see table above).

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are **high level-sensitive** like INTR (and INT on the SAB 8080) and are recognized with the same timing as INTR. RST 7.5 is **rising edge-sensitive.**

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset

by using the SIM instruction or by issuing a $\overline{\text{RESET IN}}$ to the SAB 8085AH. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{\text{RESET IN}}$.

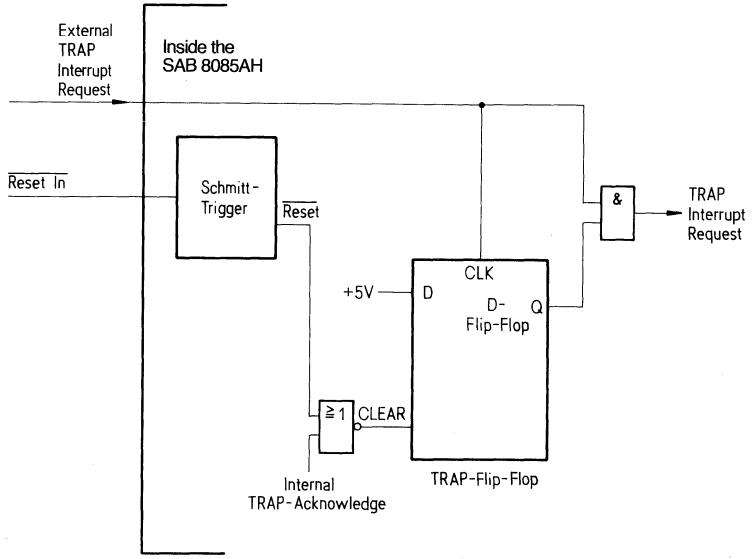
The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP – highest priority, RST 7.5, RST 6.5, RST 5.5, INTR – lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both **edge and level sensitive.** The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. The following figure illustrates the TRAP interrupt request circuitry within the SAB 8085AH. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5 – 7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

TRAP and RESET in Circuit



Driving the X_1 and X_2 Inputs

You may drive the clock inputs of the SAB 8085AH or SAB 8085AH-2 with a crystal, an LC tuned circuit, an RC network, or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the SAB 8085AH is operated with a 6 MHz crystal (for 3 MHz clock), and the SAB 8085AH-2 can be operated with a 10 MHz crystal (for 5 MHz clock).

If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired

C_L (load capacitance) $\leq$ 30 pf
C_s (shunt capacitance) $\leq$ 7 pf
R_s (equivalent shunt resistance) $\leq$ 75 Ohms
Drive level: 10 mW
Frequency tolerance: $\pm$.005% (suggested)

Note the use of the 20 pF capacitor between X_2 and ground. This capacitor is required with crystal frequencies below 4 MHz to assure oscillator startup at the correct frequency. A parallel-resonant LC circuit may be used as the frequency-determining network for the SAB 8085AH, providing that its frequency tolerance of approximately $\pm$10% is acceptable. The components are from the formula:

$$f = \frac{1}{2\pi\sqrt{L\,(C_{ext} + C_{int})}}$$

To minimize variations in frequency, it is recommended that you choose a value for C_{ext} that is at least twice that of C_{int}, or 30 pF. The use of an LC circuit is not recommended for frequencies higher than approximately 5 MHz.

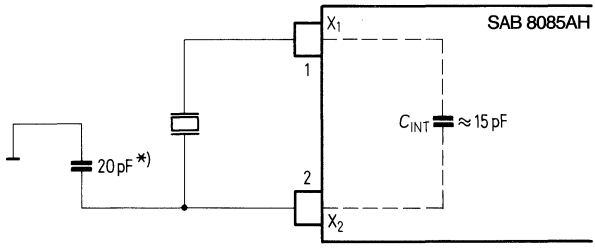
An RC circuit may be used as the frequency-determining network for the SAB 8085AH if maintaining a precise clock frequency is of no importance. Variations in the on-chip timing generation can cause a wide variation in frequency when using the RC mode. Its advantage is its low component costs. The driving frequency generated by the circuit shown is approximately 3 MHz. It is not recommended that frequencies greatly higher or lower than this be attempted.

The following figures show the recommended clock driver circuits. Note in D and E that pullup resistors are required to assure that the high level voltage of the input is at least 4V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 opencircuited (Figure D). If the driving frequency is from 6 MHz to 10 MHz, stability of the clock generator will be improved by driving both X_1 and X_2 with a pushpull source (Figure E). To prevent self-oscillation of the SAB 8085AH, be sure that X_2 is not coupled back to X_1 through the driving circuit.

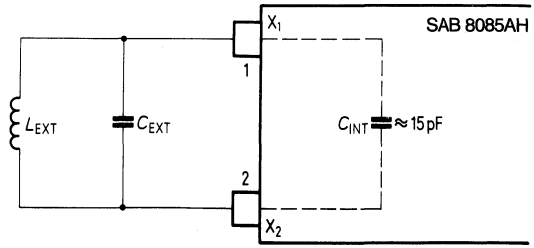
Clock Driver Circuits

A) Quartz Crystal Clock Driver

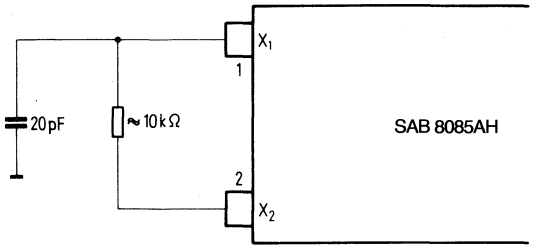


*) 20 pF Capacitors required for Crystal Frequency ≤ 4 MHz only.

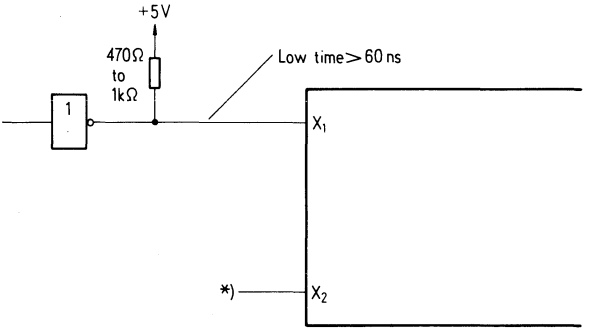
B) LC Tuned Circuit Clock Driver



C) RC Circuit Clock Driver

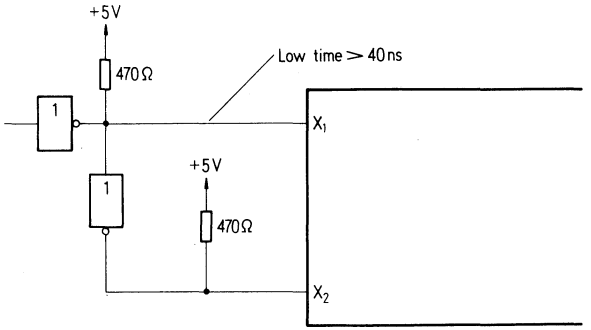


D) 1 – 6 MHz Input Frequency External Clock Driver Circuit



*) X_2 left floating

E) 1 – 10 MHz Input Frequency External Clock Driver Circuit



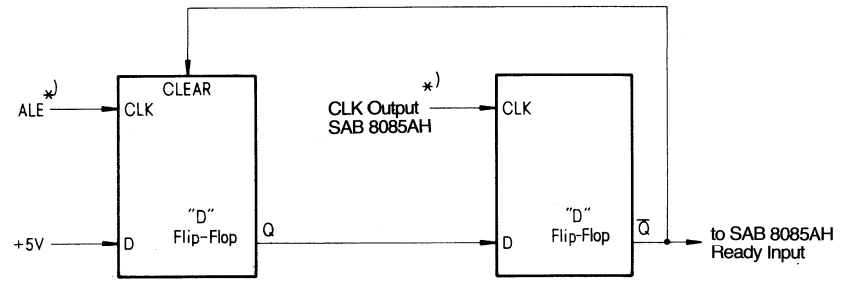
Generating Wait State

If your system requirements are such that slow memories or peripheral devices are being used, the circuit shown in the following figure may be used to insert one WAIT state in each SAB 8085AH machine cycle.

The D flip-flops should be chosen so that
- CLK is rising edge-triggered
- CLEAR is low-level active.

As in the SAB 8080, the READY line is used to extend the read and write pulse lengths so that the SAB 8085AH can be used with slow memory. HOLD causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.

Generation of a Wait State for SAB 8085AH CPU



*) ALE and CLK (Out) should be buffered if CLK Input of Latch Exceeds SAB 8085AH IOL or IOH.

System Interface

The SAB 8085A family includes memory components, which are directly compatible to the SAB 8085AH CPU. For example, a system consisting of the three chips, SAB 8085AH, SAB 8156, and SAB 8355 will have the following features:

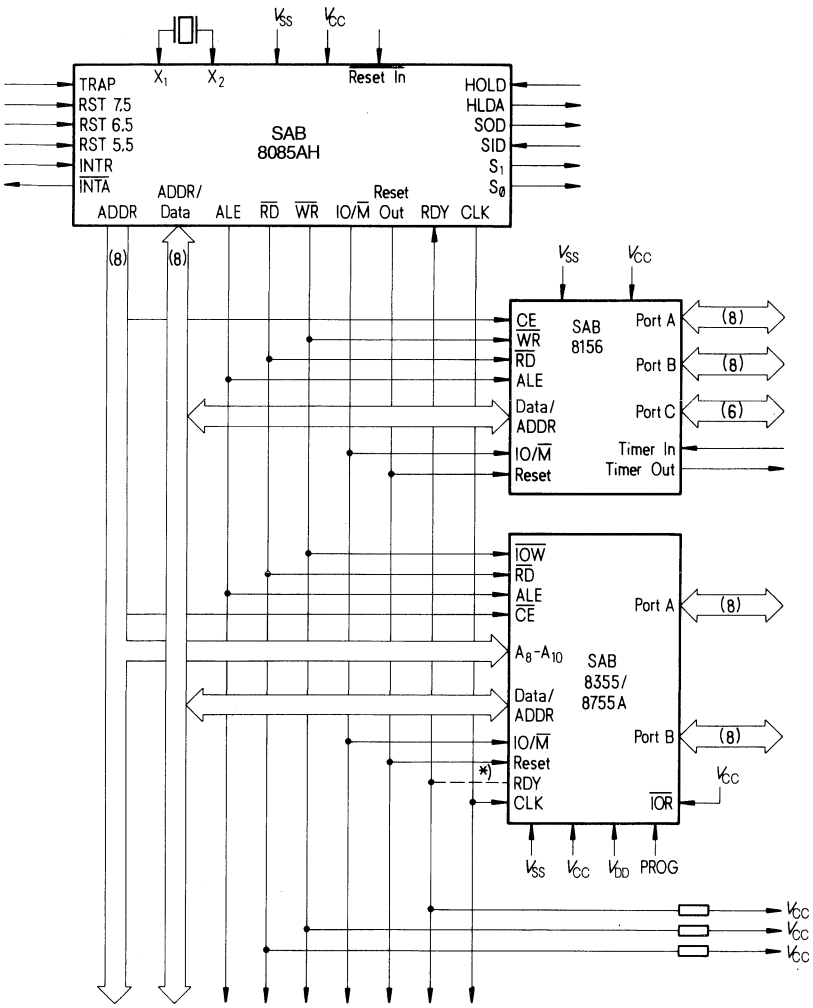
- 2K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8-bit I/O Ports
- 1 6-bit I/O Port
- 4 Interrupt Levels
- Serial In/Serial Out Ports

This minimum system, using the standard I/O technique is as shown in the following figure.

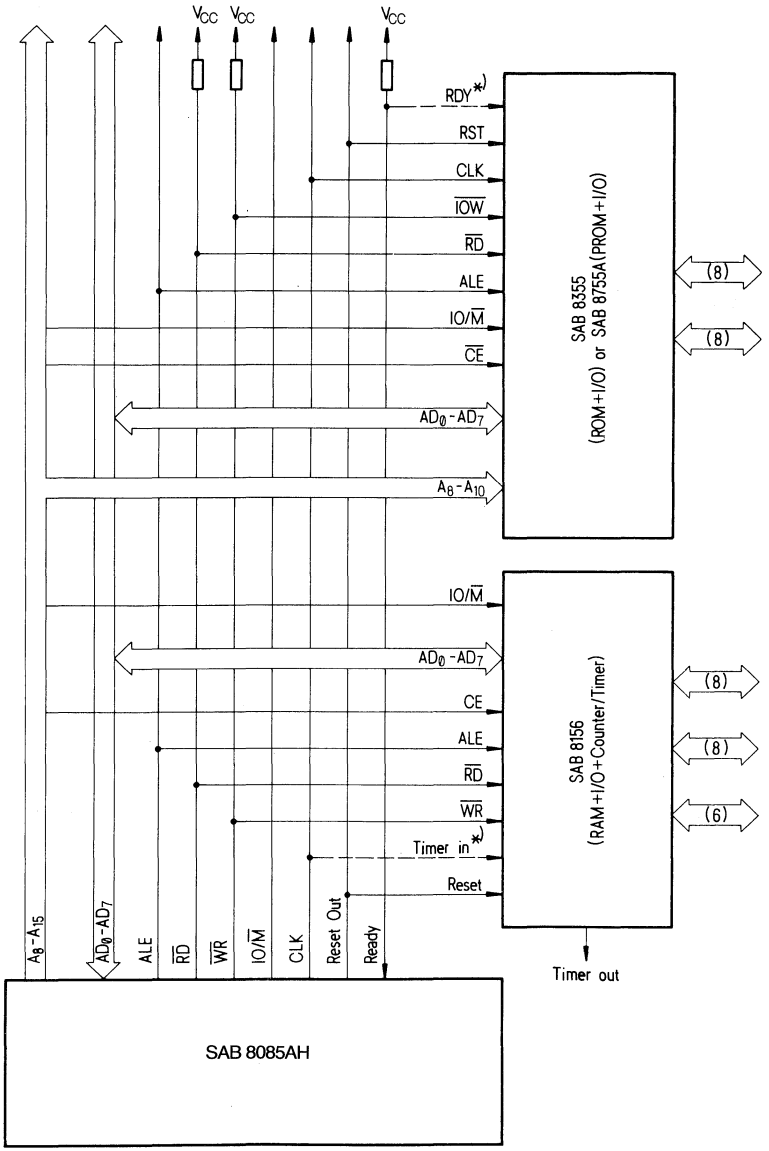
In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. The figure on page 11 shows the system configuration of Memory Mapped I/O using SAB 8085AH.

The SAB 8085AH CPU can also interface with the standard memory that does **not** have the multiplexed address/data bus. It will require a simple SAB 8282 (8-bit latch) as shown in the figure on page 12.

SAB 8085AH Minimum System (Standard I/O Technique)

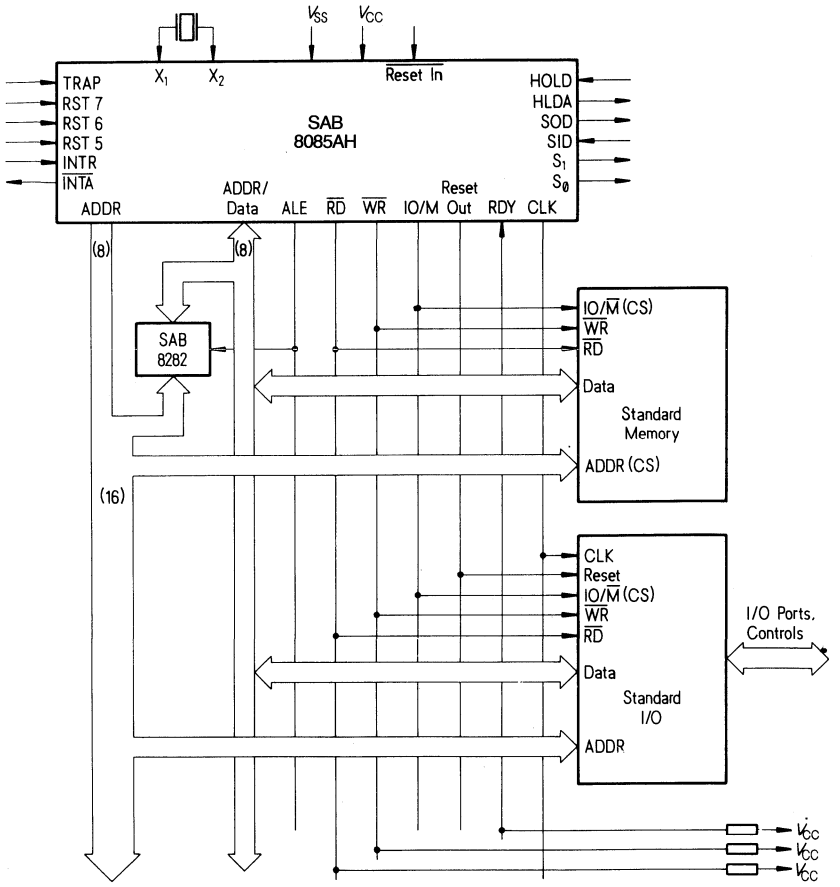


SAB 8085AH Minimum System (Memory Mapped I/O)



*) Optional Connection

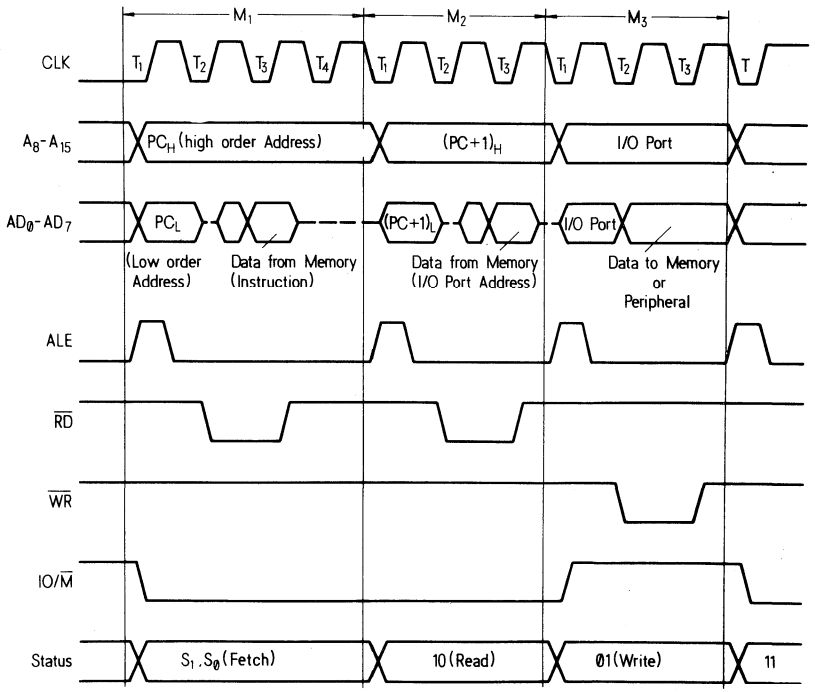
SAB 8085AH System (Using Standard Memories)



Basic System Timing

The SAB 8085AH has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. The following figure shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both, the upper and lower half of the address.

SAB 8085AH Basic System Timing



There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines (IO/$\overline{M}$, S_1, $S_\emptyset$) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$); (see following table). The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each maching cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

SAB 8085AH Machine Cycle Chart

Machine Cycle		Status			Control		
		IO/$\overline{M}$	S1	SØ	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch	(OF)	Ø	1	1	Ø	1	1
Memory Read		Ø	1	Ø	Ø	1	1
Memory Write		Ø	Ø	1	1	Ø	1
I/O Read	(IOR)	1	1	Ø	Ø	1	1
I/O Write	(IOW)	1	Ø	1	1	Ø	1
Acknowledge for INTR	(INA)	1	1	1	1	1	Ø
Bus Idle	(BI): DAD	Ø	1	Ø	1	1	1
	ACK of RST, TRAP	1	1	1	1	1	1
	HALT	TS	Ø	Ø	TS	TS	1

Ø = Logic "Ø"; 1 = Logic "1"; TS = High Impedance

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, as summarized in the following table.

SAB 8085AH Machine State Chart

Machine State	Status and Buses				Control		
	S1, SØ	IO/$\overline{M}$	A_8–A_{15}	$AD_Ø$–AD_7	$\overline{RD}$, $\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1 [1]
T_2	X	X	X	X	X	X	Ø
T_{WAIT}	X	X	X	X	X	X	Ø
T_3	X	X	X	X	X	X	Ø
T_4	1	Ø [2]	X	TS	1	1	Ø
T_5	1	Ø [2]	X	TS	1	1	Ø
T_6	1	Ø [2]	X	TS	1	1	Ø
T_{RESET}	X	TS	TS	TS	TS	1	Ø
T_{HALT}	Ø	TS	TS	TS	TS	1	Ø
T_{HOLD}	X	TS	TS	TS	TS	1	Ø

Ø = Logic "Ø"; 1 = Logic "1"; TS = High Impedance; X = Unspecified.
[1]) ALE not generated during 2nd and 3nd machine cycles of DAD instruction.
[2]) IO/$\overline{M}$ = 1 during T_4–T_6 of INA machine cycle.

Instruction Set Summary

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
MOVE, LOAD, AND STORE									
MOVr1 r2	0	1	D	D	D	S	S	S	Move register to register
MOV M.r	0	1	1	1	0	S	S	S	Move register to memory
MOV r.M	0	1	D	D	D	1	1	0	Move memory to register
MVI r	0	0	D	D	D	1	1	0	Move immediate register
MVI M	0	0	1	1	0	1	1	0	Move immediate memory
LXI B	0	0	0	0	0	0	0	1	Load immediate register Pair B & C
LXI D	0	0	0	1	0	0	0	1	Load immediate register Pair D & E
LXI H	0	0	1	0	0	0	0	1	Load immediate register Pair H & L
STAX B	0	0	0	0	0	0	1	0	Store A indirect
STAX D	0	0	0	1	0	0	1	0	Store A indirect
LDAX B	0	0	0	0	1	0	1	0	Load A indirect
LDAX D	0	0	0	1	1	0	1	0	Load A indirect
STA	0	0	1	1	0	0	1	0	Store A direct
LDA	0	0	1	1	1	0	1	0	Load A direct
SHLD	0	0	1	0	0	0	1	0	Store H & L direct
LHLD	0	0	1	0	1	0	1	0	Load H & L direct
XCHG	1	1	1	0	1	0	1	1	Exchange D & E, H & L Registers
STACK OPS									
PUSH B	1	1	0	0	0	1	0	1	Push register Pair B & C on stack
PUSH D	1	1	0	1	0	1	0	1	Push register Pair D & E on stack
PUSH H	1	1	1	0	0	1	0	1	Push register Pair H & L on stack
PUSH PSW	1	1	1	1	0	1	0	1	Push A and Flags on stack
POP B	1	1	0	0	0	0	0	1	Pop register Pair B & C off stack
POP D	1	1	0	1	0	0	0	1	Pop register Pair D & E off stack
POP H	1	1	1	0	0	0	0	1	Pop register Pair H & L off stack
POP PSW	1	1	1	1	0	0	0	1	Pop A and Flags off stack
XTHL	1	1	1	0	0	0	1	1	Exchange top of stack, H & L
SPHL	1	1	1	1	1	0	0	1	H & L to stack pointer
LXI SP	0	0	1	1	0	0	0	1	Load immediate stack pointer
INX SP	0	0	1	1	0	0	1	1	Increment stack pointer
DCX SP	0	0	1	1	1	0	1	1	Decrement stack pointer
JUMP									
JMP	1	1	0	0	0	0	1	1	Jump unconditional
JC	1	1	0	1	1	0	1	0	Jump on carry
JNC	1	1	0	1	0	0	1	0	Jump on no carry
JZ	1	1	0	0	1	0	1	0	Jump on zero
JNZ	1	1	0	0	0	0	1	0	Jump on no zero
JP	1	1	1	1	0	0	1	0	Jump on positive
JM	1	1	1	1	1	0	1	0	Jump on minus
JPE	1	1	1	0	1	0	1	0	Jump on parity even
JPO	1	1	1	0	0	0	1	0	Jump on perity odd
PCHL	1	1	1	0	1	0	0	1	H & L to program counter

Instruction Set Summary (Cont'd)

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
CALL									
CALL	1	1	0	0	1	1	0	1	Call unconditional
CC	1	1	0	1	1	1	0	0	Call on carry
CNC	1	1	0	1	0	1	0	0	Call on no carry
CZ	1	1	0	0	1	1	0	0	Call on zerro
CNZ	1	1	0	0	0	1	0	0	Call on no zerro
CP	1	1	1	1	0	1	0	0	Call on positive
CM	1	1	1	1	1	1	0	0	Call on minus
CPE	1	1	1	0	1	1	0	0	Call on parity even
CPO	1	1	1	0	0	1	0	0	Call on parity odd
RETURN									
RET	1	1	0	0	1	0	0	1	Return
RC	1	1	0	1	1	0	0	0	Return on carry
RNC	1	1	0	1	0	0	0	0	Return on no carry
RZ	1	1	0	0	1	0	0	0	Return on zero
RNZ	1	1	0	0	0	0	0	0	Return on no zero
RP	1	1	1	1	0	0	0	0	Return on positive
RM	1	1	1	1	1	0	0	0	Return on minus
RPE	1	1	1	0	1	0	0	0	Return on parity even
RPO	1	1	1	0	0	0	0	0	Return on parity odd
RESTART									
RST	1	1	A	A	A	1	1	1	Restart
INPUT/OUTPUT									
IN	1	1	0	1	1	0	1	1	Input
OUT	1	1	0	1	0	0	1	1	Output
INCREMENT AND DECREMENT									
INR r	0	0	D	D	D	1	0	0	Increment register
DCR r	0	0	D	D	D	1	0	1	Decrement register
INR M	0	0	1	1	0	1	0	0	Increment memory
DCR M	0	0	1	1	0	1	0	1	Decrement memory
INX B	0	0	0	0	0	0	1	1	Increment B & C registers
INX D	0	0	0	1	0	0	1	1	Increment D & E registers
INX H	0	0	1	0	0	0	1	1	Increment H & L registers
DCX B	0	0	0	0	1	0	1	1	Decrement B & C
DCX D	0	0	0	1	1	0	1	1	Decrement D & E
DCX H	0	0	1	0	1	0	1	1	Decrement H & L
ADD									
ADD r	1	0	0	0	0	S	S	S	Add register to A
ADC r	1	0	0	0	1	S	S	S	Add register to A with carry
ADD M	1	0	C	0	0	1	1	0	Add memory to A
ADC M	1	0	0	0	1	1	1	0	Add memory to A with carry
ADI	1	1	0	0	0	1	1	0	Add immediate to A
ACI	1	1	0	0	1	1	1	0	Add immediate to A with carry
DAD B	0	0	0	0	1	0	0	1	Add B & C to H & L
DAD D	0	0	0	1	1	0	0	1	Add D & E to H & L
DAD H	0	0	1	0	1	0	0	1	Add H & L to H & L
DAD SP	0	0	1	1	1	0	0	1	Add stack pointer to H & L

Instruction Set Summary (Cont'd)

Mnemonic	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operations Description
SUBTRACT									
SUB r	1	0	0	1	0	S	S	S	Subtract register from A
SBB r	1	0	0	1	1	S	S	S	Subtract register from A with borrow
SUB M	1	0	0	1	0	1	1	0	Subtract memory from A
SBB M	1	0	0	1	1	1	1	0	Subtract memory from A with borrow
SUI	1	1	0	1	0	1	1	0	Subtract immediate from A
SBI	1	1	0	1	1	1	1	0	Subtract immediate from A with borrow
LOGICAL									
ANA r	1	0	1	0	0	S	S	S	And register with A
XRA r	1	0	1	0	1	S	S	S	Exclusive OR register with A
ORA r	1	0	1	1	0	S	S	S	OR register with A
CMP r	1	0	1	1	1	S	S	S	Compare register with A
ANA M	1	0	1	0	0	1	1	0	And memory with A
XRA M	1	0	1	0	1	1	1	0	Exclusive OR memory with A
ORA M	1	0	1	1	0	1	1	0	OR memory with A
CMP M	1	0	1	1	1	1	1	0	Compare memory with A
ANI	1	1	1	0	0	1	1	0	And immediate with A
XRI	1	1	1	0	1	1	1	0	Exclusive OR immediate with A
ORI	1	1	1	1	0	1	1	0	OR immediate with A
CPI	1	1	1	1	1	1	1	0	Compare immediate with A
ROTATE									
RLC	0	0	0	0	0	1	1	1	Rotate A left
RRC	0	0	0	0	1	1	1	1	Rotate A right
RAL	0	0	0	1	0	1	1	1	Rotate A left throught carry
RAR	0	0	0	1	1	1	1	1	Rotate A right through carry
SPECIALS									
CMA	0	0	1	0	1	1	1	1	Complement A
STC	0	0	1	1	0	1	1	1	Set carry
CMC	0	0	1	1	1	1	1	1	Complement carry
DAA	0	0	1	0	0	1	1	1	Decimal adjust A
CONTROL									
EI	1	1	1	1	1	0	1	1	Enable interrupts
DI	1	1	1	1	0	0	1	1	Disable Interrupt
NOP	0	0	0	0	0	0	0	0	No-operation
HLT	0	1	1	1	0	1	1	0	Halt
NEW SAB 8085AH INSTRUCTIONS									
RIM	0	0	1	0	0	0	0	0	Read Interrupt Mask
SIM	0	0	1	1	0	0	0	0	Set Interrupt Mask

NOTES
1. DDS or SSS: B 000, C 001, D 010, E 011, H 100, L 101, Memory 110, A 111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

Absolute maximum ratings *)

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on any Pin with Respect to Ground	−0.5 to +7 V
Power Dissipation	1.5 Watt

D.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±10%; V_{SS} = 0 V; (unless otherwise specified)

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	+0.8	V	–
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5		
V_{OL}	Output Low Voltage	–	0.45		I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4	–		I_{OH} = −400 µA
I_{CC}	Power Supply Current	–	120	mA	–
I_{IL}	Input Leakage		±10	µA	$0 \lesssim V_{IN} \lesssim V_{CC}$
I_{LO}	Output Leakage				$0.45\,V \leq V_{OUT} \leq V_{CC}$
V_{ILR}	Input Low Level, RESET	−0.5	+0.8	V	–
V_{IHR}	Input High Level, RESET	2.4	V_{CC}+0.5		
V_{HY}	Hysteresis, RESET	0.25			

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values				Units
		SAB 8085AH [2]		SAB 8085AH-2 [2]		
		Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	ns
t_1	CLK Low Time (Standard CLK Loading)	80	–	40	–	
t_2	CLK High Time Standard CLK Loading)	120		70		
t_r, t_f	CLK Rise and Fall Time		30	–	30	
t_{XKR}	X_1 Rising to CLK Rising	30	120	30	100	
t_{XKF}	X_1 Rising to CLK Falling		150		110	
t_{AC}	A_8–A_{15} Valid to Leading Edge of Control [1]	270	–	115	–	
t_{ACL}	$A_\emptyset$–A_7 Valid to Leading Edge of Control	240				
t_{AD}	$A_\emptyset$–A_{15} Valid to Valid Data In	–	575	–	350	
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0		0	
t_{AL}	A_8–A_{15} Valid Before Trailing Edge of ALE [1]	115	–	50	–	
t_{ALL}	$A_\emptyset$–A_7 Valid Before Trailing Edge of ALE	90				
t_{ARY}	READY Valid from Address Valid	–	220	–	100	
t_{CA}	Address (A_8–A_{15}) Valid After Control	120	–	60	–	
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	400		230		
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		230		
t_{HABE}	HLDA to Bus Enable	–	210	–	150	
t_{HABF}	Bus Float After HLDA					
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110	–	40	–	
t_{HDH}	HOLD Hold Time	0		0		
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		
t_{INH}	INTR Hold Time	0		0		
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		150		
t_{LA}	Address Hold Time After ALE	100		50		
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		60		
t_{LCK}	ALE Low During CLK High	100		50		

Notes see next page.

A.C. Characteristics (continued)

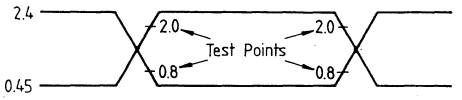
Symbol	Parameter	Limit Values				Units
		SAB 8085AH[2]		SAB 8085AH-2[2]		
		Min.	Max.	Min.	Max.	
t_{LDR}	ALE to Valid Data During Read	–	460	–	270	
t_{LDW}	ALE to Valid Data During Write		200		120	
t_{LL}	ALE Width	140	–	80	–	
t_{LRY}	ALE to READY Stable	–	110	–	30	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150	–	90	–	
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data	–	300	–	150	
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400	–	220	–	ns
t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$[7]	0		0		ns
t_{RYH}	READY Hold Time					
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		100		
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	100		60		
t_{WDL}	LEADING Edge of WRITE to Data Valid	–	40	–	20	

NOTES

1. A_8–A_{15} address Specs apply to IO/$\overline{M}$, $S_\emptyset$, and S_1 except A_8–A_{15} are undefined during T_4–T_6 of OF cycle, whereas IO/$\overline{M}$, $S_\emptyset$, and S_1 are stable.
2. **Test conditions:** t_{CYC} = 320 ns (SAB 8085AH)/200 ns (SAB 8085AH-2); C_L = 150 pF.
3. For all output timing where C_L = 150 pF use the following correction factors:
   25 pF $\leq C_L <$ 150 pF: −0.10 ns/pF
   150 pF $< C_L \leq$ 300 pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. All timings are measured at output votage V_L = 0.8V, V_H = 2.0V, and 1.5V with 20 ns rise and fall time on inputs.
6. To calculate timing specifications at other values of t_{CYC} the following table should be used.
7. Data hold time is guaranteed under all loading conditions.

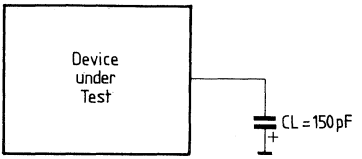
A.C. Testing

Input, Output Waveform



A.C. Testing: Input are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0".
Timing Measurements are made at 2.0 V for a Logic "1" and 0.8 V for a Logic "0".

Load Circuit



C_L = 150 pF
C_L = includes JIG Capacitance

Bus Timing Specification as a t_{CYC} Dependent

SAB 8085AH

Symb.	Min.	Max.
t_{AL}	(1/2) T − 45	
t_{LA}	(1/2) T − 60	
t_{LL}	(1/2) T − 20	−
t_{LCK}	(1/2) T − 60	
t_{LC}	(1/2) T − 30	
t_{AD}	−	(5/2 + N) T − 225
t_{RD}		(3/2 + N) T − 180
t_{RAE}	(1/2) T − 10	
t_{CA}	(1/2) T − 40	
t_{DW}	(3/2 + N) T − 60	
t_{WD}	(1/2) T − 60	−
t_{CC}	(3/2 + N) T − 80	
t_{CL}	(1/2) T − 110	
t_{ARY}	−	(3/2) T − 260
t_{HACK}	(1/2) T − 50	−
t_{HABF}	−	(1/2) T + 50
t_{HABE}		(1/2) T + 50
t_{AC}	(2/2) T − 50	
t_1	(1/2) T − 80	−
t_2	(1/2) T − 40	
t_{RV}	(3/2) T − 80	
t_{LDR}	−	(4/2) T − 180

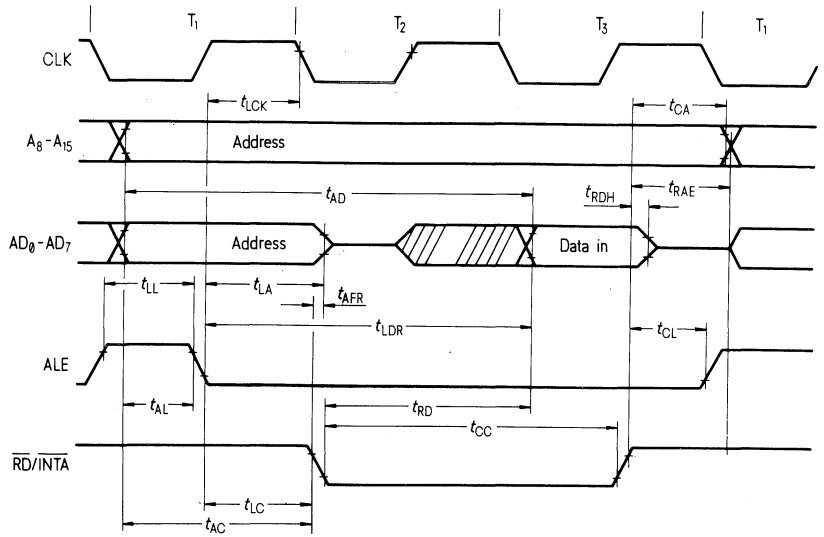
SAB 8085AH-2

Symb.	Min.	Max.
t_{AL}	(1/2) T − 50	
t_{LA}	(1/2) T − 50	
t_{LL}	(1/2) T − 20	−
t_{LCK}	(1/2) T − 50	
t_{LC}	(1/2) T − 40	
t_{AD}	−	(5/2 + N) T − 150
t_{RD}		(3/2 + N) T − 150
t_{RAE}	(1/2) T − 10	
t_{CA}	(1/2) T − 40	
t_{DW}	(3/2 + N) T − 70	−
t_{WD}	(1/2) T − 40	
t_{CC}	(3/2 + N) T − 70	
t_{CL}	(1/2) T − 75	
t_{ARY}	−	(3/2) T − 200
t_{HACK}	(1/2) T − 60	−
t_{HABF}	−	(1/2) T + 50
t_{HABE}		(1/2) T + 50
t_{AC}	(2/2) T − 85	
t_1	(1/2) T − 60	−
t_2	(1/2) T − 30	
t_{RV}	(3/2) T − 80	
t_{LDR}	−	(4/2) T − 130

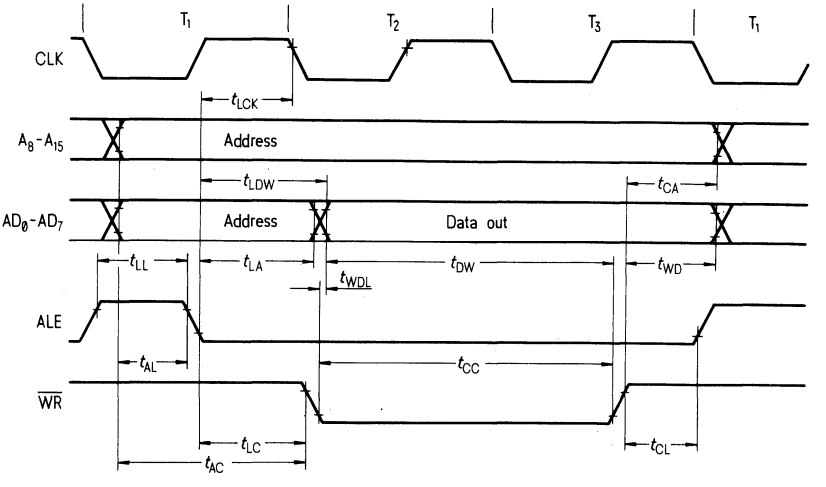
N is equal to the total WAIT states. T = t_{CYC}.

Waveforms

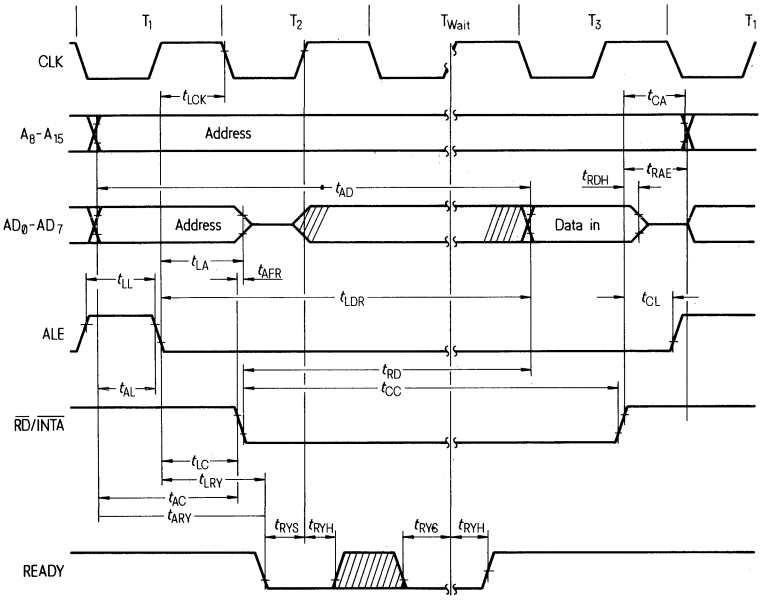
Read



Write

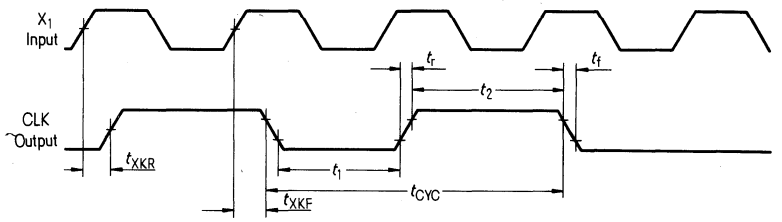


Read Operation with Cycle (Typical) – Same Ready Timing Applies to Write

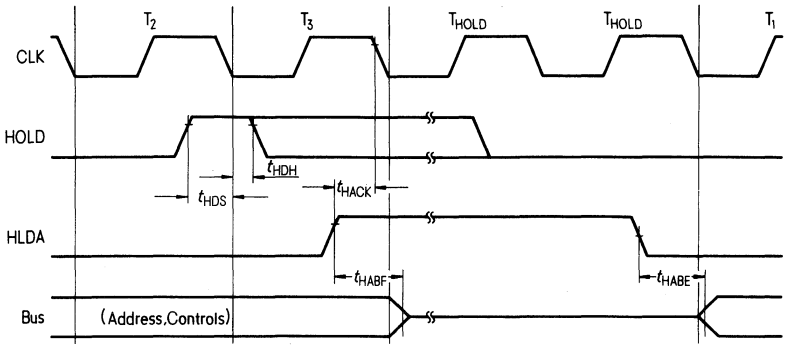


READY must remain stable during setup and hold times.

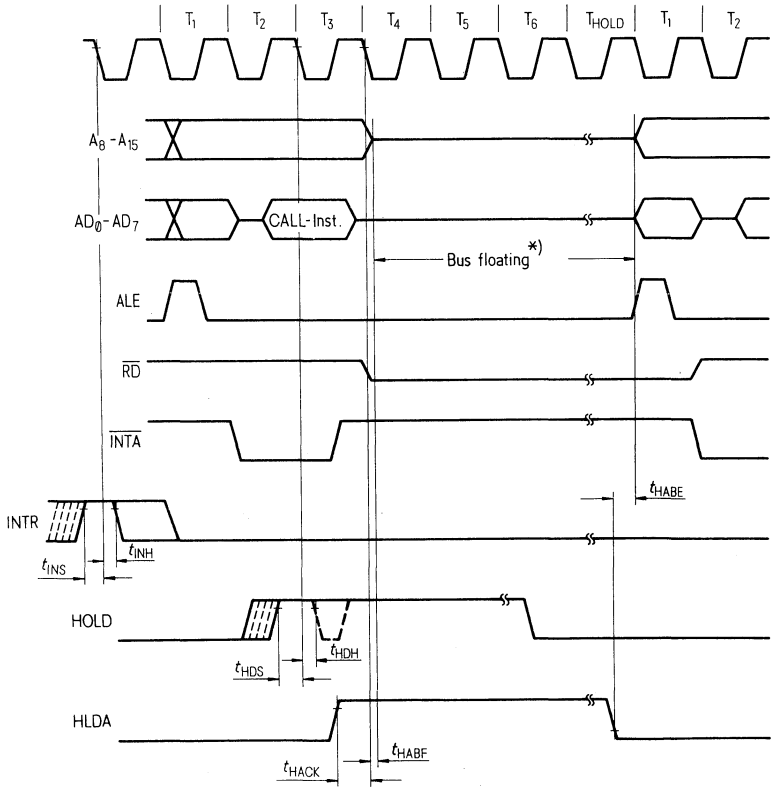
Clock


X1
Input
CLK
Output
tr
t2
tf
tXKR
t1
tXKF
tCYC

Hold


T2
T3
THOLD
THOLD
T1
CLK
HOLD
tHDH
tHACK
tHDS
HLDA
tHABF
tHABE
Bus
(Address,Controls)

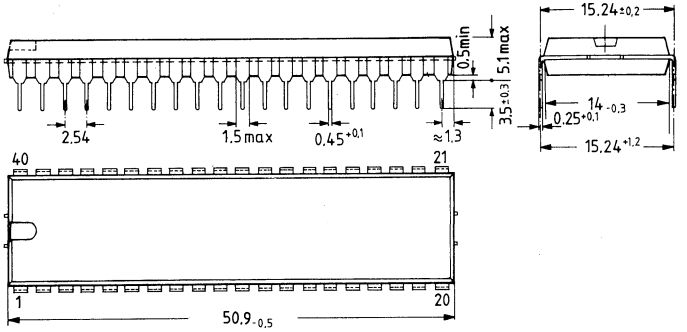
Interrupt and Hold



*) IO/$\overline{M}$ is also floating during this time.

Package Outline

40 Pin Plastic Package Type P



Ordering Information

Component	Description	Ordering Number
	8-Bit Microprocessor	
SAB 8085AH-P	3 MHz, 1.3 µs, (plastic)	Q 67120-C122
SAB 8085AH-2-P	5 MHz, 0.8 µs, (plastic)	Q 67120-C124

Preliminary

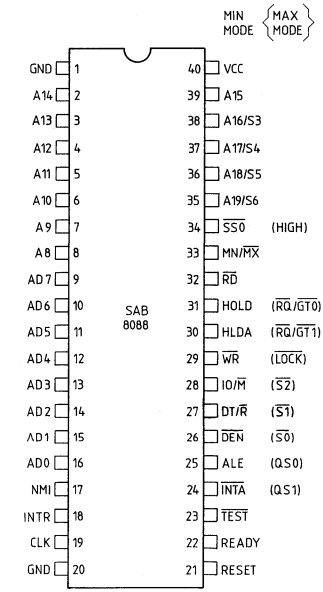
SAB 8088
8-Bit Microprocessor

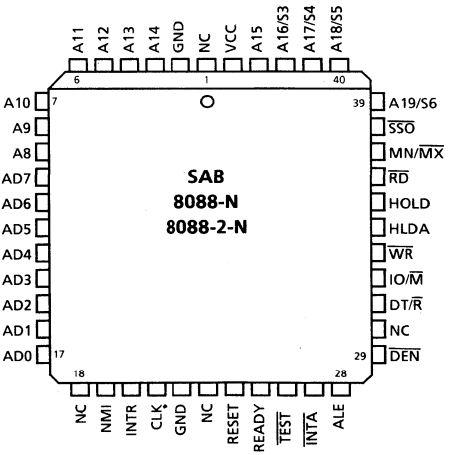
SAB 8088 5 MHz
SAB 8088-2 8 MHz

SAB 8088-1 10 MHz

- 8-bit data bus interface
- 16-bit internal architecture
- Direct addressing capability to 1 Mbyte of memory
- Software compatible with SAB 8086
- 14-word by 16-bit register set with symetrical operations
- Byte, word and block operations
- 24 operand addressing modes
- 8-bit and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide
- Three clock rates:
  5 MHz for SAB 8088
  8 MHz for SAB 8088-2
  10 MHz for SAB 8088-1
- Compatible with industry standard 8088

Pin Configuration





SAB 8088 is a high-performance 8-bit microprocessor implemented in +5V advanced Siemens MYMOS technology, packaged in a 40-pin package. It is 100 percent compatible with the industry standard 8088. With features like string handling, 16-bit arithmetic with multiply and divide it significantly increases system performance. It is highly suited for multiprocessor applications in various configurations.

10.86

Pin Definitions and Functions

The following pin definitions are for SAB 8088 systems in **either minimum or maximum mode.** The "local bus" in these descriptions is the direct multiplexed bus interface connection to the SAB 8088 (without regard to additional bus buffers).

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>AD7–AD0</td><td>9–16</td><td>I/O</td><td>ADDRESS DATA BUS:
These lines constitute the time multiplexed memory I/O address (T1) and data (T2, T3, TW, and T4) bus. These lines are active high and float to tristate off during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A15–A8</td><td>39, 2–8</td><td>O</td><td>ADDRESS BUS:
These lines provide address bits 8 through 15 for the entire bus cycle (T1–T4). These lines do not have to be latched by ALE to remain valid. A15–A8 are active high and float to tristate off during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A19/S6, A18/S5,
A17/S4, A16/S3</td><td>34–38</td><td>O</td><td>ADDRESS/STATUS:
During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are low. During memory and I/O operations, status information is available on these lines during T2, T3, TW and T4. S6 is always low. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown.
<table>
<tr><th>S4</th><th>S3</th><th>Characteristics</th></tr>
<tr><td>0</td><td>0</td><td>Alternate Data</td></tr>
<tr><td>0</td><td>1</td><td>Stack</td></tr>
<tr><td>1</td><td>0</td><td>Code or None</td></tr>
<tr><td>1</td><td>1</td><td>Data</td></tr>
</table>
This information indicates which segment register is presently being used for data accessing.
These lines float to tristate off during local bus "hold acknowledge".</td></tr>
<tr><td>$\overline{RD}$</td><td>32</td><td>O</td><td>$\overline{READ}$:
Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/$\overline{M}$ pin or S2. This signal is used to read devices which reside on the SAB 8088 local bus. $\overline{RD}$ is active low during T2, T3 and TW of any read cycle, and is guaranteed to remain high in T2 until the SAB 8088 local bus has floated.
This signal floats to tristate off in "hold acknowledge".</td></tr>
<tr><td>READY</td><td>22</td><td>I</td><td>READY:
This is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the SAB 8284A/8284B clock generator to form READY. This signal is active high. The SAB 8088 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.</td></tr>
<tr><td>INTR</td><td>18</td><td>I</td><td>INTERRUPT REQUEST:
This is a level-triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation.
A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active high.</td></tr>
</table>

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{TEST}}$	23	I	$\overline{\text{TEST}}$: This input is examined by the "wait for test" instruction. If the $\overline{\text{TEST}}$ input is low, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: This is an edge-triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from low to high initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: Causes the processor to immediately terminate its present activity. The signal must be active high for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns low. RESET is internally synchronized.
CLK	19	I	CLOCK: Provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
VCC	40	–	POWER SUPPLY (+5V)
GND	1, 20	–	GROUND (OV)
MN/$\overline{\text{MX}}$	33	I	MINIMUM/$\overline{\text{MAXIMUM}}$: Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

Pin Definitions and Functions (cont'd)

The following pin definitions are for the SAB 8088 **minimum mode** (i.e. MN/$\overline{MX}$ = VCC). Only the pin functions which are unique to minimum mode are described; all other pin functions are as already described.

Symbol	Pin	Input (I) Output (O)	Function
IO/$\overline{M}$	28	O	STATUS LINE: Is an inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = high, M = low). IO/$\overline{M}$ floats to tristate off in local bus "hold acknowledge".
$\overline{WR}$	29	O	$\overline{WRITE}$: The write strobe indicates that the processor is performing a write memory or write I/O cycle depending on the state of the IO/$\overline{M}$ signal. $\overline{WR}$ is active for T2, T3, and TW of any write cycle. It is active low, and floats to tristate off in local bus "hold acknowledge".
$\overline{INTA}$	24	O	$\overline{INTERRUPT\ ACKNOWLEDGE}$: Is used as a read strobe for interrupt acknowledge cycles. It is active low during T2, T3, and TW of each interrupt acknowledge cycle.
ALE	25	O	ADDRESS LATCH ENABLE: Is provided by the processor to latch the address into the SAB 8282 /8282A/8283/8283A address latch. It is a high pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/$\overline{RECEIVE}$: Is needed in a minimum system that desires to use an SAB 8286/8286A/8287/8287A data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T = high, R = low). This signal floats to tristate off in local "hold acknowledge".
$\overline{DEN}$	26	O	$\overline{DATA\ ENABLE}$: Is provided as an output enable for the SAB 8286/8286A/8287/8287A in a minimum system which uses the transceiver. $\overline{DEN}$ is active low during each memory and I/O access, and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ floats to tristate off during local bus "hold acknowledge".
HOLD, HLDA	31, 30	I/O	HOLD: Indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active high. The processor receiving the "hold" request will issue HLDA (high) as an acknowledgement, in the middle of a T4 or T1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being low, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{SS0}$	34	O	STATUS LINE: Is logically equivalent to $\overline{S0}$ in the maximum mode. The combination of $\overline{SS0}$, IO/$\overline{M}$ and DT/$\overline{R}$ allows the system to completely decode the current bus cycle status.

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SS0}$	Characteristics
1	0	0	Interrupt Acknowledge
1	0	1	Read I/O Port
1	1	0	Write I/O Port
1	1	1	Halt
0	0	0	Code Access
0	0	1	Read Memory
0	1	0	Write Memory
0	1	1	Passive

Pin Definitions and Functions (cont'd)

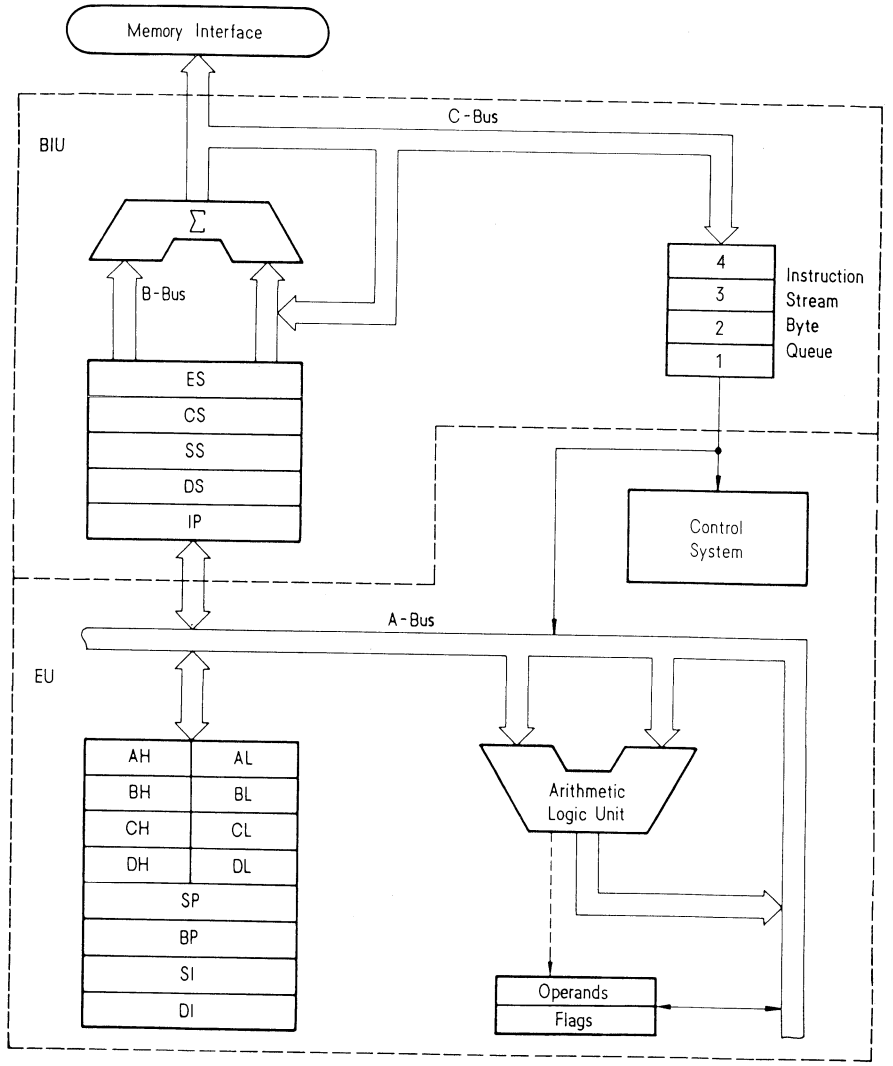
The following pin definitions are for the SAB 8088/8288 system in **maximum mode** (i.e. MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described. All other pin functions are as already described.

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{S2}$, $\overline{S1}$, $\overline{S0}$</td><td>28–26</td><td>O</td><td>$\overline{STATUS}$:
Is active during clock high of T4, T1, and T2, and is returned to the passive state (1,1,1) during T3 or during TW when READY is high. This status is used by the SAB 8288/8288A bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or TW is used to indicate the end of a bus cycle.
These signals float to tristate off during "hold acknowledge". During the first clock cycle after RESET becomes active, these signals are active high. After this first clock, they float to tristate off.
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Characteristics</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Code Access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table>
</td></tr>
<tr><td>$\overline{RQ}$/$\overline{GT0}$
$\overline{RQ}$/$\overline{GT1}$</td><td>31
30</td><td>I/O
I/O</td><td>$\overline{REQUEST}$/$\overline{GRANT}$:
Pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}$/$\overline{GT0}$ having higher priority than $\overline{RQ}$/$\overline{GT1}$. $\overline{RQ}$/$\overline{GT}$ has an internal pullup resistor so may be left unconnected. The request/grant sequence is as follows (see page 38):
1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to the SAB 8088 (pulse 1).
2. During a T4 or T1 clock cycle, a pulse one clock wide from the SAB 8088 to the requesting master (pulse 2), indicates that the SAB 8088 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge". The same rules as for HOLD/HOLDA apply when the bus is released.
3. A pulse one CLK wide from the requesting master indicates to the SAB 8088 (pulse 3) that the "hold" request is about to end and that the SAB 8088 can reclaim the local bus at the next CLK. The CPU then enters T4.
Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active low.</td></tr>
</table>

Pin Definitions and Functions (cont'd)

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td></td><td></td><td></td><td>If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met:
1. Request occurs on or before T2.
2. Current cycle is not the low byte of a word.
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.
If the local bus is idle when the request is made the two possible events will follow:
1. Local bus will be released during the next clock.
2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.</td></tr>
<tr><td>$\overline{\text{LOCK}}$</td><td>29</td><td>O</td><td>$\overline{\text{LOCK}}$:
Indicates that other system bus masters are not to gain control of the system bus while $\overline{\text{LOCK}}$ is active (low). The $\overline{\text{LOCK}}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active low, and floats to tristate off in "hold acknowledge".</td></tr>
<tr><td>QS1, QS0</td><td>24, 25</td><td>O</td><td>QUEUE STATUS:
Provide status to allow external tracking of the internal SAB 8088 instruction queue.
The queue status is valid during the CLK cycle after which the queue operation is performed.
<table><tr><th>QS1</th><th>QS0</th><th>Characteristics</th></tr><tr><td>0</td><td>0</td><td>No Operation</td></tr><tr><td>0</td><td>1</td><td>First Byte of Op Code from Queue</td></tr><tr><td>1</td><td>0</td><td>Empty the Queue</td></tr><tr><td>1</td><td>1</td><td>Subsequent Byte from Queue</td></tr></table></td></tr>
<tr><td>–</td><td>34</td><td>O</td><td>Pin 34 is always high in the maximum mode.</td></tr>
</table>

Block Diagram



Functional Description

Memory Organization

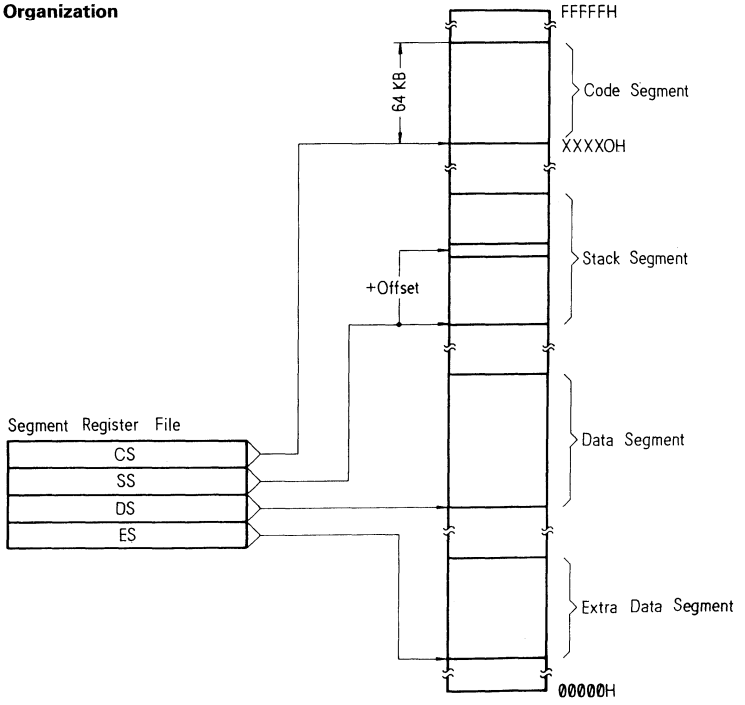
The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64 Kbytes each, with each segment falling on 16-byte boundaries.

All memory references are made relative to base addresses contained in high-speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type shares the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU will automatically execute two fetch or write cycles for 16-bit operands.

Certain locations in memory are reserved for specific CPU operations. Locations from addresses FFFF0H trough FFFFFH are reserved for operations including a jump to the initial system initialization routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Four-byte pointers consisting of a 16-bit segment address and a 16-bit offset address direct program flow to one of the 256 possible interrupt service routines. The pointer elements are assumed to have been stored at their respective places in reserved memory prior to the occurrence of interrupts.

Memory Organization



Minimum and Maximum Modes

The requirements for supporting minimum and maximum SAB 8088 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the SAB 8088 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the SAB 8088 defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to VCC, the SAB 8088 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode SAB 8088 can be used with either a multiplexed or demultiplexed bus. The multiplexed bus configuration is compatible with the SAB 8085A multiplexed bus peripherals (e.g. SAB 8155) and provides the user with a minimum chip count system. This architecture provides the SAB 8088 processing power in a highly integrated form.

The demultiplexed mode requires one latch (for 64K addressability) or two latches (for a full megabyte of addressing). A third latch can be used for buffering if the address bus loading requires it. An SAB 8286/8286A or SAB 8287/8287A transceiver can also be used if data bus buffering is required. The SAB 8088 provides $\overline{DEN}$ and DT/$\overline{R}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the SAB 8288/8288A bus controller. The SAB 8288/8288A decodes status lines $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$, and provides the system with all bus control signals. Moving the bus control to the SAB 8288/8288A provides better source and sink current capability to the control lines, and frees the SAB 8088 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the SAB 8088 in maximum mode. These features allow coprocessors in local bus and remote bus configurations.

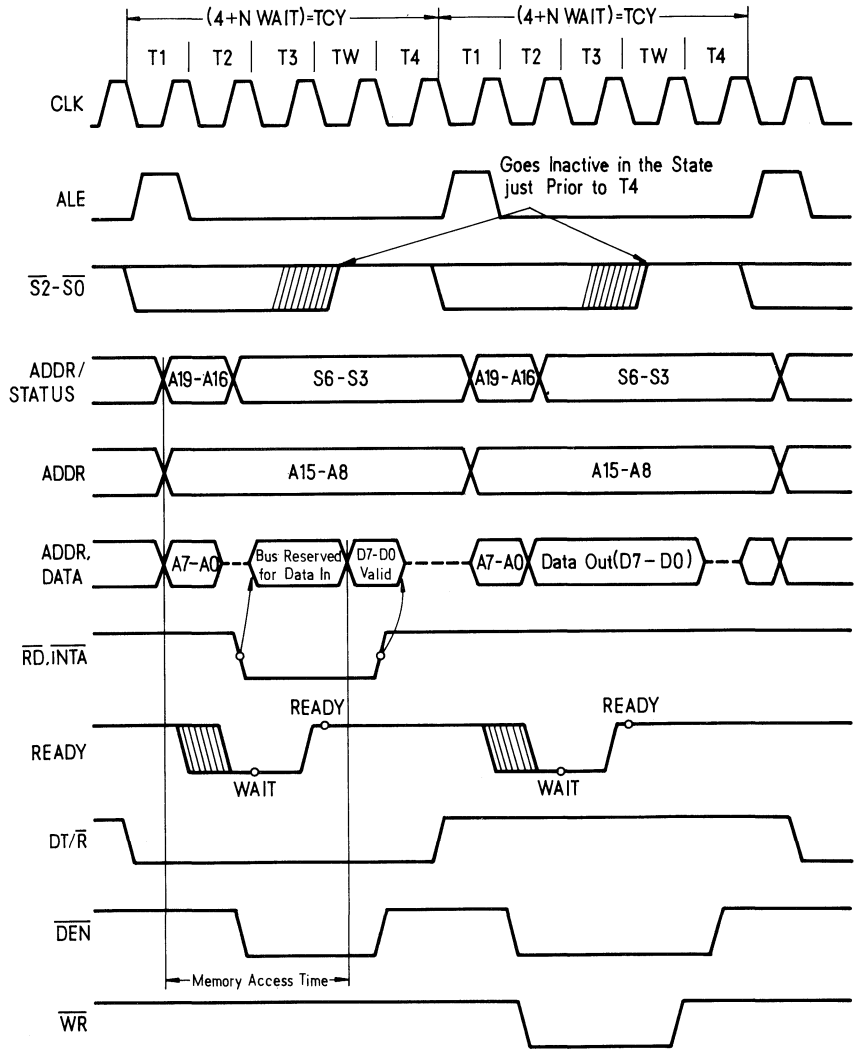
Bus Operation

The SAB 8088 address/data bus is broken into three parts – the lower eight address/data bits (AD0–AD7), the midle eight address bits (A8–A15), and the upper four address bits (A16–A19). The address/data bits and the highest four address bits are time multiplexed. This technique provides the most efficient use of pins on the processor, permitting the use of a standard 40 lead package. The middle eight address bits are not multiplexed, i.e. they remain valid throughout each bus cycle. In addition, the bus can be demultiplexed at the processor with a single address latch if a standard, non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4. The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, wait states (TW) are inserted between T3 and T4. Each inserted wait state is of the same duration as a CLK cycle. Periods can occur between SAB 8088 driven bus cycles. These are referred to as "idle" states (Ti), or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T1 of any bus cycle, the ALE (address latch enable) signal is emitted (by either the processor or the SAB 8288/8288A bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Basic System Timing



Status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (Low)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (High)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S3 through S6 are multiplexed with high-order address bits and are therefore valid during T2 through T4. S3 and S4 indicate which segment register was used for this bus cycle in forming the address according to the following table:

S4	S3	Characteristics
0 (Low)	0	Alternate Data (extra segment)
0	1	Stack
1 (High)	0	Code or None
1	1	Data

S5 is a reflection of the PSW interrupt enable bit. S6 is always equal to 0.

I/O Addressing

In the SAB 8088, I/O operations can address up to a maximum of 64 K I/O registers. The I/O address appears in the same format as the memory address on bus lines A15 to A0. The address lines A19 to A16 are zero in I/O operations. The variable I/O instructions, which use register DX as a pointer have full address capability, while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space. I/O ports are addressed in the same manner as memory locations.

Design engineers familiar with the SAB 8085 or upgrading an SAB 8085 design should observe that the SAB 8085 addresses I/O with an 8-bit address on both halves of the 16-bit address bus. The SAB 8088 uses a full 16-bit address on its lower 16 address lines.

System Components

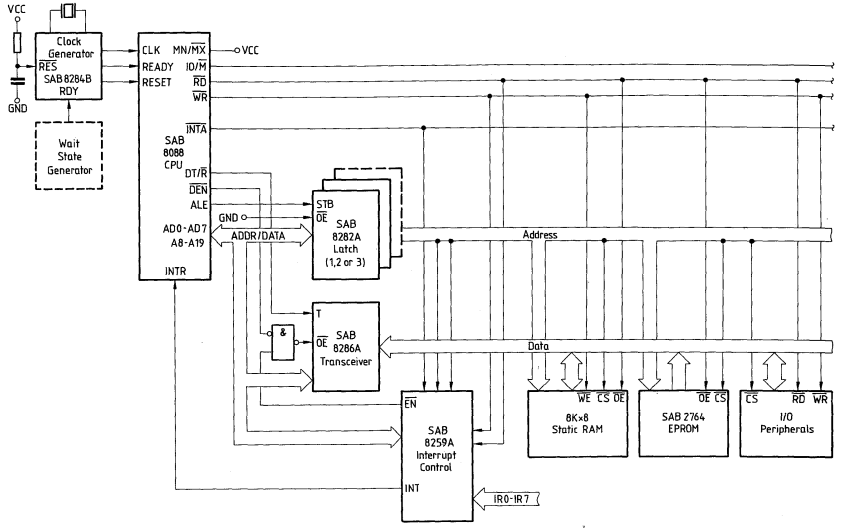
Support Circuits

SAB 8282/8282A	Octal Latch
SAB 8283/8283A	Octal Latch (inverting)
SAB 8284A/8284B	Clock Generator and Driver
SAB 8286/8286A	Octal Bus Transceiver
SAB 8287/8287A	Octal Bus Transceiver (inverting)
SAB 8288/8288A	Bus Controller
SAB 8289	Bus Arbiter
SAB 8259A	Programmable Interrupt Controller

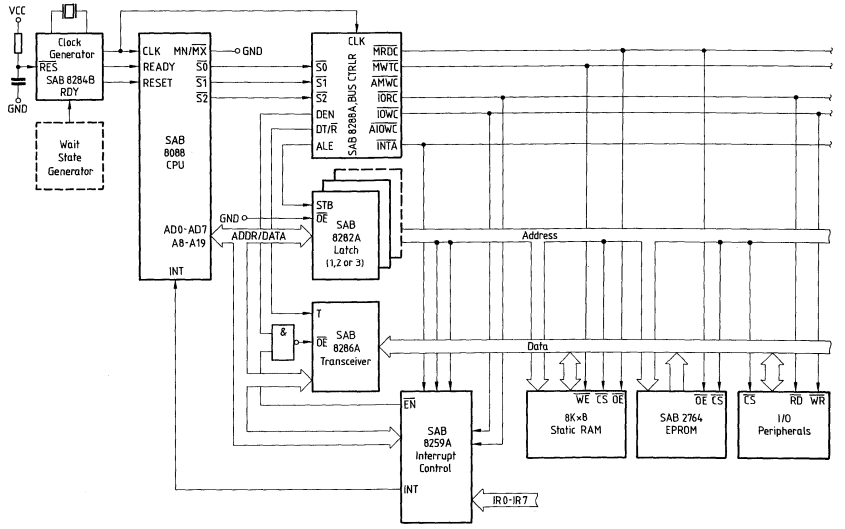
Typical Applications

The SAB 8088 is a general-purpose 8-bit microprocessor which can be used for applications ranging from process control to data processing. The next page shows typical system configurations for SAB 8088 familiy components.

Minimum Mode SAB 8088 Typical System Configuration



Maximum Mode SAB 8088 Typical System Configuration



Instruction Set Summary

Data Transfer
MOV = Move:

	76543210	76543210	76543210	76543210
Register / memory to / from register	100010dw	mod reg r/m		
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1
Immediate to register	1011w reg	data	data if w=1	
Memory to accumulator	1010000w	addr-low	addr-high	
Accumulator to memory	1010001w	addr-low	addr-high	
Register/memory to segment register	10001110	mod 0 reg r/m		
Segment register to register/memory	10001100	mod 0 reg r/m		

PUSH = Push:

Register/memory	11111111	mod 110 r/m
Register	01010 reg	
Segment register	000 reg 110	

POP = Pop:

Register/memory	10001111	mod 000 r/m
Register	01011 reg	
Segment register	000 reg 111	

XCHG = Exchange:

Register/memory with register	1000011w	mod reg r/m
Register with accumulator	10010 reg	

IN = Input from:

Fixed port	1110010w	port
Variable port	1110110w	

OUT = Output to:	76543210	76543210	76543210	76543210
Fixed port	1110011w	port		
Variable port	1110111w			
XLAT = Translate byte to AL	11010111			
LEA = Load EA to register	10001101	mod reg r/m		
LDS = Load pointer to DS	11000101	mod reg r/m		
LES = Load pointer to ES	11000100	mod reg r/m		
LAHF = Load AH with flags	10011111			
SAHF = Store AH into flags	10011110			
PUSHF = Push flags	10011100			
POPF =Pop flags	10011101			

Arithmetic

ADD = Add:				
Reg./memory with register to either	000000dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s: w=01
Immediate to accumulator	0000010w	data	data if w=1	

ADC = Add with carry:				
Reg./memory with register to either	000100dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s:w=01
Immediate to accumulator	0001010w	data	data if w=1	

INC = Increment:				
Register/memory	1111111w	mod 000 r/m		
Register	01000reg			
AAA = ASCII adjust for add	00110111			
DAA = Decimal adjust for add	00100111			

	76543210	76543210	76543210	76543210
SUB = Subtract:				
Reg./memory and register to either	001010dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s:w=01
Immediate from accumulator	0010110w	data	data if w=1	
SBB = Subtract with borrow:				
Reg./memory and register to either	000110dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s:w=01
Immediate from accumulator	0001110w	data	data if w=1	
DEC = Decrement:	76543210	76543210	76543210	76543210
Register/memory	1111111w	mod 001 r/m		
Register	01001reg			
NEG = Change sign	1111011w	mod 011 r/m		
CMP = Compare:				
Register/memory and register	001110dw	mod reg r/m		
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s:w=01
Immediate with accumulator	0011110w	data	data if w=1	
AAS = ASCII adjust for subtract	00111111			
DAS = Decimal adjust for subtract	00101111			
MUL = Multiply (unsigned)	1111011w	mod 100 r/m		
IMUL = Integer multiply (signed)	1111011w	mod 101 r/m		
AAM = ASCII adjust for multiply	11010100	00001010		
DIV = Divide (unsigned)	1111011w	mod 110 r/m		
IDIV = Integer divide (signed)	1111011w	mod 111 r/m		
AAD = ASCII adjust for divide	11010101	00001010		
CBW = Convert byte to word	10011000			
CWD = Convert word to double word	10011001			

Logic	76543210	76543210	76543210	76543210
NOT = Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL = Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR = Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR = Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL = Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR = Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL = Rotate through carry flag left	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR = Rotate through carry flag right	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w=1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w=1	
TEST = And function to flags, no result:				
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w=1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w=1	
OR = Or:				
Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w=1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w=1	
XOR = Exclusive Or:				
Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w=1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w=1	

String Manipulation	**76543210**	**76543210**	**76543210**
REP = Repeat	1111001z		
MOVS = Move byte/word	1010010w		
CMPS = Compare byte/word	1010011w		
SCAS = Scan byte/word	1010111w		
LODS = Load byte/word to AL/AX	1010110w		
STOS = Store byte/word from AL/A	1010101w		

Control Transfer

CALL = **Call:**

Direct within segment	11101000	disp-low	disp-high
Indirect within segment	11111111	mod 010 r/m	
Direct intersegment	10011010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 011 r/m	

JMP = **Unconditional jump:**

Direct within segment	11101001	disp-low	disp-high
Direct within segment short	11101011	disp	
Indirect within segment	11111111	mod 100 r/m	
Direct intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 101 r/m	

RET = Return from CALL:	**76543210**	**76543210**	**76543210**
Within segment	11000011		
Within seg. adding immediate to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment adding immediate to SP	11001010	data-low	data-high
JE/JZ = Jump on equal/zero	01110100	disp	
JL/JNGE = Jump on less/not greater or equal	01111100	disp	
JLE/JNG = Jump on less or equal/not greater	01111110	disp	
JB/JNAE = Jump on below/not above or equal	01110010	disp	
JBE/JNA = Jump on below or equal/ not above	01110110	disp	
JP/JPE = Jump on parity/parity even	01111010	disp	
JO = Jump on overflow	01110000	disp	
JS = Jump on sign	01111000	disp	
JNE/JNZ = Jump on not equal/not zero	01110101	disp	
JNL/JGE = Jump on not less/greater or equal	01111101	disp	
JNLE/JG = Jump on not less or equal/ greater	01111111	disp	
JNB/JAE = Jump on not below/above or equal	01110011	disp	
JNBE/JA = Jump on not below or equal/above	01110111	disp	
JNP/JPO = Jump on not parity/parity odd	01111011	disp	
JNO = Jump on not overflow	01110001	disp	
JNS = Jump on not sign	01111001	disp	
LOOP = Loop CX times	11100010	disp	
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp	
JCXZ = Jump on CX zero	11100011	disp	

INT = **Interrupt**	**76543210**	**76543210**
Type specified	11001101	type
Type 3	11001100	
INTO = Interrupt on overflow	11001110	
IRET = Interrupt return	11001111	

Processor Control

CLC = Clear carry	11111000	
CMC = Complement carry	11110101	
STC = Set carry	11111001	
CLD = Clear direction	11111100	
STD = Set direction	11111101	
CLI = Clear interrupt	11111010	
STI = Set interrupt	11111011	
HLT = Halt	11110100	
WAIT = Wait	10011011	
ESC = Escape (to external device)	11011xxx	mod x x x r/m
LOCK = Bus lock prefix	11110000	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction
if s:w = 01 then 16-bits of immediate data from the operand
it s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparsion with ZF FLAG

Segment Override Prefix

0 0 1 reg 1 1 0

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp high is absent
if mod = 10 then DISP = disp-high: disp low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) +DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

* except if mod = 00 and r/m = 110 then EA = disp-high:disp-low.

REG is assigned according to the following table

16-bit (w=1)	8-bit (w=0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instruction which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Absolute Maximum Ratings [1]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−1.0 to +7V
Power dissipation	2.5 W

DC Characteristics

SAB 8088: TA = 0 to 70°C, VCC = 5 V ±10%
SAB 8088-2: TA = 0 to 70°C, VCC = 5 V ± 5%
SAB 8088-1: TA = 0 to 70°C, VCC = 5 V ± 5%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
VIL	Input low voltage	−0.5	+0.8	V	[2]
VIH	Input high voltage	2.0	VCC+0.5	V	[2] [3]
VOL	Output low voltage	–	0.45	V	IOL = 2.0 mA
VOH	Output high voltage	2.4	–	V	IOH = −400 µA
ICC	Power supply current	–	340	mA	All outputs open TA = 25°C
ILI	Input leakage current	–	±10	µA	0V ≤ VIN ≤ VCC
ILO	Output leakage current	–	±10	µA	0.45 V ≤ VOUT ≤ VCC
VCL	Clock input low voltage	−0.5	+0.6	V	–
VCH	Clock input high voltage	3.9	VCC+1.0	V	–
CIN	Capacitance of input buffer (all inputs except AD0 to AD7, $\overline{RQ}/\overline{GT}$)	–	15	pF	fc = 1 MHz
CIO	Capacitance of I/O buffer (AD0 to AD7, $\overline{RQ}/\overline{GT}$)	–	15	pF	fc = 1 MHz

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] VIL tested with MN/$\overline{MX}$ in = 0 V
VIH tested with MN/$\overline{MX}$ in = 5 V
MN/$\overline{MX}$ pin is a strap pin.

[3] Not applicable to $\overline{RG}/\overline{GT0}$ and $\overline{RG}/\overline{GT1}$ pins (pin 30 and 31)

AC Characteristics for SAB 8088/8088-2

SAB 8088: TA = 0 to 70°C, VCC = 5 V ± 10%
SAB 8088-2: TA = 0 to 70°C, VCC = 5 V ± 5%

Minimum Complexity System Timing Requirements

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 8088		SAB 8088-2			
		min.	max.	min.	max.		
TCLCL	CLK cycle period	200	500	125	500	ns	–
TCLCH	CLK low time	118	–	68	–	ns	–
TCHCL	CLK high time	69	–	44	–	ns	–
TCH1CH2	CLK rise time	–	10	–	10	ns	from 1.0 to 3.5V
TCL2CL1	CLK fall time	–	10	–	10	ns	from 3.5 to 1.0V
TDVCL	Data in setup time	30	–	20	–	ns	–
TCLDX	Data in hold time	10	–	10	–	ns	–
TR1VCL	RDY setup time into SAB 8284A/8284B [1] [2]	35	–	35	–	ns	–
TCLR1X	RDY hold time into SAB 8284A/8284B [1] [2]	0	–	0	–	ns	–
TRYHCH	READY setup time into SAB 8088	118	–	68	–	ns	–
TCHRYX	READY hold time into SAB 8088	30	–	20	–	ns	–
TRYLCL	READY inactive to CLK [3]	−8	–	−8	–	ns	–
THVCH	HOLD setup time	35	–	20	–	ns	–
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ setup time [2]	30	–	15	–	ns	–
TILIH	Input rise time (except CLK)	–	20	–	20	ns	from 0.8 to 2.0V
TIHIL	Input fall time (except CLK)	–	12	–	12	ns	from 2.0 to 0.8V

[1]) Signal at SAB 8284A/8284B shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T2 state (8 ns into T3).

Timing Responses

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 8088		SAB 8088-2			
		min.	max.	min.	max.		
TCLAV	Address valid delay	10	110	10	60	ns	[1]
TCLAX	Address hold time	10	–	10	–	ns	[1]
TCLAZ	Address float delay	TCLAX	80	TCLAX	50	ns	[1]
TLHLL	ALE width	TCLCH–20	–	TCLCH–10	–	ns	[1]
TCLLH	ALE active delay	–	80	–	50	ns	[1]
TCHLL	ALE inactive delay	–	85	–	55	ns	[1]
TLLAX	Address hold time to ALE inactive	TCHCL–10	–	TCHCL–10	–	ns	[1]
TCLDV	Data valid delay	10	110	10	60	ns	[1]
TCHDX	Data hold time	10	–	10	–	ns	[1]
TWHDX	Data hold time after $\overline{WR}$	TCLCH–30	–	TCLCH–30	–	ns	[1]
TCVCTV	Control active delay 1	10	110	10	70	ns	[1]
TCHCTV	Control active delay 2	10	110	10	60	ns	[1]
TCVCTX	Control inactive delay	10	110	10	70	ns	[1]
TAZRL	Address float to READ active	0	–	0	–	ns	[1]
TCLRL	$\overline{RD}$ active delay	10	165	10	100	ns	[1]
TCLRH	$\overline{RD}$ inactive delay	10	150	10	80	ns	[1]
TRHAV	$\overline{RD}$ inactive to next address active	TCLCL–45	–	TCLCL–40	–	ns	[1]
TCLHAV	HLDA valid delay	10	160	10	100	ns	[1]
TRLRH	$\overline{RD}$ width	2TCLCL–75	–	2TCLCL–50	–	ns	[1]
TWLWH	$\overline{WR}$ width	2TCLCL–60	–	2TCLCL–40	–	ns	[1]
TAVAL	Address valid to ALE low	TCLCH–60	–	TCLCH–40	–	ns	[1]
TOLOH	Output rise time	–	20	–	20	ns	from 0.8 to 2.0V
TOHOL	Output fall time	–	12	–	12	ns	from 2.0 to 0.8V

[1]) CL = 20–100 pF for all SAB 8088 outputs in addition to the internal loads

Maximum Mode System (using SAB 8288/8288A bus controller)
Timing Requirements

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 8088		SAB 8088-2			
		min.	max.	min.	max.		
TCLCL	CLK cycle period	200	500	125	500	ns	–
TCLCH	CLK low time	118	–	68	–	ns	–
TCHCL	CLK high time	69	–	44	–	ns	–
TCH1CH2	CLK rise time	–	10	–	10	ns	from 1.0 to 3.5V
TCL2CL1	CLK fall time	–	10	–	10	ns	from 3.5 to 1.0V
TDVCL	Data in setup time	30	–	20	–	ns	–
TCLDX	Data in hold time	10	–	10	–	ns	–
TR1VCL	RDY setup time into SAB 8284A/8284B [1] [2]	35	–	35	–	ns	–
TCLR1X	RDY hold time into SAB 8284A/8284B [1] [2]	0	–	0	–	ns	–
TRYHCH	READY setup time into SAB 8088	118	–	68	–	ns	–
TCHRYX	READY hold time into SAB 8088	30	–	20	–	ns	–
TRYLCL	READY inactive to CLK [3]	−8	–	−8	–	ns	–
TINVCH	Setup time for recognition (INTR, NMI, $\overline{\text{TEST}}$) [2]	30	–	15	–	ns	–
TGVCH	$\overline{\text{RQ}}/\overline{\text{GT}}$ setup time	30	–	15	–	ns	–
TCHGX	$\overline{\text{RQ}}$ hold time into SAB 8088	40	–	30	–	ns	–
TILIH	Input rise time (except CLK)	–	20	–	20	ns	from 0.8 to 2.0V
TIHIL	Input fall time (except CLK)	–	12	–	12	ns	from 2.0 to 0.8V

[1]) Signal at SAB 8284A/8284B or SAB 8288/8288A shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T2 state (8 ns into T3).

Timing Responses

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 8088		SAB 8088-2			
		min.	max.	min.	max.		
TCLML	Command Active Delay [1])	10	35	10	35	ns	[3]
TCLMH	Command Inactive Delay [1])	10	35	10	35	ns	[3]
TRYHSH	READY Active to status passive [2])	–	110	–	65	ns	[3]
TCHSV	Status active delay	10	110	10	60	ns	[3]
TCLSH	Status inactive delay	10	130	10	70	ns	[3]
TCLAV	Address valid delay	10	110	10	60	ns	[3]
TCLAX	Address hold time	10	–	10	–	ns	[3]
TCLAZ	Address float delay	TCLAX	80	TCLAX	50	ns	[3]
TSVLH	Status valid to ALE high [1])	–	20	–	20	ns	[3]
TSVMCH	Status valid to MCE high [1])	–	20	–	20	ns	[3]
TCLLH	CLK low to ALE valid [1])	–	20	–	20	ns	[3]
TCLMCH	CLK low to MCE high [1])	–	20	–	20	ns	[3]
TCHLL	ALE inactive delay [1])	4	15	4	15	ns	[3]
TCLDV	Data valid delay	10	110	10	60	ns	[3]
TCHDX	Data hold time	10	–	10	–	ns	[3]
TCVNV	Control active delay [1])	5	45	5	45	ns	[3]
TCVNX	Control inactive delay [1])	10	45	10	45	ns	[3]

[1]) Signal at SAB 8284A/8284B or SAB 8288/8288A shown for reference only.
[2]) Applies only to T2 state (8 ns into T3).
[3]) CL = 20–100 pF for all SAB 8088 outputs in addition to the internal loads.

Timing Responses (cont'd)

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 8088		SAB 8088-2			
		min.	max.	min.	max.		
TAZRL	Address float to READ active	0	–	0	–	ns	[2]
TCLRL	$\overline{RD}$ active delay	10	165	10	100	ns	[2]
TCLRH	$\overline{RD}$ inactive delay	10	150	10	80	ns	[2]
TRHAV	$\overline{RD}$ inactive to next address active	TCLCL–45	–	TCLCL–40	–	ns	[2]
TCHDTL	Direction control active delay [1]	–	50	–	50	ns	[2]
TCHDTH	Direction control inactive delay [1]	–	30	–	30	ns	[2]
TCLGL	$\overline{GT}$ active delay	–	85	–	50	ns	[2]
TCLGH	$\overline{GT}$ inactive delay	–	85	–	50	ns	[2]
TRLRH	$\overline{RD}$ width	2TCLCL–75	–	2TCLCL–50	–	ns	[2]
TOLOH	Output rise time	–	20	–	20	ns	from 0.8 to 2.0V
TOHOL	Output fall time	–	12	–	12	ns	from 2.0 to 0.8V

[1]) Signal at SAB 8284A/8284B or SAB 8288/8288A shown for reference only.
[2]) CL = 20–100 pF for all SAB 8088 outputs in addition to the internal loads.

AC Characteristics for SAB 8088-1

SAB 8088-1: TA = 0 to 70°C, VCC = 5 V ± 5%

Minimum Complexity System Timing Requirements

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCLCL	CLK cycle period	100	500	ns	–
TCLCH	CLK low time	53	–	ns	–
TCHCL	CLK high time	39	–	ns	–
TCH1CH2	CLK rise time	–	10	ns	from 1.0 to 3.5V
TCL2CL1	CLK fall time	–	10	ns	from 3.5 to 1.0V
TDVCL	Data in setup time	5	–	ns	–
TCLDX	Data in hold time	10	–	ns	–
TR1VCL	RDY setup time into SAB 8284A/8284B [1] [2]	35	–	ns	–
TCLR1X	RDY hold time into SAB 8284A/8284B [1] [2]	0	–	ns	–
TRYHCH	READY setup time into SAB 8088	53	–	ns	–
TCHRYX	READY hold time into SAB 8088	20	–	ns	–
TRYLCL	READY inactive to CLK [3]	−10	–	ns	–
THVCH	HOLD setup time	20	–	ns	–
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ setup time [2]	15	–	ns	–
TILIH	Input rise time (except CLK)	–	20	ns	from 0.8 to 2.0V
TIHIL	Input fall time (except CLK)	–	12	ns	from 2.0 to 0.8V

[1] Signal at SAB 8284A/8284B shown for reference only.
[2] Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3] Applies only to T2 state (8 ns into T3).

Timing Responses

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCLAV	Address valid delay	10	50	ns	[1]
TCLAX	Address hold time	10	–	ns	[1]
TCLAZ	Address float delay	10	40	ns	[1]
TLHLL	ALE width	TCLCH–10	–	ns	[1]
TCLLH	ALE active delay	–	40	ns	[1]
TCHLL	ALE inactive delay	–	45	ns	[1]
TLLAX	Address hold time to ALE inactive	TCHCL–10	–	ns	[1]
TCLDV	Data valid delay	10	50	ns	[1]
TCHDX	Data hold time	10	–	ns	[1]
TWHDX	Data hold time after $\overline{WR}$	TCLCH–25	–	ns	[1]
TCVCTV	Control active delay 1	10	50	ns	[1]
TCHCTV	Control active delay 2	10	45	ns	[1]
TCVCTX	Control inactive delay	10	50	ns	[1]
TAZRL	Address float to READ active	0	–	ns	[1]
TCLRL	$\overline{RD}$ active delay	10	70	ns	[1]
TCLRH	$\overline{RD}$ inactive delay	10	60	ns	[1]
TRHAV	$\overline{RD}$ inactive to next address active	TCLCL–35	–	ns	[1]
TCLHAV	HLDA valid delay	10	60	ns	[1]
TRLRH	$\overline{RD}$ width	2TCLCL–40	–	ns	[1]
TWLWH	$\overline{WR}$ width	2TCLCL–35	–	ns	[1]
TAVAL	Address valid to ALE low	TCLCH–35	–	ns	[1]
TOLOH	Output rise time	–	20	ns	from 0.8 to 2.0V
TOHOL	Output fall time	–	12	ns	from 2.0 to 0.8V

[1]) CL = 20–100 pF for all SAB 8088 outputs in addition to the internal loads.

Maximum Mode System (using SAB 8288/8288A bus controller)
Timing Requirements

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCLCL	CLK cycle period	100	500	ns	–
TCLCH	CLK low time	53	–	ns	–
TCHCL	CLK high time	39	–	ns	–
TCH1CH2	CLK rise time	–	10	ns	from 1.0 to 3.5V
TCL2CL1	CLK fall time	–	10	ns	from 3.5 to 1.0V
TDVCL	Data in setup time	5	–	ns	–
TCLDX	Data in hold time	10	–	ns	–
TR1VCL	RDY setup time into SAB 8284A/8284B [1] [2]	35	–	ns	–
TCLR1X	RDY hold time into SAB 8284A/8284B [1] [2]	0	–	ns	–
TRYHCH	READY setup time into SAB 8088	53	–	ns	–
TCHRYX	READY hold time into SAB 8088	20	–	ns	–
TRYLCL	READY inactive to CLK [3]	−10	–	ns	–
TINVCH	Setup time for recognition (INTR, NMI, $\overline{\text{TEST}}$) [2]	15	–	ns	–
TGVCH	$\overline{\text{RQ}}/\overline{\text{GT}}$ setup time	12	–	ns	–
TCHGX	$\overline{\text{RQ}}$ hold time into SAB 8088	20	–	ns	–
TILIH	Input rise time (except CLK)	–	20	ns	from 0.8 to 2.0V
TIHIL	Input fall time (except CLK)	–	12	ns	from 2.0 to 0.8V

[1]) Signal at SAB 8284A/8284B or SAB 8288/8288A shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T2 state (8 ns into T3).

Timing Responses

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCLML	Command active delay [1])	10	35	ns	[3]
TCLMH	Command inactive delay [1])	10	35	ns	[3]
TRYHSH	READY active to status passive [2])	–	45	ns	[3]
TCHSV	Status active delay	10	45	ns	[3]
TCLSH	Status inactive delay	10	55	ns	[3]
TCLAV	Address valid delay	10	50	ns	[3]
TCLAX	Address hold time	10	–	ns	[3]
TCLAZ	Address float delay	10	40	ns	[3]
TSVLH	Status valid to ALE high [1])	–	20	ns	[3]
TSVMCH	Status valid to MCE high [1])	–	20	ns	[3]
TCLLH	CLK low to ALE valid [1])	–	20	ns	[3]
TCLMCH	CLK low to MCE high [1])	–	20	ns	[3]
TCHLL	ALE inactive delay [1])	4	15	ns	[3]
TCLDV	Data valid delay	10	50	ns	[3]
TCHDX	Data hold time	10	–	ns	[3]
TCVNV	Control active delay [1])	5	45	ns	[3]
TCVNX	Control inactive delay [1])	10	45	ns	[3]

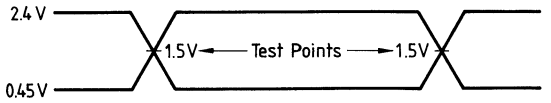
[1]) Signal at SAB 8284A/8284B or SAB 8288/8288A shown for reference only.
[2]) Applies only to T2 state (8 ns into T3).
[3]) CL = 20–100 pF for all SAB 8088 outputs in addition to the internal loads.

Timing Responses (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TAZRL	Address float to READ active	0	–	ns	[2]
TCLRL	$\overline{RD}$ active delay	10	70	ns	[2]
TCLRH	$\overline{RD}$ inactive delay	10	60	ns	[2]
TRHAV	$\overline{RD}$ inactive to next address active	TCLCL–35	–	ns	[2]
TCHDTL	Direction control active delay [1]	–	50	ns	[2]
TCHDTH	Direction control inactive delay [1]	–	30	ns	[2]
TCLGL	$\overline{GT}$ active delay	0	45	ns	[2]
TCLGH	$\overline{GT}$ inactive delay	0	45	ns	[2]
TRLRH	$\overline{RD}$ width	2TCLCL–40	–	ns	[2]
TOLOH	Output rise time	–	20	ns	from 0.8 to 2.0V
TOHOL	Output fall time	–	12	ns	from 2.0 to 0.8V

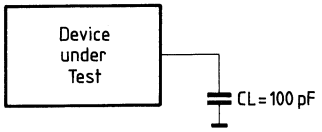
[1] Signal at SAB 8284A/8284B or SAB 8288/8288A shown for reference only.
[2] CL = 20–100 pF for all SAB 8088 outputs in addition to the internal loads.

Input/Output Waveforms for AC Tests



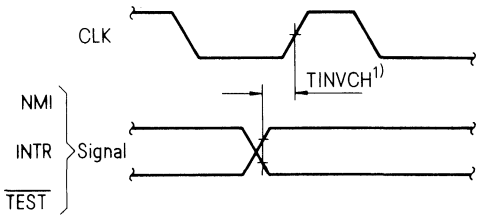
AC Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". The clock is driven at 4.3V and 0.25V. Timing measurements are made at 1.5V for both a logic "1" and "0".

Load Circuit for AC Tests



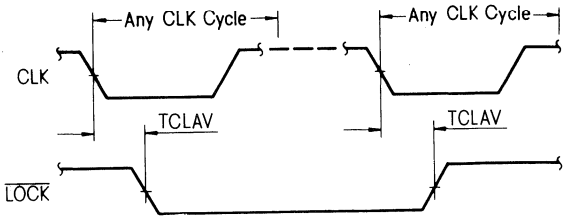
CL includes Jig Capacitance

Asynchronous Signal Recognition

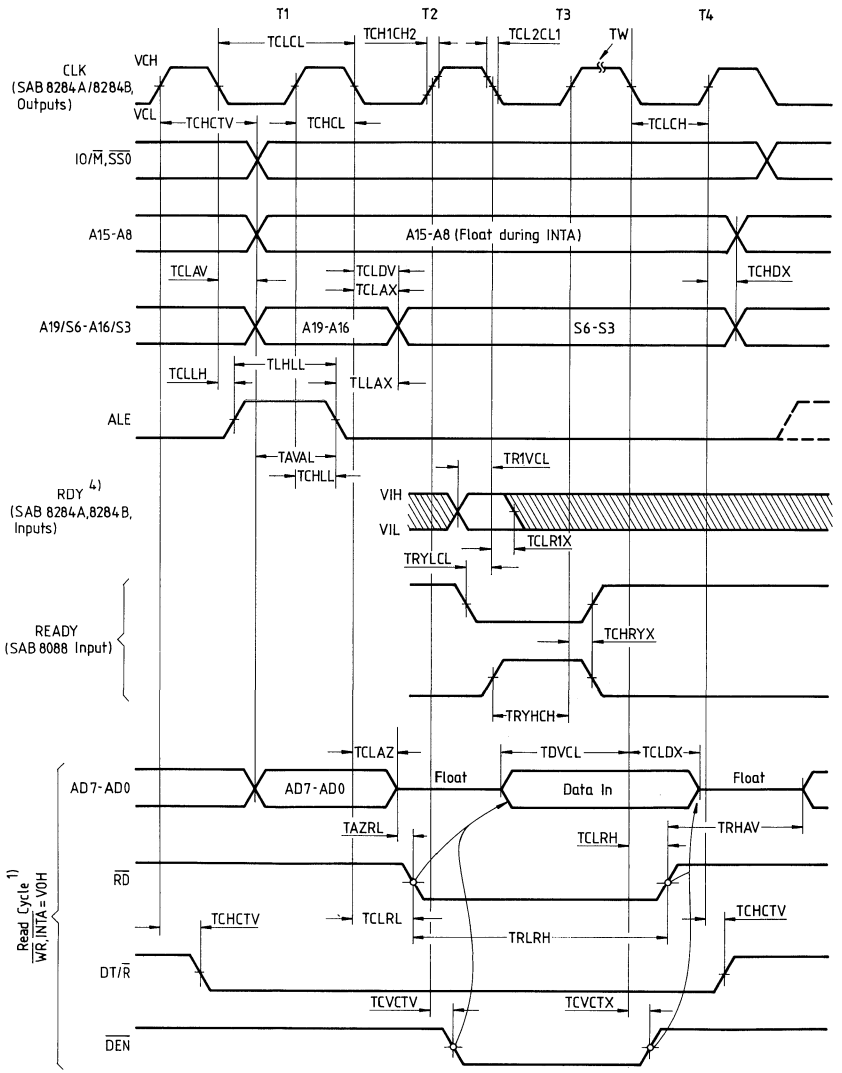


1) Setup requirements for asynchronous signals only to guarantee recognition at next CLK

Bus Lock Signal Timing (maximum mode only)

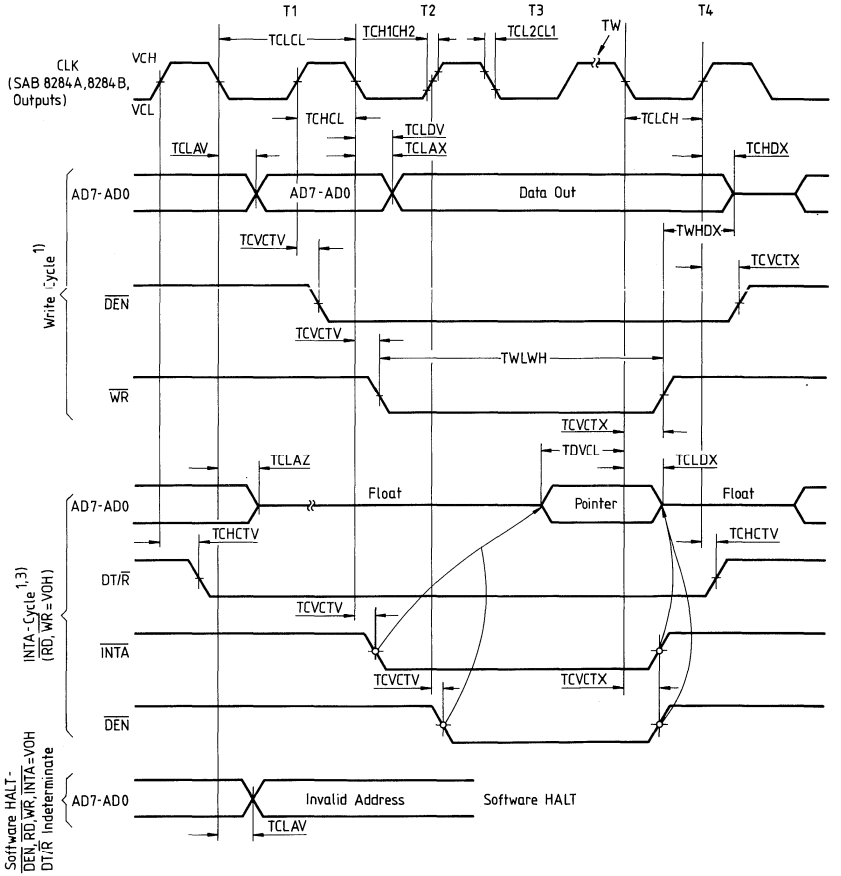


Bus Timing – Minimum Mode System



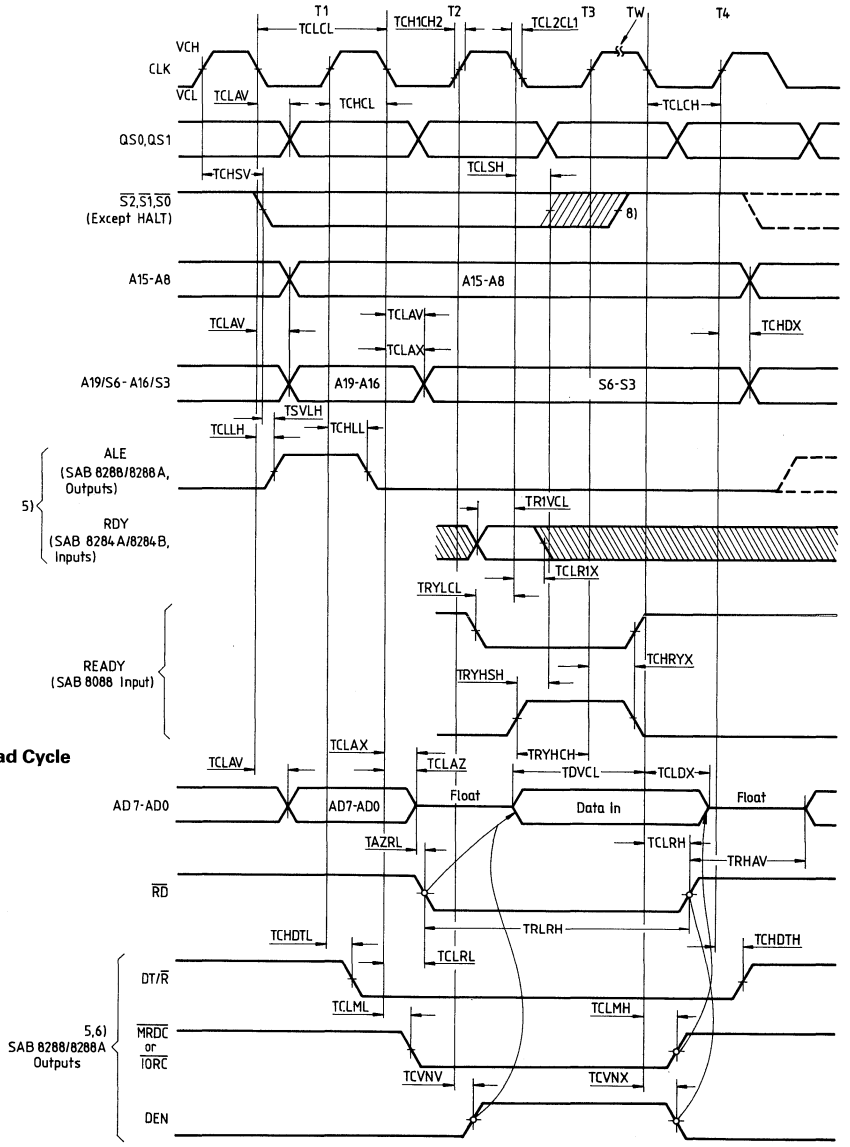
Notes see next page

Bus Timing — Minimum Mode System (cont'd)



[1]) All signals switch between VOH and VOL unless otherwise specified.
[2]) RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
[3]) Two INTA cycles run back to back. The SAB 8088 local ADDR/DATA bus is floating during both INTA cycles. Control signals shown for second INTA cycle.
[4]) Signals at SAB 8284A/8284B are shown for reference only.
[5]) All timing measurements are made at 1.5V unless otherwise noted.

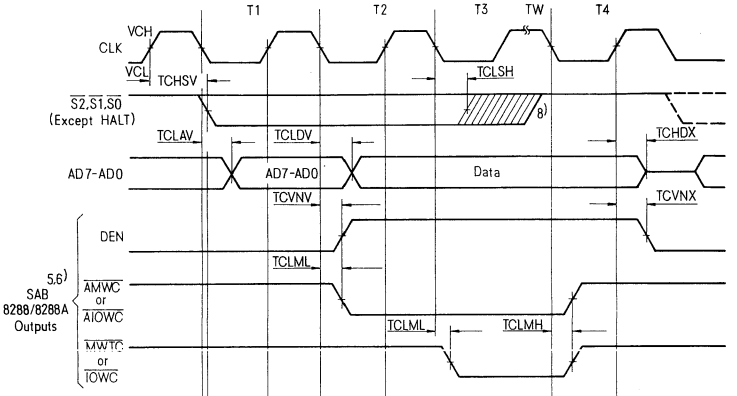
Bus Timing – Maximum Mode System (using SAB 8288/8288A)



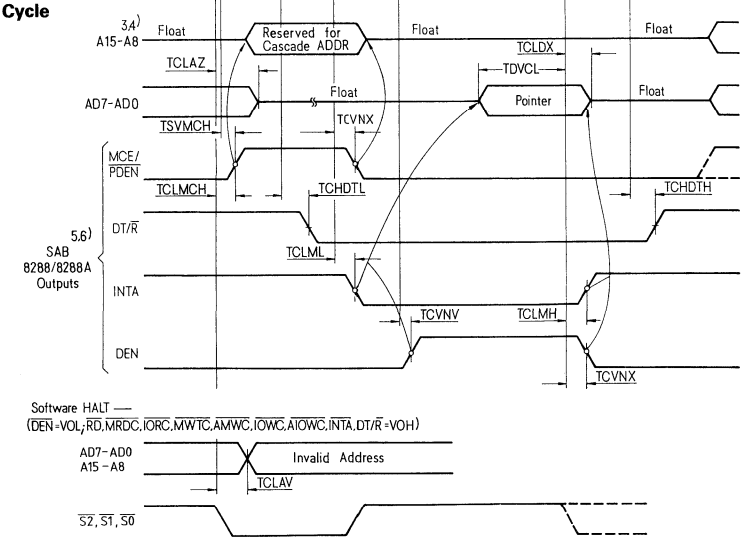
Notes see next page.

Bus Timing – Maximum Mode System (using SAB 8288/8288A)

Write Cycle

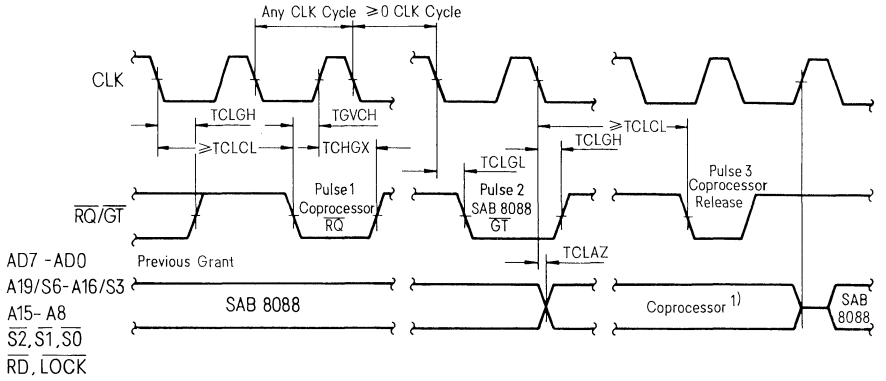


INTA Cycle



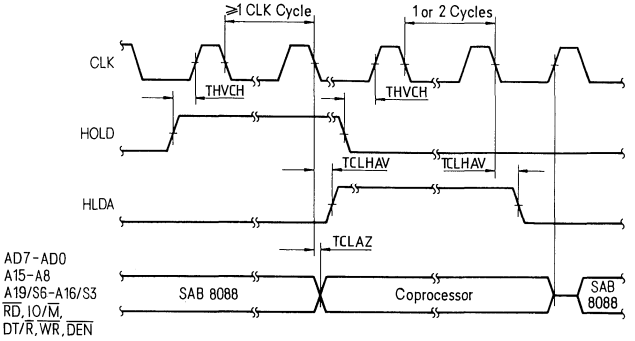
1) All signals switch between VOH and VOL unless otherwise specified.
2) RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3) Cascade address is valid between first and second INTA cycle.
4) Two INTA cycles run back-to-back. The SAB 8088 local ADDR/DATA bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5) Signals at SAB 8284A/8284B or SAB 8288/8288A are shown for reference only.
6) The issuance of the SAB 8288/8288A command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ and DEN) lags the active high SAB 8288/8288A DEN.
7) All timing measurements are made at 1.5 V unless otherwise noted.
8) Status inactive in state just prior to T4.

Request/Grant Sequence Timing (maximum mode only)



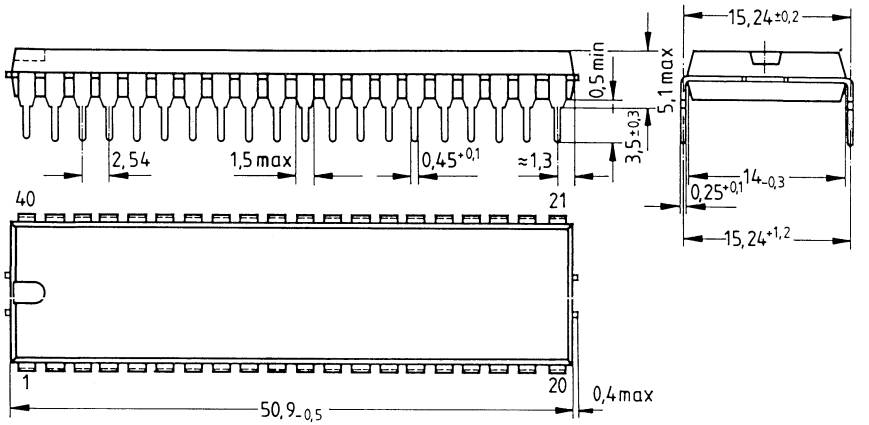
[1]) The coprocessor may not drive the buses outside the region shown without risking contention

Hold/Hold Acknowledge Timing (minimum mode only)



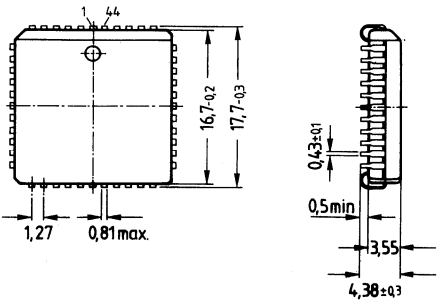
Package Outlines

Plastic Package, P-DIP, 40 Pins



Dimensions in mm

Plastic Package, PLCC, 44 Pins



Dimensions in mm

Ordering Information

Type	Ordering code	Function
SAB 8088-P	Q67120-C106	8-bit microprocessor – 5 MHz (P-DIP40)
SAB 8088-2-P	Q67120-C213	8-bit microprocessor – 8 MHz (P-DIP40)
SAB 8088-1-P	Q67120-C249	8-bit microprocessor – 10 MHz (P-DIP40)
SAB 8088-N	Q67120-C301	8-bit microprocessor – 5 MHz (PLCC44)
SAB 8088-2-N	Q67120-C302	8-bit microprocessor – 8 MHz (PLCC44)

SAB 80188/80188-1 High-Integration 8-Bit Microprocessor

Preliminary

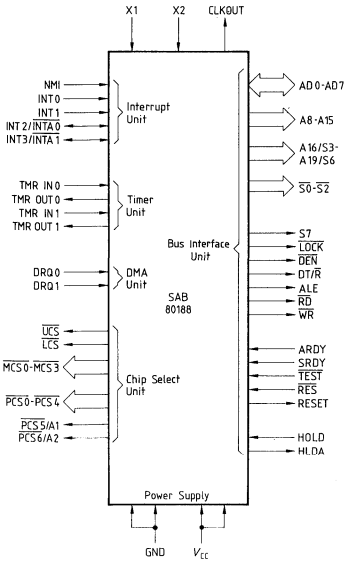
SAB 80188 8 MHz

- Integrated feature set
  - enhanced SAB 8088-2 CPU
  - clock generator
  - 2 independent high-speed DMA channels
  - programmable interrupt controller
  - 3 programmable 16-bit timers
  - programmable memory and peripheral chip-select logic
  - programmable wait state generator
  - local bus controller
- High-performance processor
  - twice the performance of the standard SAB 8088 at 8 MHz
  - 2 Mbyte/s bus bandwidth interface at 8 MHz

SAB 80188-1 10 MHz

- Direct addressing capability to 1 Mbyte of memory
- Completely object-code compatible with all existing SAB 8086/8088 software
  - 10 new instruction types
- Optional numerical processor extension
- Compatible with the bus support components SAB 8282A/8283A/8286A/8287A and SAB 8288A/8289
- Compatible with industry standard 80188 processor
- Available in 10 MHz (SAB 80188-1) and 8 MHz (SAB 80188) versions

Logic Symbol



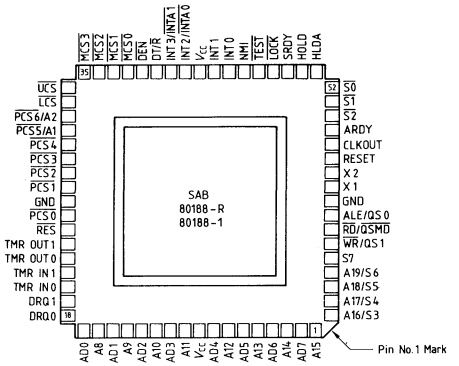
Pin Names

AD0–AD7	Address/Data Bus
A8–A15	Address Bus
A16/S3–A19/S6	Address Bus/Status Lines
S0–S2	Status Lines
S7	Status Line
LOCK	Bus Lock
DEN	Data Enable
DT/R	Data Transmit/Receive
ALE/QS0	Address Latch Enable/Queue Status
RD/QSMD	Read Strobe/Queue Status Mode
WR/QS1	Write Strobe/Queue Status
ARDY	Asynchronous Ready
SRDY	Synchronous Ready
TEST	Test Line
RES	Reset Input
RESET	Reset Output
HOLD	Hold Request
HLDA	Hold Acknowledge
NMI	Non-Maskable Interrupt
INT0, INT1	Interrupt Request
INT2/INTA0	Interrupt Request/Acknowledge
INT3/INTA1	Interrupt Request/Acknowledge
TMR IN0/TMR OUT0	Timer 0 Input/Output
TMR IN1/TMR OUT1	Timer 1 Input/Output
DRQ0, DRQ1	Data Request
UCS, LCS	Upper/Lower Chip Select
MCS0–MCS3	Memory Chip Select
PCS0–PCS4	Peripheral Chip Select
PCS5/A1, PCS6/A2	Peripheral Chip Select/Address
V_{CC}	Power Supply (+5 V)
GND	Ground (0 V)

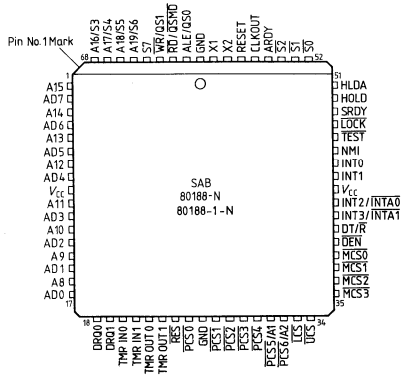
The SAB 80188 is a highly integrated 8-bit microprocessor implemented in +5 V advanced Siemens MYMOS technology. It effectively combines 15 to 20 of the most common SAB 8088 system components onto one chip. The 8 MHz SAB 80188 provides twice the throughput of the standard 5 MHz SAB 8088. The SAB 80188 is upward-compatible with SAB 8086 and SAB 8088 software, and adds 10 new instruction types to the existing set. The SAB 80188 comes in a 68-pin packages and requires single +5 V power supply.

Pin Configuration

LCC Package
Component pad view – as viewed from underside of component when mounted on the board.



Leaded Chip Carrier Package (top view)



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
AD7–AD0	2, 4, 6, 8, 11, 13, 15, 17	I/O	ADDRESS/DATA BUS (0 TO 7) These signals constitute the time-multiplexed memory or I/O address (T1) and data (T2, T3, TW, and T4) bus. The bus is active high.
A15–A8	1, 3, 5, 7 10, 12, 14, 16	O	ADDRESS BUS (8 TO 15) Contains valid address from T1 to T4. The bus is active high.
DRQ0 DRQ1	18 19	I I	DMA REQUEST Is driven high by an external device when it desires that a DMA channel (channel 0 or 1) performs a transfer. These signals are active high, level-triggered, and internally synchronized.
TMR IN 0, TMR IN 1	20 21	I I	TIMER INPUTS Are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active high (or low-to-high transitions are counted) and internally synchronized.
TMR OUT 0, TMR OUT 1	22 23	O O	TIMER OUTPUTS Are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected.
$\overline{RES}$	24	I	$\overline{SYSTEM\ RESET}$ Causes the SAB 80188 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the SAB 80188 clock. The SAB 80188 begins fetching instructions approximately 7 clock cycles after $\overline{RES}$ is returned high. $\overline{RES}$ is required to be low for greater than 4 clock cycles and is internally synchronized. For proper initialization, the low-to-high transition of $\overline{RES}$ must occur no sooner than 50 microseconds after power up. This input is provided with a Schmitt trigger to facilitate power-on $\overline{RES}$ generation via an RC network. When $\overline{RES}$ occurs, the SAB 80188 will drive the status lines to an inactive level for one clock, and then tristate them.
$\overline{PCS0}$ $\overline{PCS1-4}$	25 27, 28, 29, 30	O O	$\overline{PERIPHERAL\ CHIP\ SELECT\ 0\ TO\ 4}$ These signals are active low when a reference is made to the defined peripheral area (64 Kbyte I/O space). These lines are not tristated during bus hold. The address ranges activating $\overline{PCS0-4}$ are software-programmable.
$\overline{PCS5}$/A1	31	O	$\overline{PERIPHERAL\ CHIP\ SELECT\ 5}$/LATCHED A1 May be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software-programmable. When programmed to provide latched A1, rather than $\overline{PCS5}$, this pin will retain the previously latched value of A1 during a bus HOLD. A1 is active high.
$\overline{PCS6}$/A2	32	O	$\overline{PERIPHERAL\ CHIP\ SELECT\ 6}$/LATCHED A2 May be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software-programmable. When programmed to provide latched A2, rather than $\overline{PCS6}$, this pin will retain the previously latched value of A2 during a bus HOLD. A2 is active high.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{LCS}$	33	O	$\overline{LOWER\ MEMORY\ CHIP\ SELECT}$ Is active low whenever a memory reference is made to the defined lower portion (1 K to 256 K) of memory. This line is not tristated during bus HOLD. The address range activating $\overline{LCS}$ is software-programmable.
$\overline{UCS}$	34	O	$\overline{UPPER\ MEMORY\ CHIP\ SELECT}$ Is an active low output whenever a memory reference is made to the defined upper portion (1 K to 256 K block) of memory. This line is not tristated during bus HOLD. The address range activating $\overline{UCS}$ is software-programmable.
$\overline{MCS0-3}$	38, 37, 36, 35	O	$\overline{MIDRANGE\ MEMORY\ CHIP\ SELECT\ 0\ TO\ 3}$ These signals are active low when a memory reference is made to the defined midrange portion of memory (8 K to 512 K). These lines are not tristated during bus HOLD. The address ranges activating $\overline{MCS0-3}$ are software-programmable.
$\overline{DEN}$	39	O	$\overline{DATA\ ENABLE}$ Is provided as an SAB 8286A/8287A data bus transceiver output enable. $\overline{DEN}$ is active low during each memory and I/O access. $\overline{DEN}$ is high whenever DT/$\overline{R}$ changes its state.
DT/$\overline{R}$	40	O	DATA TRANSMIT/$\overline{RECEIVE}$ Controls the direction of data flow through the external SAB 8286A/8287A data bus transceiver. When low data is transferred to the SAB 80188. When high the SAB 80188 places write data on the data bus.
INT0, INT1, INT2/$\overline{INTA0}$ INT3/$\overline{INTA1}$	45, 44 42 41	I I/O I/O	MASKABLE INTERRUPT REQUEST Can be requested by strobing one of these pins. When configured as inputs, these pins are active high. Interrupt requests are synchronized internally. INT2 and INT3 may be configured via software to provide active low interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When iRMX mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).
NMI	46	I	NON-MASKABLE INTERRUPT Is an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from low to high initiates the interrupt at the next instruction boundary. NMI is latched internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized.
$\overline{TEST}$	47	I	$\overline{TEST}$ Is examined by the WAIT instruction. If the $\overline{TEST}$ input is high when "WAIT" execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled until it goes low, at which time execution will be resumed. If interrupts are enabled while the SAB 80188 is waiting for $\overline{TEST}$, interrupts will be serviced. This input is synchronized internally.

Pin Definitions and Functions (cont'd)

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{\text{LOCK}}$</td><td>48</td><td>O</td><td>$\overline{\text{LOCK}}$
This output indicates that other system bus masters are not to gain control of the system bus while $\overline{\text{LOCK}}$ is active low. The $\overline{\text{LOCK}}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the $\overline{\text{LOCK}}$ prefix. It remains active until the completion of the instruction following the $\overline{\text{LOCK}}$ prefix. No prefetches will occur while $\overline{\text{LOCK}}$ is asserted. $\overline{\text{LOCK}}$ is active low, is driven high for one clock during reset, and then tristated.</td></tr>
<tr><td>SRDY</td><td>49</td><td>I</td><td>SYNCHRONOUS READY
Must be synchronized externally to the SAB 80188. The use of SRDY provides a relaxed system-timing specification on the ready input. This is accomplished by eliminating the one-half clock cycle which is required for internally resolving the signal level when using the ARDY input. This line is active high. If this line is connected to V_{CC} no wait states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active before a bus cycle is terminated. If unused, this line should be tied low.</td></tr>
<tr><td>HOLD
HLDA</td><td>50
51</td><td>I
O</td><td>HOLD/HOLD ACKNOWLEDGE
Indicates that another bus master is requesting the local bus. The HOLD input is active high. HOLD may be asynchronous with respect to the SAB 80188 clock. The SAB 80188 will issue a HLDA (high) in response to a HOLD request at the end of T4 or T1. Simultaneous with issuing HLDA, the SAB 80188 will tristate the local bus and control lines. After HOLD is detected as being low, the SAB 80188 will lower HLDA. When the SAB 80188 needs to run another bus cycle, it will again drive the local bus and control lines.</td></tr>
<tr><td>$\overline{\text{S0}}$, $\overline{\text{S1}}$, $\overline{\text{S2}}$</td><td>52–54</td><td>O</td><td>$\overline{\text{BUS CYCLE STATUS}}$
$\overline{\text{S0}}$ to $\overline{\text{S2}}$ are encoded to provide bus transaction information:
SAB 80188 Bus Cycle Status Information
<table>
<tr><th>$\overline{\text{S2}}$</th><th>$\overline{\text{S1}}$</th><th>$\overline{\text{S0}}$</th><th>Bus Cycle Initiated</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction Fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Data from Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Data to Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive (no bus cycle)</td></tr>
</table>
The status pins are tristated during "HOLD."
$\overline{\text{S2}}$ may be used as a logical M/$\overline{\text{IO}}$ indicator, and $\overline{\text{S1}}$ as a DT/$\overline{\text{R}}$ indicator.
The status lines are driven high for one clock during reset, and then tristated until a bus cycle begins.</td></tr>
</table>

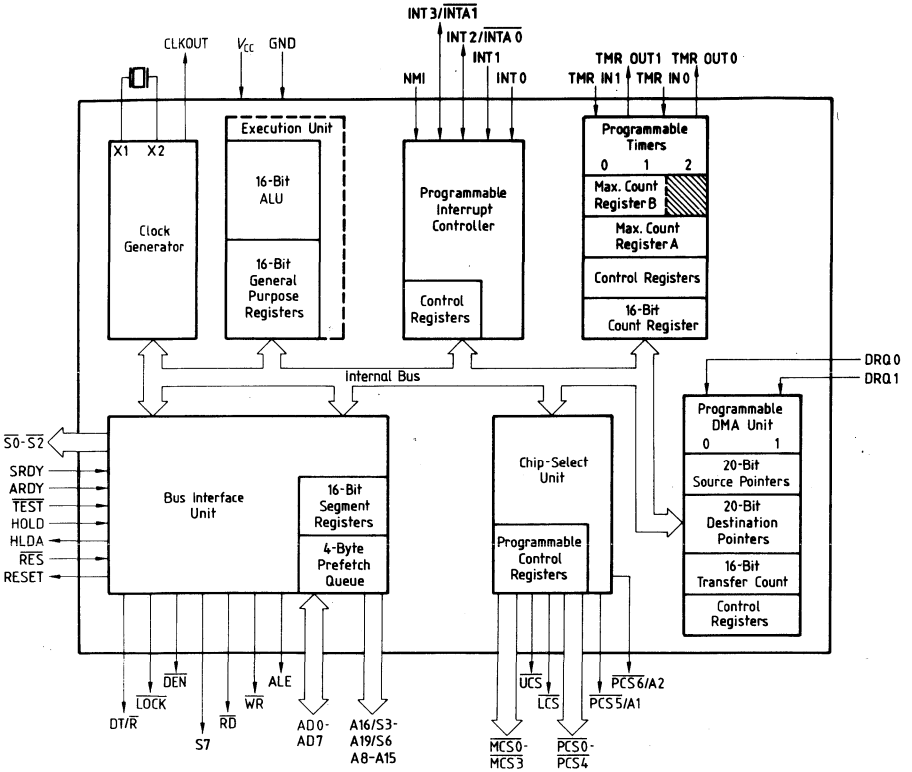
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
ARDY	55	I	ASYNCHRONOUS READY Informs the SAB 80188 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input and is active high. Only the rising edge is internally synchronized by the SAB 80188. This means that the falling edge of ARDY must be synchronized to the SAB 80188 clock. If connected to V_{CC} no wait states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active to terminate a bus cycle. If unused, this line should be tied low.
CLKOUT	56	O	CLOCK OUTPUT Provides the system with a 50% duty cycle waveform. All device pin timings are specified relative in CLKOUT.
RESET	57	O	RESET This output indicates that the SAB 80188 CPU is being reset, and can be used as a system reset. It is active high, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal.
X1, X2	59, 58	I	CRYSTAL INPUTS X1 and X2 provide an external connection for a fundamental-mode parallel resonant crystal for the internal crystal oscillator. X1 can interface to an external clock instead of a crystal. In this case, minimize the capacitance on X2 or drive X2 with complemented X1. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
ALE/QS0	61	O	ADDRESS LATCH ENABLE/QUEUE STATUS 0 Is provided by the SAB 80188 to latch the address into the SAB 8282A/8283A address latches. ALE is active high. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T1 of the associated bus cycle, effectively half a clock cycle earlier than in the standard SAB 8088. The trailling edge is generated off the CLKOUT rising edge in T1 like in the SAB 8088. Note that ALE is never tristated.
$\overline{RD}$/QSMD	62	O	$\overline{READY}$ STROBE Indicates that the SAB 80188 is performing a memory or I/O read cycle. $\overline{RD}$ is active low for T2, T3 and TW of any read cycle. It is guaranteed not to go low in T2 until after the address bus is tristated. $\overline{RD}$ is active low and tristated during "HOLD". $\overline{RD}$ is driven high for one clock during reset, and then the output driver is tristated. A weak internal pullup mechanism on the $\overline{RD}$ line holds it high when the line is not driven. During reset, the pin is sampled to determine whether the SAB 80188 should provide ALE, $\overline{WR}$ and $\overline{RD}$, or if the queue status should be provided. $\overline{RD}$ should be connected to GND to provide queue status data.

Pin Definitions and Functions (cont'd)

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{WR}$/QS1</td><td>63</td><td>O</td><td>$\overline{WRITE\ STROBE}$/QUEUE STATUS 1
Indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T2, T3, and TW of any write cycle. It is active low and tristated during "HOLD." It is driven high for one clock during reset, and then tristated. When the SAB 80188 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.
<table>
<tr><th>QS1</th><th>QS0</th><th>Queue Operation</th></tr>
<tr><td>0</td><td>0</td><td>No Queue Operation</td></tr>
<tr><td>0</td><td>1</td><td>First Op Code Byte Fetched from the Queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent Byte Fetched from the Queue</td></tr>
<tr><td>1</td><td>0</td><td>Empty the Queue</td></tr>
</table></td></tr>
<tr><td>S7</td><td>64</td><td>O</td><td>STATUS LINE 7
This signal is always high to indicate that the SAB 80188 has an 8-bit data bus, and is tristated off during bus hold.</td></tr>
<tr><td>A19/S6,
A18/S5,
A17/S4,
A16/S3</td><td>65
66
67
68</td><td>O
O
O
O</td><td>ADDRESS BUS OUTPUTS (16 TO 19) and
BUS CYCLE STATUS (3 TO 6)
They reflect the four most significant address bits during T1. These signals are active high. During T2, T3, TW, and T4, status information is available on these lines as encoded below:
<table>
<tr><th></th><th>Low</th><th>High</th></tr>
<tr><td>S6</td><td>Processor Cycle</td><td>DMA Cycle</td></tr>
</table>
S3, S4, and S5 are defined as being low during T2 to T4.</td></tr>
<tr><td>V_{CC}</td><td>9, 43</td><td>I</td><td>POWER SUPPLY (+5 V)</td></tr>
<tr><td>GND</td><td>26, 60</td><td>I</td><td>GROUND (0 V)</td></tr>
</table>

Block Diagram



Functional Description

The SAB 8086, 8088, 80186, 80188 and 80286 families all contain the same basic set of registers, instructions, and addressing modes. The SAB 80188 processor is upward-compatible with the SAB 8086 and SAB 8088 CPUs.

Register Set

The SAB 80188 base architecture has fourteen registers. These registers are grouped into the following categories.

General registers

Eight 16-bit general-purpose registers may be used to contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

Segment registers

Four 16-bit special-purpose registers select, at any time given, the segments of memory that are immediately addressable for code, stack, and data.

Base and index registers

Four of the general-purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

Status and control registers

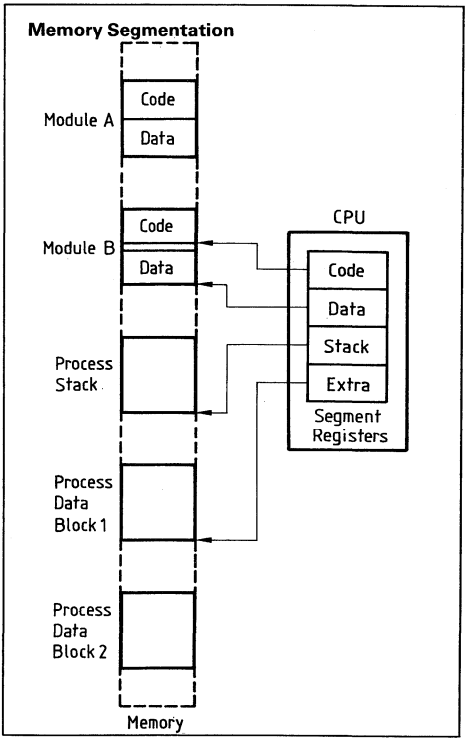
Two 16-bit special-purpose registers record or alter certain aspects of the SAB 80188 processor state. These are the instruction pointer register, which contains the offset address of the next sequential instruction to be executed, and the status word register, which contains status and control flag bits.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64 K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment registers (code, data, stack, extra). The physical address is calculated by shifting the base value left by four bits and adding the 16-bit offset value to yield a 20-bit physical address. This allows for a 1 Mbyte physical address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used. These rules follow the way programs are written as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs.



I/O Space

The I/O space consists of 64 K 8-bit or 32 K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero-extended such that A15 to A8 are low I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (status word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware-initiated, INT instructions, and instruction exceptions. Hardware-initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.

Interrupt Sources

The SAB 80188 can service interrupts generated by software or hardware. The software interrupts are generated by specific instructions (INT, ESC, unused OP, etc.) or the results of conditions specified by instructions (array bounds check, INT0, DIV, IDIV, etc.). All interrupt sources are serviced by an indirect call through an element of a vector table. This vector table is indexed by using the interrupt vector type, multiplied by four. All hardware-generated interrupts are sampled at the end of each instruction. Thus, the software interrupts will begin service first. Once the service routine is entered and interrupts are enabled, any hardware source of sufficient priority can interrupt the service routine in progress.

Interrupt Vector Table

Interrupt Name	Vector Type	Default Priority [5]	Related Instructions
Divide Error Exception	0	1 [1]	DIV, IDIV
Single-Step Interrupt	1	12 [2] 2	All
NMI	2	1	All
Breakpoint Interrupt	3	1 [1]	INT
INT0 Detected Overflow Exception	4	1 [1]	INT0
Array Bounds Exception	5	1 [1]	BOUND
Unused Op Code Exception	6	1 [1]	Undefined Op Codes
ESC Op Code Exception	7	1 [1] [3]	ESC Op Codes
Timer 0 Interrupt	8	2A [4]	
Timer 1 Interrupt	18	2B [4]	
Timer 2 Interrupt	19	2C [4]	
Reserved	9	3	
DMA 0 Interrupt	10	4	
DMA 1 Interrupt	11	5	
INT0 Interrupt	12	6	
INT1 Interrupt	13	7	
INT2 Interrupt	14	8	
INT3 Interrupt	15	9	

1) These are generated as the result of an instruction execution.
2) This is handled as in the SAB 8088.
3) An escape op code will cause a trap only if the proper bit is set in the peripheral control block relocation register.
4) All three timers constitute one source of request to the interrupt controller. The timer interrupts all have the same default priority level with respect to all other interrupt sources. However, they have a defined priority ordering amongst themselves. (Priority 2A is higher priority than 2B.) Each timer interrupt has a separate vector type number.
5) Default priorities for the interrupt sources are used only if the user does not program each source into a unique priority level.

Initialization and Processor Reset

Processor initialization or startup is accomplished by driving the $\overline{RES}$ input pin low. $\overline{RES}$ forces the SAB 80188 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as $\overline{RES}$ is active. After $\overline{RES}$ becomes inactive and an internal processing interval elapses, the SAB 80188 begins execution with the instruction at physical location FFFF0(H). $\overline{RES}$ also sets some registers to predefined values.

Initial Register State after RESET

Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation Register	20FF(H)
UMCS	FFFB(H)

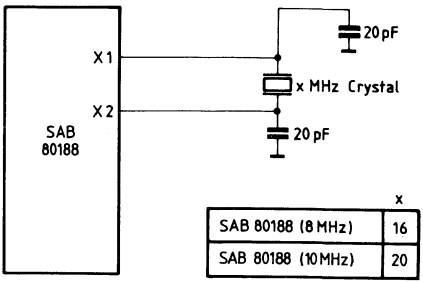
Clock Generator

The SAB 80188 provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs and reset circuitry.

Oscillator

The oscillator circuit of the SAB 80188 is designed to be used with a parallel resonant fundamental mode crystal. This is used as the time base for the SAB 80188. The crystal frequency selected will be twice the CPU clock frequency. Use of an LC or RC circuit is not recommended with this oscillator. If an external oscillator is used, it can be connected directly to input pin X1 in lieu of a crystal. The output of the oscillator is not directly available outside the SAB 80188.

Recommended SAB 80188 Crystal Configuration



The following parameters may be used for choosing a crystal:

Temperature range	0 to 70 °C
ESR (equivalent series resistance)	30 Ω max.
C0 (shunt capacitance of crystal)	7.0 pF max.
C1 (load capacitance)	20 pF ± 2 pF
Drive level	1 mW max.

Ready Synchronization

The SAB 80188 provides both synchronous and asynchronous ready inputs. Asynchronous ready synchronization is accomplished by circuitry which samples ARDY in the middle of T2, T3 and again in the middle of each TW until ARDY is sampled high.

A second ready input (SRDY) is provided to interface with externally synchronized ready signals. This input is sampled at the end of T2,T3 and again at the end of each TW until it is sampled high.

Reset Logic

The SAB 80188 provides both a $\overline{RES}$ input pin and a synchronized reset pin for use with other system components. The $\overline{RES}$ input pin on the SAB 80188 is provided with hysteresis in order to facilitate power-on reset generation via an RC network.

Local Bus Controller

The SAB 80188 provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides control lines that can be used to enable external buffers and to direct the flow of data on and off the local bus.

When the SAB 80188 relinquishes control of the local bus, it tristates $\overline{DEN}$, $\overline{RD}$, $\overline{WR}$, $\overline{S0}$ to $\overline{S2}$, $\overline{LOCK}$, AD0 to AD7, A8 to A19, S7 and DT/$\overline{R}$ to allow another master to drive these lines directly.

Local bus controller and reset

Upon receipt of a reset pulse from the $\overline{RES}$ input, the local bus controller will perform the following actions:

- Drive $\overline{DEN}$, $\overline{RD}$, and $\overline{WR}$ high for one clock cycle, then float.

  Note: $\overline{RD}$ is also provided with an internal pullup device to prevent the processor from inadvertently entering queue status mode during reset.
- Drive $\overline{S0}$ to $\overline{S2}$ to the passive state (all high) and then float.
- Drive $\overline{LOCK}$ high and then float.
- Tristate AD0 to AD7, A8 to A19, S7, DT/$\overline{R}$.
- Drive ALE low (ALE is never tristated).
- Drive HLDA low.

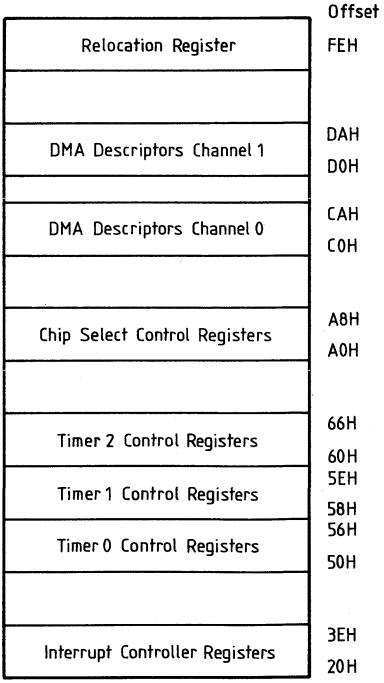
Internal Peripheral Interface

All the SAB 80188 integrated peripherals are controlled via 16-bit registers contained within an internal 256 byte control block. This control block may be mapped into either memory or I/O space. Internal logic will recognize the address and respond to the bus cycle. During bus cycles to internal registers, the bus controller will signal the operation externally (i.e., the $\overline{RD}$, $\overline{WR}$, status, address, data, etc., lines will be driven as in a normal bus cycle), but D7 to D0, SRDY, and ARDY will be ignored.

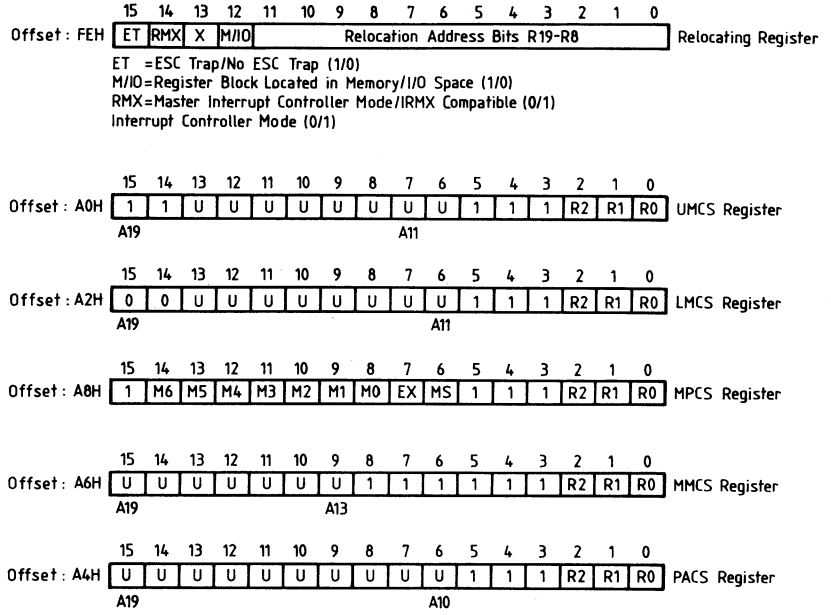
The control block base address is programmed via a 16-bit relocation register contained within the control block at offset FEH from the base address of the control block. It provides the upper 12 bits of the base address of the control block.

The integrated SAB 80188 peripherals operate semi-autonomously from the CPU. Access to them for the most part is via software read/write of the control and data locations in the control block. Most of these registers can be both read and written. A few dedicated lines, such as interrupts and DMA request provide real-time communication between the CPU and peripherals as in a more conventional system utilizing discrete peripheral blocks.

Internal Register Map



Chip Select Registers



UMCS Programming Values

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0=R1=R2=0)
FFC00	1 K	FFF8H
FF800	2 K	FFB8H
FF000	4 K	FF38H
FE000	8 K	FE38H
FC000	16 K	FC38H
F8000	32 K	F838H
F0000	64 K	F038H
E0000	128 K	E038H
C0000	256 K	C038H

LMCS Programming Values

Upper Address	Memory Block Size	LMCS Value (Assuming R0=R1=R2=0)
003FFH	1 K	0038H
007FFH	2 K	0078H
00FFFH	4 K	00F8H
01FFFH	8 K	01F8H
03FFFH	16 K	03F8H
07FFFH	32 K	07F8H
0FFFFH	64 K	0FF8H
1FFFFH	128 K	1FF8H
3FFFFH	256 K	3FF8H

MPCS Programming Values

Total Block Sice	Individual Select Size	MPCS Bits 14 to 8
8 K	2 K	0000001B
16 K	4 K	0000010B
32 K	8 K	0000100B
64 K	16 K	0001000B
128 K	32 K	0010000B
256 K	64 K	0100000B
512 K	128 K	1000000B

MS, EX Programming Values

Bit	Description
MS	1=Peripherals Mapped into Memory Space. 0=Peripherals Mapped into I/O Space.
EX	0=5 $\overline{\text{PCS}}$ Lines. A1, A2 Provided. 1=7 $\overline{\text{PCS}}$ Lines. A1, A2 Are Not Provided.

Ready Bits Programming

R2	R1	R0	Number of Wait States Generated
0	0	0	0 Wait States, External RDY Also Used
0	0	1	1 Wait State Inserted, External RDY Also Used.
0	1	0	2 Wait States Inserted, External RDY Also Used.
0	1	1	3 Wait States Inserted, External RDY Also Used
1	0	0	0 Wait States, External RDY Ignored.
1	0	1	1 Wait State Inserted, External RDY Ignored.
1	1	0	2 Wait States Inserted, External RDY ignored.
1	1	1	3 Wait States Inserted, External RDY Ignored.

Chip Select Logic

The SAB 80188 contains logic which provides programmable chip select generation for both, memories and peripherals. In addition, it can be programmed to provide ready (or wait state) generation. It can also provide latched address bits A1 and A2. The chip select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

Memory Chip Selects

The SAB 80188 provides 6 memory chip select outputs for 3 address areas: upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

Upper Memory $\overline{CS}$

The SAB 80188 provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the SAB 80188 begins executing at memory location FFFF0H. After reset, the UMCS register is programmed for a 1 K area. It must be reprogrammed if a larger upper memory area is desired.

Lower Memory $\overline{CS}$

The SAB 80188 provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H. After reset, the LMCS register value is undefined. However, the $\overline{LCS}$ chip select line will not become active until the LMCS register is accessed.

Midrange Memory $\overline{CS}$

The SAB 80188 provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located anywhere within the 1 Mbyte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

Each of the four chip select lines is active for one of the four equal contiguous divisions of the midrange block. Thus, if the total block size is 32 K, each chip select is active for 8 K of memory with $\overline{MCS0}$ being active for the first range and $\overline{MCS3}$ being active for the last range. After reset, the contents of both of these registers is undefined.

However, none of the $\overline{MCS}$ lines will be active until both the MMCS and MPCS registers are accessed.

Peripheral Chip Selects

The SAB 80188 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. This base address may be located in either memory or I/O space.

Seven $\overline{CS}$ lines called $\overline{PCS0-6}$ are generated by the SAB 80188. The base address is user-programmable; however it can only be a multiple of 1 Kbytes, i.e. the least significant 10 bits of the starting address are always 0.

$\overline{PCS5}$ and $\overline{PCS6}$ can also be programmed to provide latched address bits A1, A2. If so programmed, they cannot be used as peripheral selects.

The starting address of the peripheral chip select block is defined by the PACS register. This register is located at offset A4H in the internal control block. Bits 15 to 6 of this register correspond to bits 19 to 10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block.

PCS Address Ranges

PCS Line	Active between Locations
PCS0	PBA – PBA+127
PCS1	PBA+128 – PBA+255
PCS2	PBA+256 – PBA+383
PCS3	PBA+384 – PBA+511
PCS4	PBA+512 – PBA+639
PCS5	PBA+640 – PBA+767
PCS6	PBA+768 – PBA+895

Ready Generation Logic

The SAB 80188 can generate a ready signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of wait states to be inserted for each peripheral or memory is programmable to provide 0 to 3 wait states for all accesses to the area for which the chip select is active. In addition, the SAB 80188 may be programmed to either ignore external ready for each chip select range individually or to factor external ready with the integrated ready generator.

Ready control consists of 3 bits for each $\overline{CS}$ line or group of lines generated by the SAB 80188.

Chip Select/Ready Logic and Reset

Upon reset, the chip select/ready logic will perform the following actions:

- All chip select outputs will be driven high.
- Upon leaving reset, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1K block with the accompanying ready control bits set at 011 to allow the maximum number of internal wait states in conjunction with external ready consideration (i.e. UMCS resets to FFFBH).
- No other chip select or ready control registers have any predefined values after reset. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the $\overline{PCS}$ lines will become active.

DMA Channels

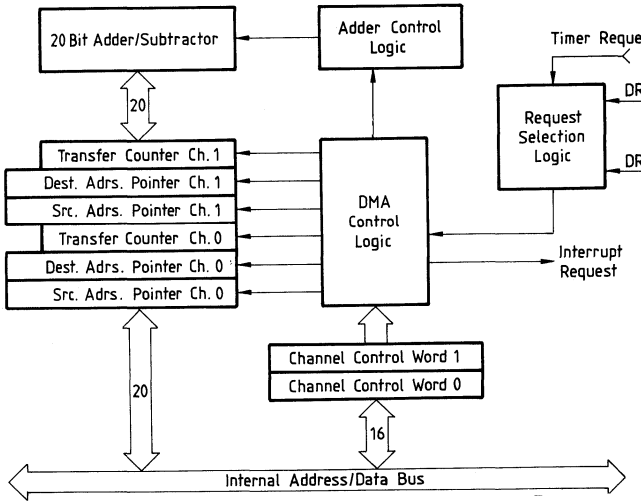
The SAB 80188 DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., memory-to-I/O) or within the same space (e.g., memory-to-memory or I/O-to-I/O). Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer. Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data. This provides a maximum data transfer rate of 1 Mbyte/s.

DMA Channel Control Word Register

Each DMA channel control word determines the mode of operation for the particular SAB 80188 DMA channel.

The DMA channel control registers may be changed while the channel is operating. However, any changes made during operation will affect the current DMA transfer.

DMA Unit Block Diagram



DMA Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M/$\overline{IO}$	Destination DEC	INC	M/$\overline{IO}$	Source DEC	INC	TC	INT	SYN		P	TDRQ	X	CHG/$\overline{NOCHG}$	ST/$\overline{STOP}$	X

X=Don't Care

DMA Memory Pointer Register Format

Higher Register Address	XXX	XXX	XXX	A19-A16
Lower Register Address	A15-A12	A11-A8	A7-A4	A3-A0

15 0

XXX=Don't Care

DMA Control Block Format

Register Name	Register Address	
	Chan. 0	Chan. 1
Control Word	CAH	DAH
Transfer Count	C8H	D8H
Destination Pointer (upper 4 bits)	C6H	D6H
Destination Pointer	C4H	D4H
Source Pointer (upper 4 bits)	C2H	D2H
Source Pointer	C0H	D0H

DMA Control Word Bit Description

ST/$\overline{STOP}$ Start/stop (1/0) channel.

CHG/$\overline{NOCHG}$ Change/do not change (1/0) ST/$\overline{STOP}$ bit. If this bit is set when writing to the control word, the ST/$\overline{STOP}$ bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/$\overline{STOP}$ bit will not be altered. This bit is not stored; it will always be a 0 on read.

INT Enable interrupts to CPU on byte count termination.

TC If set, DMA will terminate when the contents of the transfer count register reach zero. The ST/$\overline{STOP}$ bit will also be reset at this point if TC is set. If this bit is cleared, the DMA unit will decrement the transfer count register for each DMA cycle, but the DMA transfer will not stop when the contents of the TC register reach zero.

SYN (2 bits) 00 No synchronization.
Note: The ST bit will be cleared automatically when the contents of the TC register reach zero regardless of the state of the TC bit.
01 Source synchronization.
10 Destination synchronization.
11 Unused.

TDRQ 0: Disable DMA requests from timer 2.
1: Enable DMA requests from timer 2.

Source: INC Increment source pointer by 1 after each transfer.

M/$\overline{IO}$ Source pointer is in M/IO space (1/0).

DEC Decrement source pointer by 1 after each transfer.

Destin.: INC Increment destination pointer by 1 after each transfer.

M/$\overline{IO}$ Destination pointer is in M/IO space (1/0).

DEC Decrement destination pointer by 1 after each transfer.

P Channel priority – relative to other channel.
0 low priority.
1 high priority.
Channels will alternate cycles if both set at same priority level.

Bit 0 Bit 0 is not used.

Bit 3 Bit 3 is not used.

DMA Destination and Source Pointer Register

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address.

DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). This register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA control register.

DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is, the transfer will take place continually until the correct number of transfers has occurred.

DMA Priority

The DMA channels may be programmed such that one channel is always given priority over the other, or they may be programmed such as to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses or word accesses to odd memory locations; however, an external bus hold takes priority over an internal DMA cycle.

DMA Channels and Reset

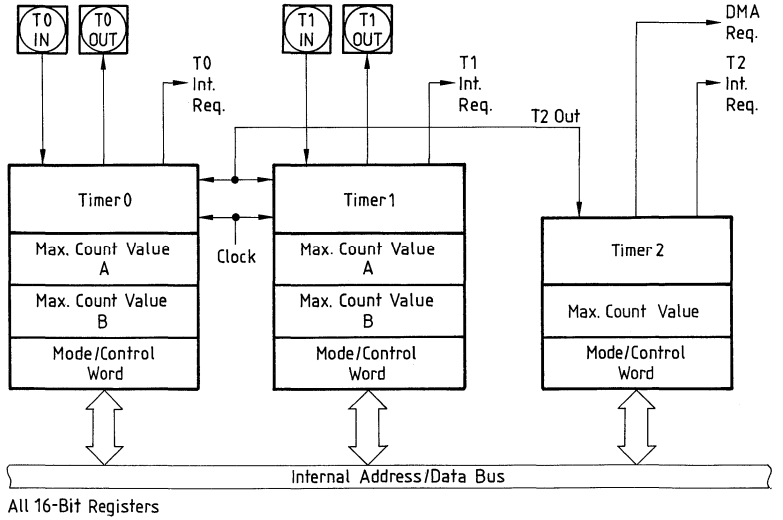
Upon reset, the DMA channels will perform the following actions:

- The start/stop bit for each channel will be reset to STOP.
- Any transfer in progress is aborted.

Timers

The SAB 80188 provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, this third timer can be used as a prescaler to the other two, or as a DMA request source.

Timer Block Diagram



Timer Mode/Control Register

15	14	13	12	11	·····	5	4	3	2	1	0
EN	$\overline{INH}$	INT	RIU	0	·····	MC	RTG	P	EXT	ALT	CONT

Timer Control Block Format

Register Name	Register Offset		
	TMR 0	TMR 1	TMR 2
Mode/Control Word	56H	5EH	66H
Max. Count B	54H	5CH	not present
Max. Count A	52H	5AH	62H
Count Register	50H	58H	60H

Timer Operation

The timers are controlled by eleven 16-bit registers in the internal peripheral control block. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incremented for each timer event. Each of the timers is equipped with a max. count register, which defines the maximum count the timer will reach. After reaching the max. count register value, the timer count value will be reset to zero during that same clock.

Each timer gets serviced every fourth CPU clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU clock rate (2 MHz for an 8 MHz CPU clock).

The timers have several programmable options.

- All three timers can be set to halt or continue on a terminal count.
- Timers 0 and 1 can select between internal and external clocks, alternate between max. count registers and be set to retrigger on external events.
- The timers may be programmed to cause an interrupt on terminal count.

Count Registers

Each of the three timers has a 16-bit count register. The current contents of this register may be read or written by the processor at any time. If the register is written into while the timer is counting, the new value will take effect in the current count cycle.

Max. Count Registers

Timers 0 and 1 have two max. count registers, while timer 2 has a single max.count register. These contain the number of events the timer will count. In timers 0 and 1, the max.count register used can alternate between the two max.count values whenever the current maximum count is reached.

Timer Mode/Control Register

The mode/control register allows the user to program the specific mode of operation or check the current programmed status for any of the three integrated timers.

ALT:
The ALT bit determines which of two max. count registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one max.count register while the other is being used, and thus provides a method of generating nonrepetitive waveforms. Square waves and pulse outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is zero, the output pin will go low for one clock, the clock after the maximum count is reached. If ALT is one, the output pin will reflect the current max.count register being used (0/1 for B/A).

CONT:
Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the max. count register A value, be reset, count to the register B value, be reset, and halt.

EXT:
The external bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the SAB 80188 clock. If EXT is set, the timer will count low-to-high transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input-to-output transition latency time may be as much as 6 clocks. However, clock inputs may be pipelined as closely together as every 4 clocks without losing clock pulses.

P:
The prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a zero, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a one, the output of timer 2 will be used as a clock for the timer. Note that the user must initialize and start timer 2 to obtain the prescaled clock.

RTG:
Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is high, the timer will count; if the input pin is low, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the SAB 80188 clock.

When RTG = 1, the input pin detects low-to-high transitions. The first transition starts the timer running, clearing the timer value to zero on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to zero, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

EN:
The enable bit provides programmer control over the timer's RUN/HALT status. When set, the timer is enabled to increment subject to the input pin constraints in the internal clock mode (discussed previously). When cleared, the timer will be inhibited from counting. All input pin transitions during which the time EN is zero will be ignored. If CONT is zero, the EN bit is automatically cleared upon maximum count.

INH:
The inhibit bit allows for selective updating of the enable (EN) bit. If INH is a one during the write to the mode/control word, then the state of the EN bit will be modified by the write. If INH is a zero during the write, the EN bit will be unaffected by the operation. This bit is not stored; it will always be a 0 on a read.

INT:
When set, the INT bit enables interrupts from the timer, which will be generated on every terminal count. If the timer is configured in dual max.count register mode, an interrupt will be generated each time the value in max.count register A is reached, and each time the value in max.count register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the interrupt controller.)

MC:
The maximum count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual max.count register mode, this bit will be set each time the value in max.count register A is reached, and each time the value in max.count register B is reached. This bit is set regardless of the timer's interrupt enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts.
Programmer intervention is required to clear this bit.

RIU:
The register in use bit indicates which max.count register is currently being used for comparison to the timer count value. A zero indicates register A. The RIU bit cannot be written, i.e. its value is not affected when the control register is written. It is always cleared when the ALT bit is zero.
Not all mode bits are provided for timer 2. Certain bits are hardwired as indicated below:

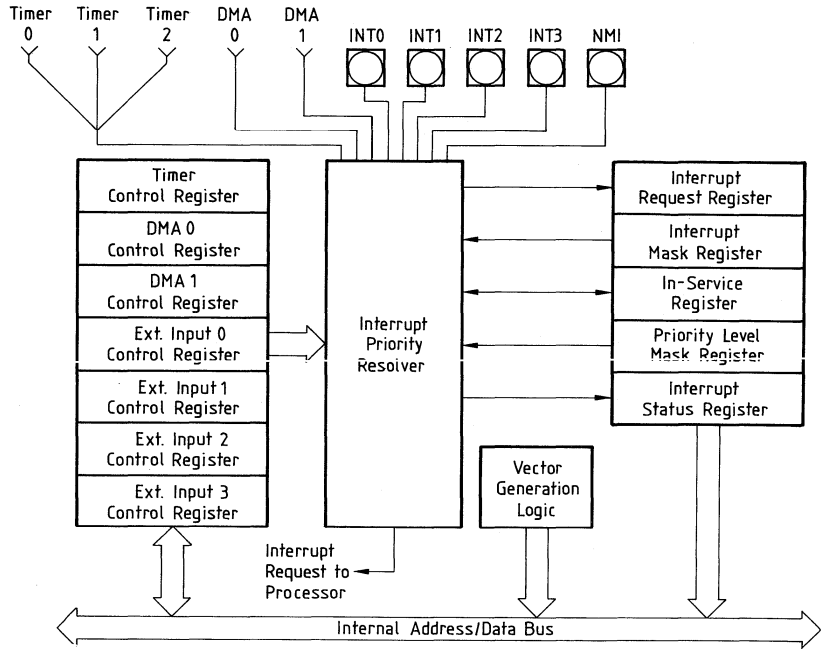
ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

Timers and Reset

Upon reset, the timers will perform the following actions:

- All EN (enable) bits are reset preventing timer counting.
- All SEL (select) bits are reset to zero. This selects max. count register A, resulting in the timer-out pins going high upon reset.

Interrupt Controller Block Diagram



Interrupt Controller

The SAB 80188 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU. Internal interrupt sources (timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The SAB 80188 interrupt controller has its own control registers that set the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may themselves be interrupted by higher priority interrupts.
The interrupt controller has a special iRMX 86 compatibility mode that allows the use of the SAB 80188 within the iRMX 86 operating system interrupt structure.

Master Mode Operation

Interrupt Controller External Interface

For external interrupt sources, five dedicated pins are provided. One of these pins is dedicated to NMI, non-maskable interrupt. This is typically used for power-fail interrupts, etc. The other four pins may function either as four interrupt input lines with internally generated interrupt vectors, as an interrupt line and an interrupt acknowledge line (called the "cascade mode") along with two other input lines with internally generated interrupt vectors, or as two interrupt input lines and two dedicated interrupt acknowledge output lines. When the interrupt lines are configured in cascade mode, the SAB 80188 interrupt controller will not generate internal interrupt vectors.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in master mode are similar to the SAB 8259A. The interrupt controller responds identical to internal interrupts in all three modes: the difference is only in the interpretation of function of the four external interrupt pins.

Fully nested mode

When in fully nested mode, four pins are used as direct interrupt requests. The vectors for these four inputs are generated internally. An in-service bit (IS) is provided for every interrupt source. If a lower priority device requests an interrupt while the in-service bit is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller.
When a service routine is completed, the proper IS bit must be reset by writing the proper pattern to the EOI register.

Cascade mode

The SAB 80188 has four interrupt pins and two of them have dual functions. In fully nested mode, the four pins are used as direct interrupt inputs and the corresponding vectors are generated internally. In cascade mode, the four pins are configured into interrupt input-dedicated acknowledge signal pairs. INT0 is an interrupt input interfaced to an SAB 8259A, while INT2/$\overline{\text{INTA0}}$ serves as the dedicated interrupt acknowledge signal to the peripheral. The same is true for INT1 and INT3/$\overline{\text{INTA1}}$. Each pair can selectively be placed in the cascade or non-cascade mode by programming the proper value INT0 and INT1 control registers.
The primary cascade mode allows the capability to serve up to 128 external interrupt sources through the use of external master and slave SAB 8259As.

Special fully nested mode

This mode is entered by setting the SFNM bit in INT0 or INT1 control register. It enables complete nestability with external SAB 8259A masters. In special fully nested mode, the SAB 80188 interrupt controller will allow interrupts from an external pin regardless of the state of the in-service bit for an interrupt source in order to allow multiple interrupts from a single pin.

Polling operation

The controller may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the interrupt controller whenever it is convenient. Polling the interrupt controller is accomplished by reading the poll word. Bit 15 in the poll word indicates to the processor that an interrupt of high enough priority is requesting service.

Interrupt Controller Registers (non-iRMX 86 mode)

	Offset
INT3 Control Register	3EH
INT2 Control Register	3CH
INT1 Control Register	3AH
INT0 Control Register	38H
DMA1 Control Register	36H
DMA0 Control Register	34H
Timer Control Register	32H
Interrupt Status Register	30H
Interrupt Request Register	2EH
In-Service Register	2CH
Priority Mask Register	2AH
Mask Register	28H
Poll Status Register	26H
Poll Register	24H
EOI Register	22H

Timer/DMA Control Register Formats

15	14	...	4	3	2	1	0
0	0	...	0	MSK	PR2	PR1	PR0

INT0/INT1 Control Register Formats

15	14	...	7	6	5	4	3	2	1	0
0	0	...	0	SFNM	C	LTM	MSK	PR2	PR1	PR0

INT2/INT3 Control Register Formats

15	14	...	5	4	3	2	1	0
0	0	...	0	LTM	MSK	PR2	PR1	PR0

In-Service, Interrupt Request, and Mask Register Formats

15	14	...	10	9	8	7	6	5	4	3	2	1	0
0	0	...	0	0	0	I3	I2	I1	I0	D1	D0	0	TMR

Priority Mask Register Format

15	14	...	3	2	1	0
0	0	...	0	PRM 2	PRM 1	PRM 0

Interrupt Status Register Format

15	14	...	7	6	5	4	3	2	1	0
DHLT	0	...	0	0	0	0	0	IRT2	IRT1	IRT0

EOI Register Format

15	14	13	...	5	4	3	2	1	0
SPEC/NSPEC	0	0	...	0	S4	S3	S2	S1	S0

Poll Register Format

15	14	13	...	5	4	3	2	1	0
INT REQ.	0	0	...	0	S4	S3	S2	S1	S0

Master Mode Features

Programmable priority
The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0 to 7) in the control register of each interrupt source.

End-of-interrupt command
The end-of-interrupt (EOI) command is used by the programmer to reset the in-service (IS) bit when an interrupt service routine is completed. The EOI command is issued by writing the proper pattern to the EOI register. There are two types of EOI commands, specific and nonspecific. The non-specific command does not specify which IS bit is reset.

Trigger mode
The four external interrupt pins can be programmed in either edge or level-trigger mode. The control register for each external source has a level-trigger mode (LTM) bit. All interrupt inputs are active high. In the edge-sense mode or the level-trigger mode, the interrupt request must remain active (high) until the interrupt request is acknowledged by the SAB 80188 CPU. In the edge-sense mode, if the level remains high after the interrupt is acknowledged, the input is disabled and no further requests will be generated. The input level must go low for at least one clock cycle to reenable the input.

Interrupt vectoring
The SAB 80188 interrupt controller will generate interrupt vectors for the integrated DMA channels and the integrated timers. In addition, the interrupt controller will generate interrupt vectors for the external interrupt lines if they are not configured in cascade or special fully nested mode.

Interrupt Controller Registers

In-service register
This register contains the in-service bit for each of the interrupt sources. The in-service bit is set to indicate that a source's service routine is in progress. When an in-service bit is set, the interrupt controller will not generate interrupts to the CPU when it receives interrupt requests from devices with a lower programmed priority level. The TMR bit is the in-service bit for all three timers; the D0 and D1 bits are the in-service bits for the two DMA channels; the I0 – I3 bits are the in-service bits for the external interrupt pins.

Interrupt request register
The internal interrupt sources have interrupt request bits inside the interrupt controller. A read from this register yields the status of these bits. The TMR bit is the logical OR of all timer interrupt requests. D0 and D1 are the interrupt request bits for the DMA channels.

Mask register
This is a 16-bit register that contains a mask bit for each interrupt source. A one in a bit position corresponding to a particular source serves to mask the source from generating interrupts. These mask bits are exactly the same bits which are used in the individual control registers.

Priority mask register
This register is used to mask all interrupts below particular interrupt priority levels. The code in the lower three bits of this register inhibits interrupts of priority lower (a higher priority number) than the code specified.

Interrupt status register
This register contains general interrupt controller status information. The bits in the status register have the following functions:

DHLT: DMA halt transfer; setting this bit halts all DMA transfers. It is automatically set whenever a non-maskable interrupt occurs, and it is reset when an IRET instruction is executed.

IRTx: These three bits represent the individual timer interrupt request bits. These bits are used to differentiate the timer interrupts, since the timer IR bit in the interrupt request register is the "OR" function of all timer interrupt requests.

Timer, DMA 0, 1 control registers
These registers are the control words for all the internal interrupt sources. The three bit positions PR0, PR1, and PR2 represent the programmable priority level of the interrupt source. The MSK bit inhibits interrupt requests from the interrupt source. The MSK bits in the individual control registers are exactly the same bits as are in the mask register; modifying them in the individual control registers will also modify them in the mask register, and vice versa.

INT0 to INT3 control registers
These registers are the control words for the four external input pins. In cascade mode or special fully nested mode, the control words for INT2 and INT3 are not used.

PR0-2: Priority programming information. Highest priority = 000, lowest priority = 111

LTM: Level-trigger mode bit. 1 = level-triggered; 0 = edge-triggered. Interrupt input levels are active high. In level-triggered mode, an interrupt is generated whenever the external line is high. In edge-triggered mode, an interrupt will be generated only when this level is preceded by an inactive-to-active transition on the line. In both cases, the level must remain active until the interrupt is acknowledged.

MSK: Mask bit, 1 = mask; 0 = nonmask.

C: Cascade mode bit, 1 = cascade; 0 = direct

SFNM: Special fully nested mode bit, 1 = SFNM

EOI register
The end-of-interrupt register is a command register which can only be written into. It initiates an EOI command when written to by the SAB 80188 CPU.

S_x: Encoded information that specifies an interrupt source vector type

NSPEC/SPEC: A bit that determines the type of EOI command. Nonspecific = 1, specific = 0.

Poll and poll status registers
These registers contain polling information. They can only be read. Reading the poll register constitutes a software poll. This will set the IS bit of the highest priority pending interrupt.

S_x: Encoded information that indicates the vector type of the highest priority interrupting source. Valid only when INTREQ = 1.

INTREQ: This bit determines if an interrupt request is present. Interrupt request = 1; no interrupt request = 0.

iRMX 86 Compatibility Mode

This mode allows iRMX 86-SAB 80188 compatibility. The interrupt model of iRMX 86 requires one master and multiple slave SAB 8259As in cascaded mode. When iRMX mode is used, the internal SAB 80188 interrupt controller will be used as a slave controller to an external master interrupt controller.
Upon reset, the SAB 80188 interrupt controller will be in the non-iRMX 86 mode of operation. To set the controller in the iRMX 86 mode, bit 14 of the relocation register should be set.

The iRMX 86 operating system requires peripherals to be assigned fixed priority levels. This is incompatible with the normal operation of the SAB 80188 interrupt controller. Therefore, the initialization software must program the proper priority levels for each source.

Required iRMX Internal Source Priority Levels

Priority Level	Interrupt Source
0	Timer 0
1	(reserved)
2	DMA 0
3	DMA 1
4	Timer 1
5	Timer 2

iRMX 86 Mode External Interface

In the iRMX 86 configuration of the SAB 80188 the INT0 input is used as the SAB 80188 CPU interrupt input. INT3 functions as an output to send the SAB 80188 slave-interrupt-request to one of the 8 master PIC inputs. Correct master-slave interface requires decoding of the slave addresses (CAS0–2). Slave SAB 8259As do this internally. Because of pin limitations, the SAB 80188 slave address will have to be decoded externally. $\overline{\text{INT1}}$ is used as a slave-select input.

$\overline{\text{INT2}}$ is used as an acknowledge output, suitable to drive the $\overline{\text{INTA}}$ input of an SAB 8259A.

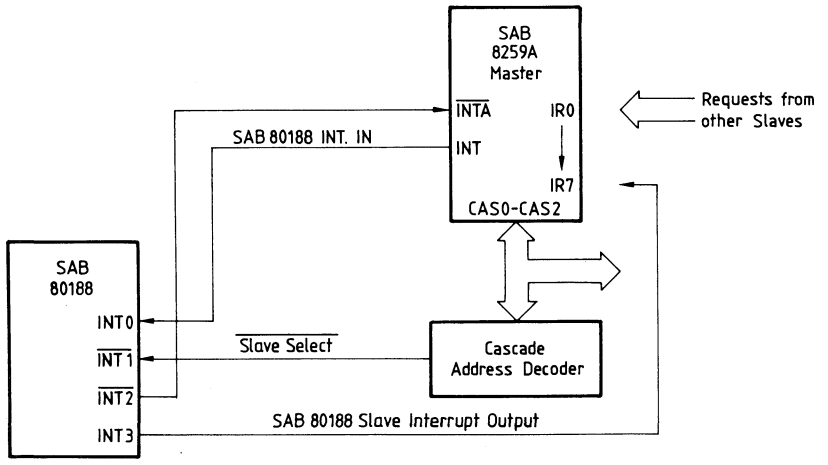
Vector Generation in the iRMX 86 Mode

Vector generation in iRMX mode is exactly like that of an SAB 8259A slave. The interrupt controller generates an 8-bit vector which the CPU multiplies by four and uses as an address into a vector table. The significant five bits of the vector are user-programmable while the lower three bits are generated by the priority logic.

Specific End-of-Interrupt

In iRMX mode the specific EOI command operates to reset an in-service bit of a specific priority. The user supplies a 3-bit priority-level value that points to an in-service bit to be reset.

iRMX 86 Interrupt Controller Interconnection



Interrupt Controller Registers (iRMX 86 mode)

	Offset
Level 5 Control Register (Timer 2)	3AH
Level 4 Control Register (Timer 1)	38H
Level 3 Control Register (DMA 1)	36H
Level 2 Control Register (DMA 0)	34H
Level 0 Control Register (Timer 0)	32H
Interrupt Status Register	30H
Interrupt-Request Register	2EH
In-Service Register	2CH
Priority-Level Mask Register	2AH
Mask Register	28H
Specific EOI Register	22H
Interrupt Vector Register	20H

Specific EOI Register Format

15	14	13	...	8	7	6	5	4	3	2	1	0
0	0	0	...	0	0	0	0	0	0	L2	L1	L0

In-Service, Interrupt Request, and Mask Register Format

15	14	13	...	8	7	6	5	4	3	2	1	0
0	0	0	...	0	0	0	TMR 2	TMR 1	D1	D0	0	TMR 0

Control Word Format

15	14	13	...	8	7	6	5	4	3	2	1	0
0	0	0	...	0	0	0	0	0	MSK	PR2	PR1	PR0

Interrupt Vector Register Format

15	14	13	...	8	7	6	5	4	3	2	1	0
0	0	0	...	0	t4	t3	t2	t1	t0	0	0	0

Priority Level Mask Register

15	14	13	...	8	7	6	5	4	3	2	1	0
0	0	0	...	0	0	0	0	0	0	m2	m1	m0

Interrupt Controller Registers in the iRMX 86 Mode

End-of-interrupt register
The end-of-interrupt register is a command register which can only be written to. It initiates an EOI command when written to by the SAB 80188 CPU.

Lx: Encoded value indicating the priority of the IS bit to be reset.

In-service register
This register contains the in-service bit for each of the internal interrupt sources. Bit positions 2 and 3 correspond to the DMA channels; positions 0, 4, and 5 correspond to the integral timers.

Interrupt request register
This register indicates which internal peripherals have interrupt requests pending. The interrupt request bits are set when a request arrives from an internal source, and are reset when the processor acknowledges the request.

Mask register
This register contains a mask bit for each interrupt source. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked.

Control registers
These registers are the control words for all the internal interrupt sources.

PRx: 3-bit encoded field indicating a priority level for the source; note that each source must be programmed at specified levels.

MSK: Mask bit for the priority level indicated by PRx bits.

Interrupt vector register
This register provides the upper five bits of the interrupt vector address. The interrupt controller itself provides the lower three bits of the interrupt vector as determined by the priority level of the interrupt request.
The format of the bits in this register is:

tx: 5-bit field indicating the upper five bits of the vector address.

Priority-level mask register
This register indicates the lowest priority-level interrupt which will be serviced.

The encoding of the bits in this register is:

mx: 3-bit encoded field indication priority-level value. All levels of lower priority will be masked.

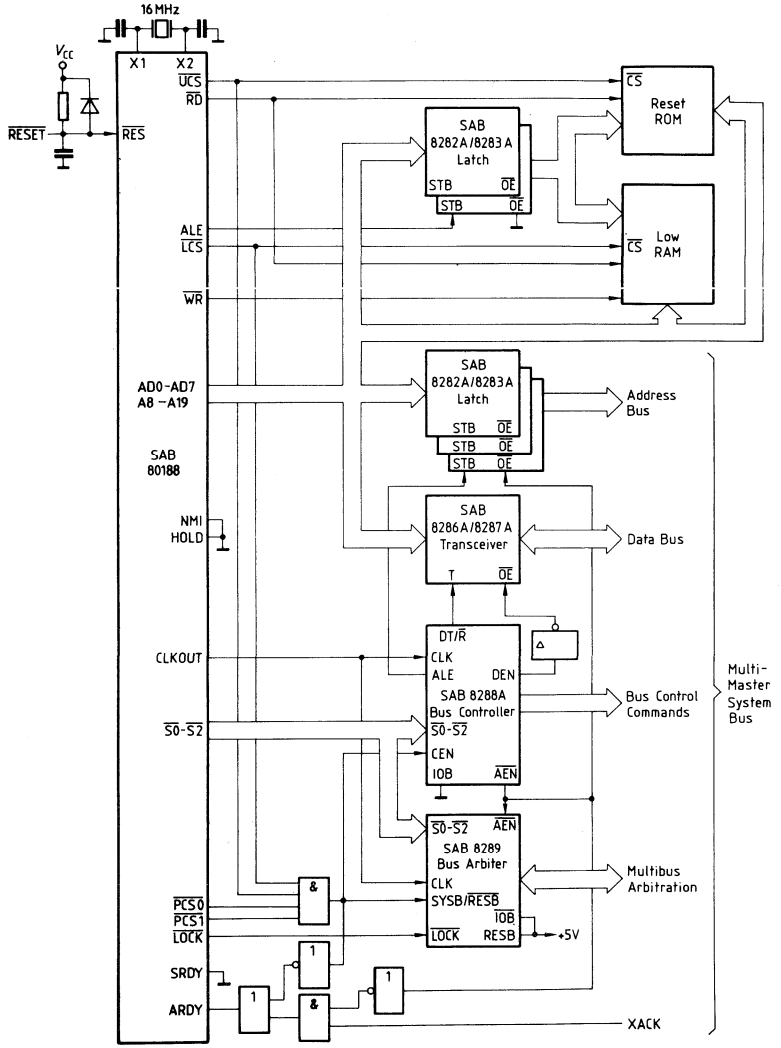
Interrupt status register
This register is defined exactly as in non-iRMX mode.

Interrupt Controller and Reset

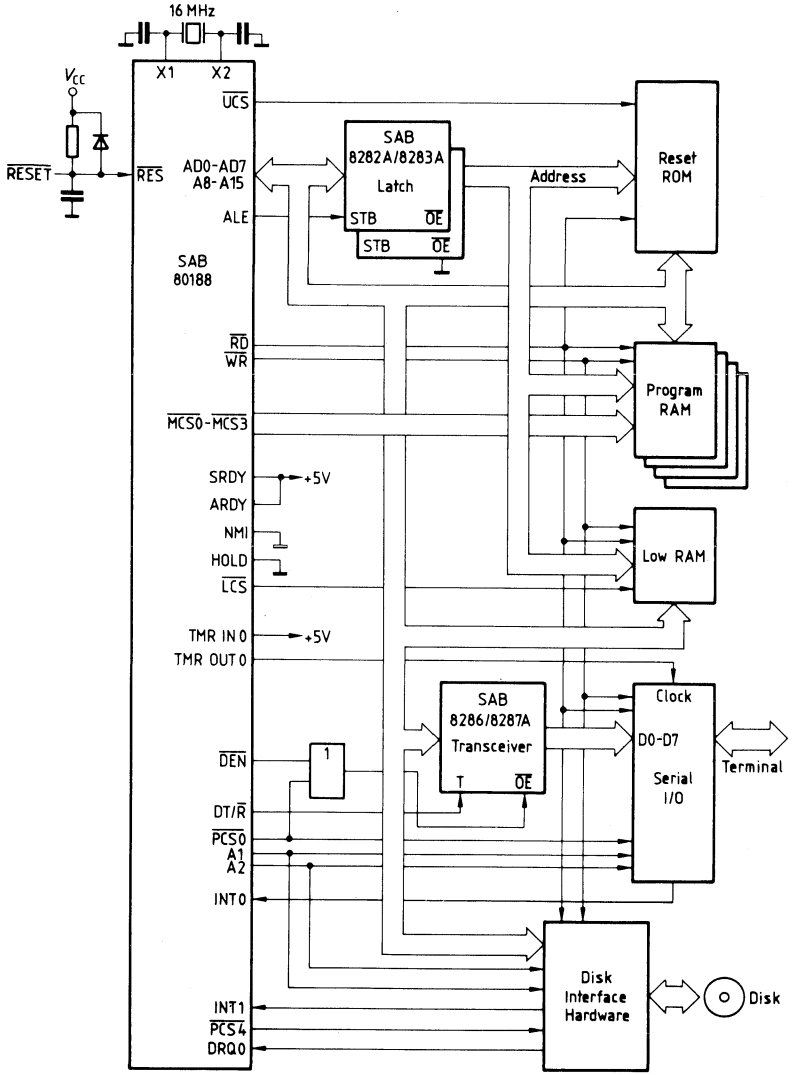
Upon reset, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying fully nested mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All interrupt service bits reset to 0.
- All interrupt request bits reset to 0.
- All MSK (interrupt mask) bits set to 1 (mask).
- All C (cascade) bits reset to 0 (non-cascade).
- All PRM (Priority mask) bits set to 1, implying no levels masked.
- Initialized to non-iRMX 86 mode.

Typical SAB 80188 Multimaster Bus Interface



Typical SAB 80188 System Configuration



Instruction Timings

The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The op code, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word data is located on even-address boundaries.

All jumps and calls include the time required to fetch the op code of the next instruction at the destination address.

All instructions which involve memory reference can require one (and in some cases, two) additional clocks above the minimum timings shown. This is due to the asynchronous nature of the handshake between the BIU and the execution unit.

Notes:

The effective address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

If r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

* except if mod = 00 and r/m = 110 then EA = disp-high: disp-low

Note: EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment override prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-bit (w = 1)	8-bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

Instruction Set Summary

Function	Format	Clock Cycles	Comments
Data Transfer			
MOV = Move:			
Register to register/memory	1000100w | mod reg r/m	2/12	
Register/memory to register	1000101w | mod reg r/m	2/9	
Immediate to register/memory	1100011w | mod 000 r/m | data | data if w = 1	12–13	8/16-bit
Immediate to register	1011w reg | data | data if w = 1	3–4	8/16-bit
Memory to accumulator	1010000w | addr-low | addr-high	9	
Accumulator to memory	1010001w | addr-low | addr-high	8	
Register/memory to segment register	10001110 | mod 0 reg r/m	2/9	
Segment register to register/memory	10001100 | mod 0 reg r/m	2/11	
PUSH = Push:			
Memory	11111111 | mod 110 r/m	16	
Register	01010 reg	10	
Segment register	000reg110	9	
Immediate	011010s0 | data | data if s = 0	10	
PUSHA = Push All	01100000	36	
POP = Pop:			
Memory	10001111 | mod 000 r/m	20	
Register	01011 reg	10	
Segment register	000reg111 (reg ≠ 01)	8	

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format			Clock Cycles	Comments
Data Transfer (cont'd)					
POPA = Pop All	01100001			51	
XCHG = **Exchange:**					
Register/memory with register	1000011w	mod reg r/m		4/17	
Register with accumulator	10010 reg			3	
IN = **Input from:**					
Fixed port	1110010w	port		10	
Variable port	1110110w			8	
OUT = **Output to:**					
Fixed port	1110011w	port		9	
Variable port	1110111w			7	
XLAT = Translate byte to AL	11010111			11	
LEA = Load EA to register	10001101	mod reg r/m		6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod ≠ 11)	18	
LES = Load pointer to ES	11000100	mod reg r/m	(mod ≠ 11)	18	
LAHF = Load AH with flags	10011111			2	
SAHF = Store AH into flags	10011110			3	
PUSHF = Push flags	10011100			9	
POPF = Pop flags	10011101			8	
SEGMENT = **Segment override:**					
CS	00101110			2	
SS	00110110			2	
DS	00111110			2	
ES	00100110			2	

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Arithmetic			
ADD = Add:			
Reg./memory with register to either	00000dw | mod reg. r/m	3/10	
Immediate to register/memory	100000sw | mod 000 r/m | data | data if s w = 01	4/16	
Immediate to accumulator	0000010w | data | data if w = 1	3/4	8/16-bit
ADC = Add with carry:			
Reg./memory with register to either	000100dw | mod reg r/m	3/10	
Immediate to register/memory	100000sw | mod 010 r/m | data | data if s w = 01	4/16	
Immediate to accumulator	0001010w | data | data if w = 1	3/4	8/16-bit
INC = Increment			
Register/memory	1111111w | mod 000 r/m	3/15	
Register	01000 reg	3	
SUB = Subtract			
Reg./memory and register to either	001010dw | mod reg r/m	3/10	
Immediate from register/memory	100000sw | mod 101 r/m | data | data if s w = 01	4/16	
Immediate from accumulator	0010110w | data | data if w = 1	3/4	8/16-bit
SBB = Subtract with borrow:			
Reg./memory and register to either	000110dw | mod reg r/m	3/10	
Immediate from register/memory	100000sw | mod 011 r/m | data | data if s w = 01	4/16	
Immediate from accumulator	0001110w | data | data if w = 1	3/4	8/16-bit

Function	Format	Clock Cycles	Comments
Arithmetic (cont'd):			
DEC = **Decrement:**			
Register/memory	1 1 1 1 1 1 1 w | mod 0 0 1 r/m	3/15	
Register	0 1 0 0 1 reg	3	
CMP = **Compare:**			
Register/memory with register	0 0 1 1 1 0 1 w | mod reg r/m	3/10	
Register with register/memory	0 0 1 1 1 0 0 w | mod reg r/m	3/10	
Immediate with register/memory	1 0 0 0 0 0 s w | mod 1 1 1 r/m | data | data if s w=01	3/10	
Immediate with accumulator	0 0 1 1 1 1 0 w | data | data if w = 1	3/4	8/16-bit
NEG = Change sign	1 1 1 1 0 1 1 w | mod 0 1 1 r/m	3	
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1	8	
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1	4	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1	7	
DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1	4	
MUL = Multiply (unsigned):	1 1 1 1 0 1 1 w | mod 1 0 0 r/m		
register–byte		26–28	
register–word		35–37	
memory–byte		32–34	
memory–word		41–43	
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w | mod 1 0 1 r/m		
register–byte		25–28	
register–word		34–37	
memory–byte		31–34	
memory–word		40–43	

Function	Format	Clock Cycles	Comments
Arithmetic (cont'd):			
IMUL = Integer immediate multiply (signed)	0 1 1 0 1 0 s 1 | mod reg r/m | data | data if s = 0	22–25/29–32	
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w | mod 1 1 0 r/m		
register–byte		29	
register–word		38	
memory–byte		35	
memory–word		44	
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w | mod 1 1 1 r/m		
register–byte		44–52	
register–word		53–61	
memory–byte		50–58	
memory–word		59–67	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0	19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1 | 0 0 0 0 1 0 1 0	15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0	2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1	4	
Logic			
Shift/rotate instructions:			
Register/memory by 1	1 1 0 1 0 0 0 w | mod TTT r/m	2/15	
Register/memory by CL	1 1 0 1 0 0 1 w | mod TTT r/m	5+n/17+n	
Register/memory by count	1 1 0 0 0 0 0 w | mod TTT r/m | count	5+n/17+n	

TTT	Instruction
0 0 0	ROL
0 0 1	ROR
0 1 0	RCL
0 1 1	RCR
1 0 0	SHL/SAL
1 0 1	SHR
1 1 1	SAR

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Logic (cont'd):			
AND = **And:**			
Reg./memory and register to either	0 0 1 0 0 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 1 0 0 r/m | data | data if w = 1	4/16	
Immediate to accumulator	0 0 1 0 0 1 0 w | data | data f w = 1	3/4	8/16-bit
TEST = **And function to flags, no result:**			
Register/memory and register	1 0 0 0 0 1 0 w | mod reg r/m	3/10	
Immediate data and register/memory	1 1 1 1 0 1 1 w | mod 0 0 0 r/m | data | data if w = 1	4/10	
Immediate data and accumulator	1 0 1 0 1 0 0 w | data | data if w = 1	3/4	8/16-bit
OR = **Or:**			
Reg./memory and register to either	0 0 0 0 1 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 0 0 1 r/m | data | data if w = 1	4/16	
Immediate to accumulator	0 0 0 0 1 1 0 w | data | data if w = 1	3/4	8/16-bit
XOR = **Exclusive Or:**			
Reg./memory and register to either	0 0 1 1 0 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 1 1 0 r/m | data | data if w = 1	4/16	
Immediate to accumulator	0 0 1 1 0 1 0 w | data | data if w = 1	3/4	8/16-bit
NOT = Invert register/memory	1 1 1 1 0 1 1 w | mod 0 1 0 r/m	3	

Function	Format	Clock Cycles	Comments
String Manipulation:			
MOVS = Move byte/word	1 0 1 0 0 1 0 w	14	
CMPS = Compare byte/word	1 0 1 0 0 1 1 w	22	
SCAS = Scan byte/word	1 0 1 0 1 1 1 w	15	
LODS = Load byte/word to AL/AX	1 0 1 0 1 1 0 w	12	
STOS = Store byte/word from AL/AX	1 0 1 0 1 0 1 w	10	
INS = Input byte/word from DX port	0 1 1 0 1 1 0 w	14	
OUTS = Output byte/word to DX port	0 1 1 0 1 1 1 w	14	
Repeated by count in CX			
MOVS = Move string	1 1 1 1 0 0 1 0 | 1 0 1 0 0 1 0 w	8 + 8n	
CMPS = Compare string	1 1 1 1 0 0 1 z | 1 0 1 0 0 1 1 w	5 + 22n	
SCAS = Scan string	1 1 1 1 0 0 1 z | 1 0 1 0 1 1 1 w	5 + 15n	
LODS = Load string	1 1 1 1 0 0 1 0 | 1 0 1 0 1 1 0 w	6 + 11n	
STOS = Store string	1 1 1 1 0 0 1 0 | 1 0 1 0 1 0 1 w	6 + 9n	
INS = Input string	1 1 1 1 0 0 1 0 | 0 1 1 0 1 1 0 w	8 + 8n	
OUTS = Output string	1 1 1 1 0 0 1 0 | 0 1 1 0 1 1 1 w	8 + 8n	

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Control Transfer:			
CALL = Call:			
Direct within segment	11101000 | disp-low | disp-high	15	
Register/memory indirect within segment	11111111 | mod 010 r/m	13/19	
Direct intersegment	10011010 | segment offset segment selector	23	
Indirect intersegment	11111111 | mod 011 r/m (mod ≠ 11)	38	

Function	Format			Clock Cycles	Comments
Control Transfer (cont'd):					
JMP = Unconditional jump:					
Short/long	11101011	disp-low		14	
Direct within segment	11101001	disp-low	disp-high	14	
Register/memory indirect within segment	11111111	mod 100 r/m		11/17	
Direct intersegment	11101010	segment offset		14	
		segment selector			
Indirect intersegment	11111111	mod 101 r/m	(mod ≠ 11)	26	
RET = Return from CALL:					
Within segment	11000011			16	
Within seg. adding immediate to SP	11000010	data-low	data-high	18	
Intersegment	11001011			22	
Intersegment adding immediate to SP	11001010	data-low	data-high	25	

Function	Format		Clock Cycles	Comments
Control Transfer (cont'd):				
JE/JZ = Jump on equal/zero	01110100	disp	4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp	4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp	4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp	4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp	4/13	
JP/JPE = Jump on parity/parity even	01111010	disp	4/13	
JO = Jump on overflow	01110000	disp	4/13	
JS = Jump on sign	01111000	disp	4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp	4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp	4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp	4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp	4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp	4/13	
JNP/JPO = Jump on not parity/parity odd	01111011	disp	4/13	
JNO = Jump on not overflow	01110001	disp	4/13	
JNS = Jump on not sign	01111001	disp	4/13	
JCXZ = Jump on CX zero	11100011	disp	5/15	
LOOP = Loop CX times	11100010	disp	6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp	6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp	6/16	

Function	Format	Clock Cycles	Comments
Control Transfer (cont'd):			
ENTER = Enter procedure	11001000 | data-low | data-high | L		
L = 0		15	
L = 1		25	
L > 1		22 + 16(n − 1)	
LEAVE = Leave procedure	11001001	8	
INT = **Interrupt:**			
Type specified	11001101 | type	47	
Type 3	11001100	45	
INTO = Interrupt on overflow	11001110	48/4	if INT taken/ if INT not taken
IRET = Interrupt return	11001111	28	
BOUND = Detect value out of range	01100010 | mod reg r/m	33–35	

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Processor Control			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{\text{TEST}} = 0$
LOCK = Bus lock prefix	11110000	2	
ESC = Processor extension escape	11011TTT mod LLL r/m (TTT LLL are op codes to processor extension)	6	

Absolute Maximum Ratings [1]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to + 150°C
Voltage on any pin with respect to ground	−0.5 to +7V
Power dissipation	3W

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5V ± 10%

Symbol	Parameter	Limit values		Unit	Test condition	
		min.	max.			
V_{IL}	Input low voltage	−0.5	+0.8	V	–	
V_{IH}	Input high voltage (all except X1 and $\overline{RES}$)	2.0	V_{CC} +0.5	V	–	
V_{IH1}	Input high voltage ($\overline{RES}$)	3.0	V_{CC} +0.5	V	–	
V_{OL}	Output low voltage	–	0.45	V	I_a = 2.5 mA for $\overline{S0}$-$\overline{S2}$ I_a = 2.0 mA for all other outputs	
V_{OH}	Output high voltage	2.4	–	V	I_{oa} = −400μA	
I_{CC}	Power supply current	–	550	mA	T_A = 0°C	All outputs disconnected
		–	450	mA	T_A = 70°C	
I_{LI}	Input leakage current	–	± 10	μA	0V < V_{IN} < V_{CC}	
I_{LO}	Output leakage current	–	± 10	μA	0.45V < V_{OUT} < V_{CC}	
V_{CLO}	Clock output low	–	0.6	V	I_a = 4.0 mA	
V_{CHO}	Clock output high	4.0	–	V	I_{oa} = −200 μA	
V_{CLI}	Clock input low voltage	−0.5	0.6	V	–	
V_{CHI}	Clock input high voltage	3.9	V_{CC} + 1.0	V	–	
C_{IN}	Input capacitance	–	10	pF	–	
C_{IO}	I/O capacitance	–	20	pF	–	

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics

T_A = 0 to 70°C, V_{CC} = 5V ± 10%

Timing requirements: all timings measured at 1.5 V unless otherwise specified

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 80188		SAB 80188-1			
		min.	max.	min.	max.		
t_{DVCL}	Data in setup (A/D)	20	–	15	–	ns	–
t_{CLDX}	Data in hold (A/D)	10	–	8	–	ns	–
t_{ARYHCH}	Asynchronous ready (ARDY) active setup time [1]	20	–	15	–	ns	–
t_{ARYLCL}	ARDY inactive setup time	35	–	25	–	ns	–
t_{CHARYX}	ARDY hold time	15	–	15	–	ns	–
t_{ARYCHL}	Asynchronous ready inactive hold time	15	–	15	–	ns	–
t_{SRYCL}	Synchronous ready (SRDY) transition setup time	20	–	20	–	ns	–
t_{CLSRY}	SRDY transition hold time	15	–	15	–	ns	–
t_{HVCL}	HOLD setup time [1]	25	–	20	–	ns	–
t_{INVCH}	INTR, NMI, $\overline{\text{TEST}}$, TIMERIN, setup time [1]	25	–	25	–	ns	–
t_{INVCL}	DRQ0, DRQ1 setup time [1]	25	–	20	–	ns	–

[1] To guarantee recognition at next clock.

Master Interfaces Timing Responses

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 80188		SAB 80188-1			
		min.	max.	min.	max.		
t_{CLAV}	Address valid delay	5	55	5	50	ns	C_L = 20 to 200 pF all outp.
t_{CLAX}	Address hold time	10	–	10	–	ns	–
t_{CLAZ}	Address float delay	t_{CLAX}	35	t_{CLAX}	30	ns	–
t_{CHCZ}	Command lines float delay	–	45	–	40	ns	–
t_{CHCV}	Command lines valid delay (after float)	–	55	–	45	ns	–
t_{LHLL}	ALE width	t_{CLCL}-35	–	t_{CLCL}-30	–	ns	–
t_{CHLH}	ALE active delay	–	35	–	30	ns	–
t_{CHLL}	ALE inactive delay	–	35	–	30	ns	–
t_{LLAX}	Address hold to ALE inactive	t_{CHCL}-25	–	t_{CHCL}-20	–	ns	–
t_{CLDV}	Data valid delay	10	44	10	40	ns	–
t_{CLDOX}	Data hold time	10	–	10	–	ns	–
t_{WHDX}	Data hold after $\overline{WR}$	t_{CLCL}-40	–	t_{CLCL}-34	–	ns	–
t_{CVCTV}	Control active delay 1	10	70	5	56	ns	–
t_{CHCTV}	Control active delay 2	10	55	10	44	ns	–
t_{CVCTX}	Control inactive delay	5	55	5	44	ns	–
t_{CVDEX}	$\overline{DEN}$ inactive delay (non-write cycle)	10	70	10	56	ns	–
t_{AZRL}	Address float to $\overline{RD}$ active	0	–	0	–	ns	–
t_{CLRL}	$\overline{RD}$ active delay	10	70	10	56	ns	–
t_{CLRH}	$\overline{RD}$ inactive delay	10	55	10	44	ns	–
t_{RHAV}	$\overline{RD}$ inactive to address active	t_{CLCL}-40	–	t_{CLCL}-40	–	ns	–
t_{CLHAV}	HLDA valid delay	5	50	5	40	ns	–
t_{RLRH}	$\overline{RD}$ width	$2t_{CLCL}$-50	–	$2t_{CLCL}$-46	–	ns	–
t_{WLWH}	$\overline{WR}$ width	$2t_{CLCL}$-40	–	$2t_{CLCL}$-34	–	ns	–
t_{AVAL}	Address valid to ALE low	t_{CLCH}-25	–	t_{CLCH}-19	–	ns	–
t_{CHSV}	Status active delay	10	55	10	45	ns	–
t_{CLSH}	Status inactive delay	10	65	10	50	ns	–
t_{CLTMV}	Timer output delay	–	60	–	48	ns	100 pF max.
t_{CLRO}	Reset delay	–	60	–	48	ns	–
t_{CHQSV}	Queue status delay	–	35	–	28	ns	–
t_{CHDX}	Status hold time	10	–	10	–	ns	–
t_{AVCH}	Address valid to clock high	10	–	10	–	ns	–
t_{CLLV}	$\overline{LOCK}$ valid/invalid delay	5	65	5	60	ns	–

Chip Select Timing Responses

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 80188		SAB 80188-1			
		min.	max.	min.	max.		
t_{CLCSV}	Chip select active delay	–	66	–	45	ns	–
t_{CXCSX}	Chip select hold from command inactive	35	–	35	–	ns	–
t_{CHCSX}	Chip select inactive delay	5	35	5	32	ns	–

CLKIN Requirements

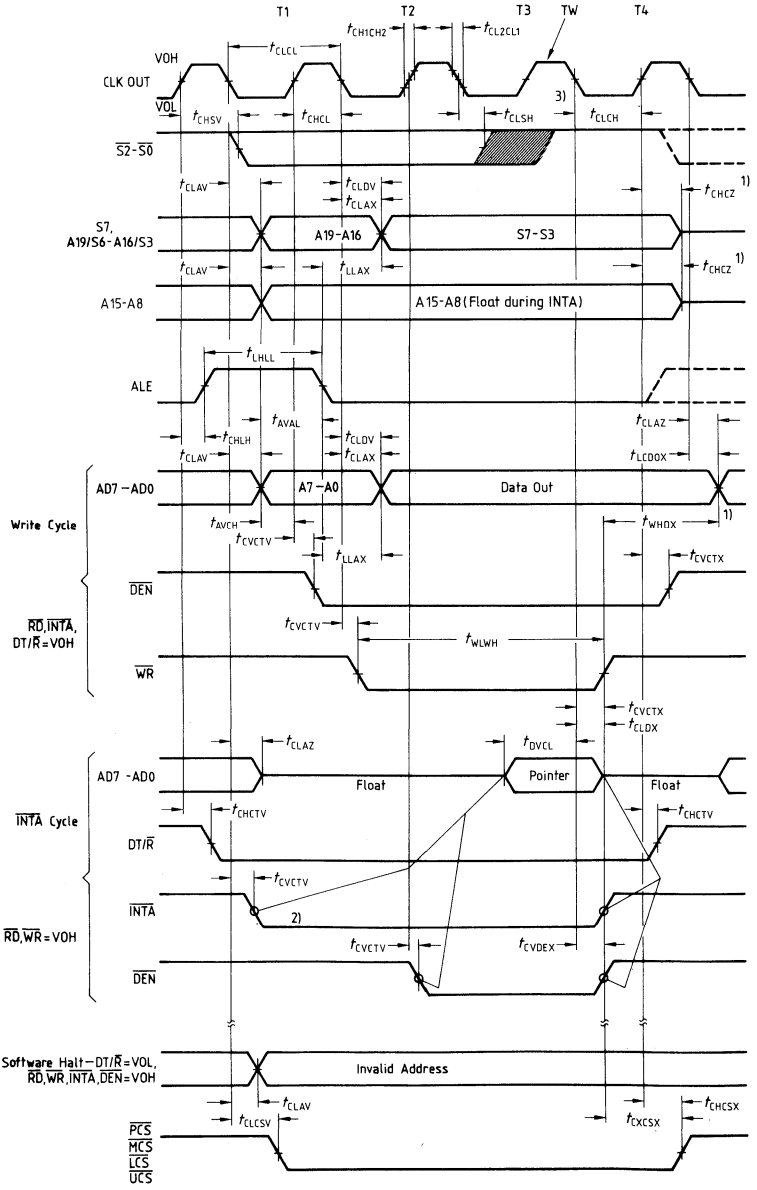
Symbol	Parameter	Limit values				Unit	Test condition
		SAB 80188		SAB 80188-1			
		min.	max.	min.	max.		
t_{CKIN}	CLKIN period	62.5	250	50	250	ns	–
t_{CKHL}	CLKIN fall time	–	10	–	10	ns	3.5 to 1.0 V
t_{CKLH}	CLKIN rise time	–	10	–	10	ns	1.0 to 3.5 V
t_{CLCK}	CLKIN low time	25	–	20	–	ns	1.5 V
t_{CHCK}	CLKIN high time	25	–	20	–	ns	1.5 V

CLKOUT Timing (200 pF load)

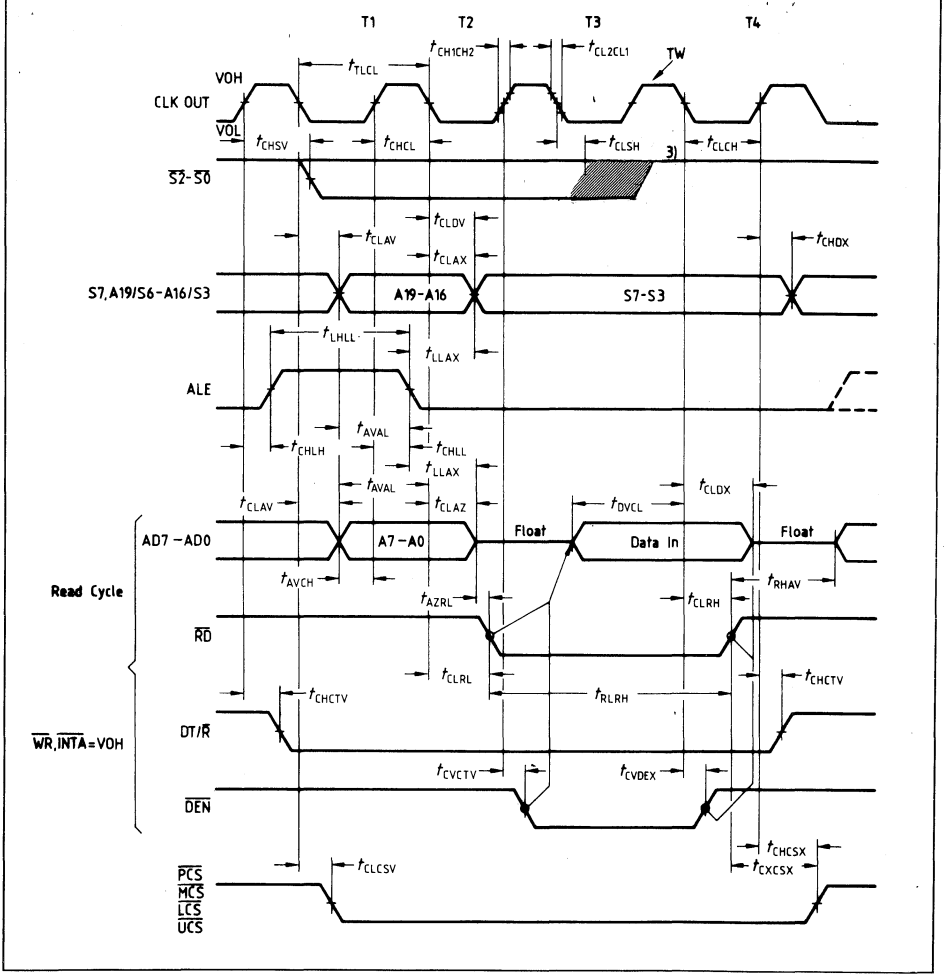
Symbol	Parameter	Limit values				Unit	Test condition
		SAB 80188		SAB 80188-1			
		min.	max.	min.	max.		
t_{CICO}	CLKIN to CLKOUT skew	–	50	–	25	ns	–
t_{CLCL}	CLKOUT period	125	500	100	500	ns	–
t_{CLCH}	CLKOUT low time	$1/2t_{CLCL}$-7.5	–	$1/2t_{CLCL}$-6.0	–	ns	1.5 V
t_{CHCL}	CLKOUT high time	$1/2t_{CLCL}$-7.5	–	$1/2t_{CLCL}$-6.0	–	ns	1.5 V
t_{CH1CH2}	CLKOUT rise time	–	15	–	12	ns	1.0 to 3.5 V
t_{CL2CL1}	CLKOUT fall time	–	15	–	12	ns	3.5 to 1.0 V

Waveforms

Major Cycle Timing



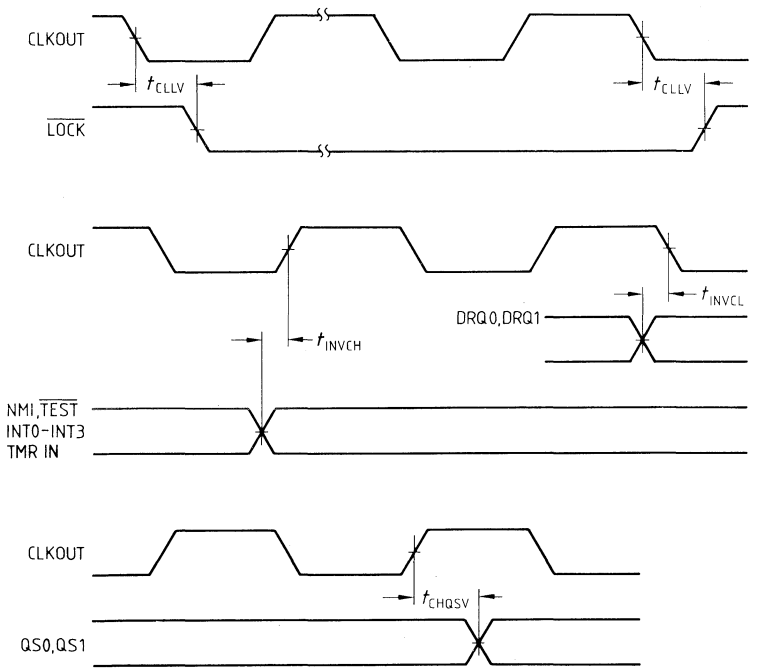
Major Cycle Timing (cont'd)



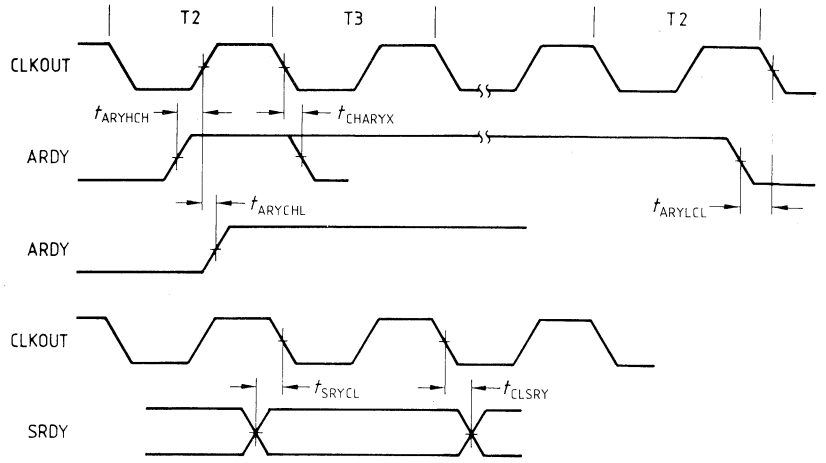
Notes

1. Following a write cycle, the local bus is tristated by the SAB 80188 only when the SAB 80188 enters a "hold acknowledge" state.
2. INTA occurs one clock later in iRMX mode.
3. Status inactive just prior to T4.

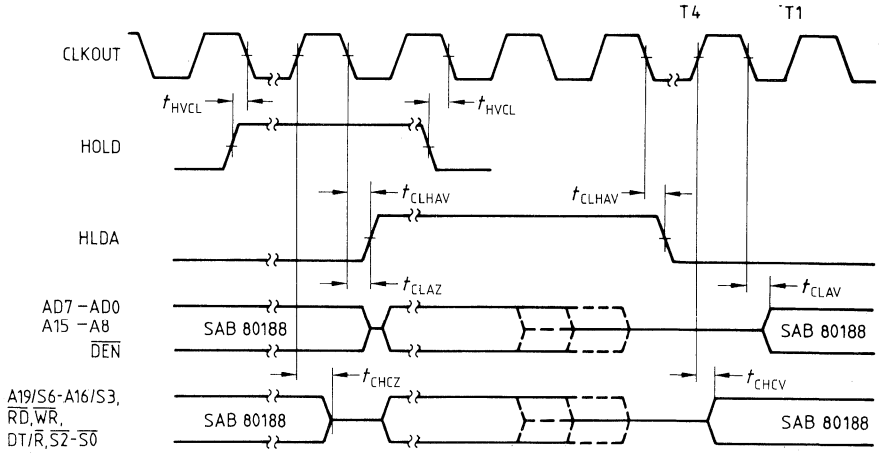
CLKOUT Timing Relationships



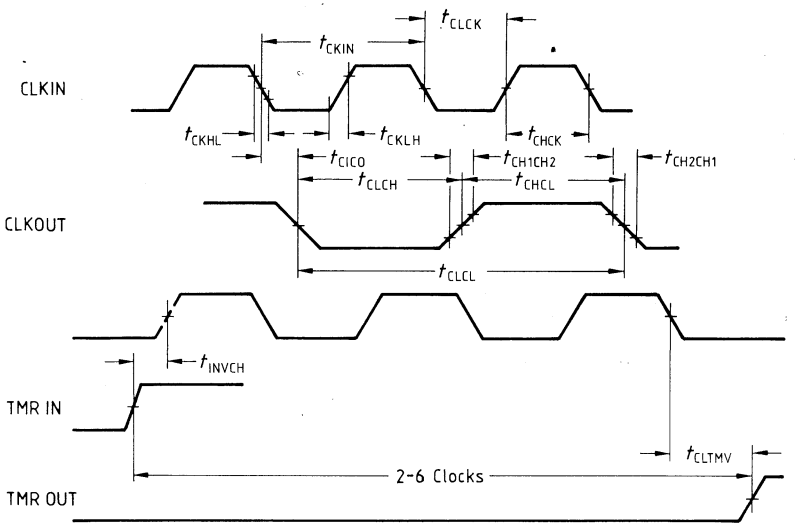
Ready Timing



HOLD-HLDA Timing

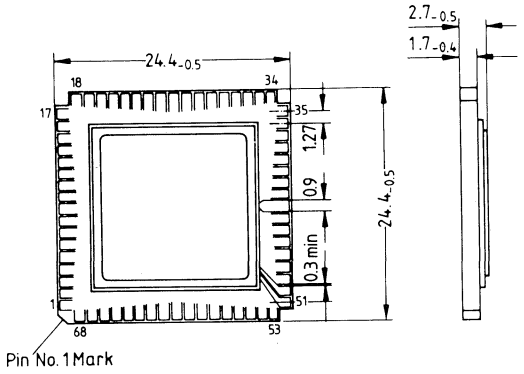


Timer Timing



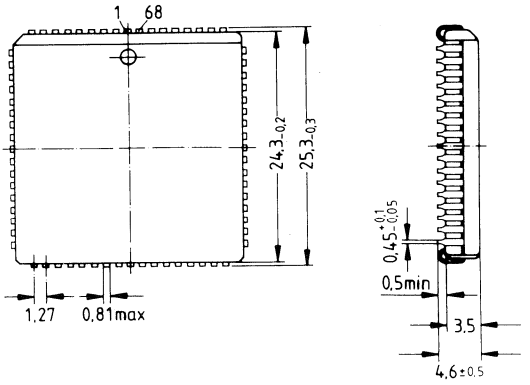
Package Outlines

Ceramic Package, CLCC, 68 Pins



Dimensions in mm

Plastic Package, PLCC, 68 Pins



Dimensions in mm

Ordering Information

Type	Ordering code	Description
SAB 80188-N	Q67120-C252	8-bit microprocessor, 8 MHz (PLCC)
SAB 80188-R	Q67120-C168	8-bit microprocessor, 8 MHz (CLCC)
SAB 80188-1-N	Q67120-C299	8-bit microprocessor, 10 MHz (PLCC)
SAB 80188-1-R	Q67120-C303	8-bit microprocessor, 10 MHz (CLCC)

16-Bit Microprocessors

SAB 8086
16-Bit Microprocessor

SAB 8086-2 8 MHz
SAB 8086-1 10 MHz

SAB 8086 5 MHz

- Direct addressing capability to 1 Mbyte of memory
- Assembly language compatible with SAB 8080 / SAB 8085
- 14 word by 16-bit register set with symmetrical operations
- 8 and 16-bit signed and unsigned arithmetic in binary or decimal including multiply and divide
- Bit, byte, word and block operations
- 24 operand addressing modes
- Clock rate up to 10 MHz (SAB 8086-1)
- Compatible with industry standard 8086
- In plastic and ceramic package

Figure 1 Pin Diagram

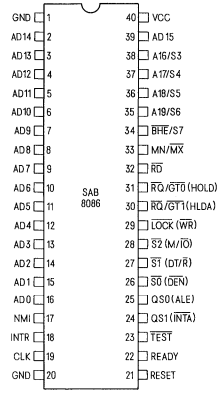


Figure 2 Pin Names

AD0–15	Address/Data	A16–19	Address
S0–2	Status	S3–7	Status
INTR	Interrupt Request	BHE	Bus High Enable
CLK	Clock	HOLD	Hold
QS0–1	Queue Status	HLDA	Hold Acknowledge
TEST	Test for Busy	WR	Write
READY	Ready	DT/R	Bus Driver Transmit/ Receive
RESET	Chip Reset		
MN/MX	Minimum/Maximum Mode	DEN	Bus Driver Enable
		ALE	Address Latch Enable
RD	Read	INTA	Interrupt Acknowledge
RQ/GT0–1	Request/Grant	NMI	Non-Maskable Interrupt
LOCK	Bus Lock		
M/IO	Memory/IO	GND	Ground
		VCC	+5V

SAB 8086 is a new generation, high-performance 16-bit microprocessor implemented in +5 V depletion load, N channel, silicon gate Siemens MYMOS technology, packaged in a 40-pin package. It is 100 percent compatible with the industry standard 8086. With features like string handling, 16-bit arithmetic with multiply and divide it significantly increases system performance. It is highly suited for multiprocessor applications in various configurations.

Pin Definitions and Functions

The following pin definitions are for SAB 8086 systems in **either minimum or maximum mode.** The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the SAB 8086 (without regard to additional bus buffers).

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>AD0–AD15</td><td>2–16
39</td><td>I/O</td><td>These lines constitute the time multiplexed memory I/O address (T1) and data (T2, T3, T4) bus. A0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D7 to D0. It is low during T1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A0 to condition chip select functions. These lines are active high and float to tristate OFF during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A16/S3
A17/S4
A18/S5
A19/S6</td><td>35–38</td><td>O</td><td>During T1 these are the four most significant address lines for memory operations. During I/O operations these lines are low. During memory and I/O operations, status information is available on these lines during T2, T3, TW and T4. The status of the interrupt enable flag bit (S5) is updated at the beginning of each CLK cycle.
A17/S4 and A16/S3 are encoded as follows:
<table>
<tr><th>A17/S4</th><th>A16/S3</th><th>Characteristics</th></tr>
<tr><td>0 (low)</td><td>0</td><td>Alternate Data</td></tr>
<tr><td>0</td><td>1</td><td>Stack</td></tr>
<tr><td>1 (high)</td><td>0</td><td>Code or None</td></tr>
<tr><td>1</td><td>1</td><td>Data</td></tr>
<tr><td>S6 is 0 (low)</td><td></td><td></td></tr>
</table>
This information indicates which relocation register is presently being used for data accessing.
These lines float to tristate OFF during local bus "hold acknowledge".</td></tr>
<tr><td>$\overline{BHE}$/S7</td><td>34</td><td>O</td><td>During T1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D15 to D8. Eight-bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is low during T1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S7 status information is available during T2, T3, and T4. The signal is active low, and floats to tristate OFF in "hold". It is low during T1 for the first interrupt acknowledge cycle.</td></tr>
<tr><td>$\overline{RD}$</td><td>32</td><td>O</td><td>Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the S2 pin. This signal is used to read devices which reside on the SAB 8086 local bus. $\overline{RD}$ is active low during T2, T3 and TW of any read cycle, and is guaranteed to remain high in T2 until the SAB 8086 local bus has floated.
This signal floats to tristate OFF in "hold acknowledge".</td></tr>
</table>

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
READY	22	I	READY is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory I/O is synchronized by the SAB 8284B clock generator to form READY. This signal is active high. The SAB 8086 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.
INTR	18	I	Interrupt request is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software reseting the interrupt enable bit. INTR is internally synchronized. This signal is active high.
$\overline{\text{TEST}}$	23	I	The $\overline{\text{TEST}}$ input is examined by the "wait" instruction. If the $\overline{\text{TEST}}$ input is low execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	Non-maskable interrupt is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a low to high initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET causes the processor to immediately terminate its present activity. The signal must be active high for at least four clock cycles. It restarts execution, as described in the Instruction Set Description, when RESET returns low. RESET is internally synchronized.
CLK	19	I	The clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
MN/$\overline{\text{MX}}$	33	I	Minimum/Maximum: indicates what mode the processor is to operate in. The two modes are discussed in the following sections.
VCC	40		POWER SUPPLY (+5V)
GND	1, 20		GROUND (0V)

Pin Definitions and Functions (cont'd)

The following pin definitions are for the SAB 8086/8288 system in **maximum mode** (i.e. MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described; all other pin functions are as already described.

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{S2}$, $\overline{S1}$, $\overline{S0}$</td><td>26–28</td><td>O</td><td>These status lines are encoded as follows:
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Characteristics</th></tr>
<tr><td>0 (low)</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1 (high)</td><td>0</td><td>0</td><td>Code Access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table>
Status is active during T4, T1, and T2 and is returned to the passive state (1,1,1) during T3 or during TW when READY is high. This status is used by the SAB 8288A bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or TW is used to indicate the end of a bus cycle.
These signals float to tristate OFF in "hold acknowledge".</td></tr>
<tr><td>$\overline{RQ}$/$\overline{GT0}$, $\overline{RQ}$/$\overline{GT1}$</td><td>30–31</td><td>I/O</td><td>The request/grant pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}$/$\overline{GT0}$ having higher priority than $\overline{RQ}$/$\overline{GT1}$. $\overline{RQ}$/$\overline{GT}$ has an internal pullup resistor so may be left unconnected. The request/grant sequence is as follows (see figure 14):
1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the SAB 8086 (pulse1).
2. During the CPU's next T4 or T1 a pulse 1 CLK wide from the SAB 8086 to the requesting master (pulse 2) indicates that the SAB 8086 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge".
3. A pulse 1 CLK wide from the requesting master indicates to the SAB 8086 (pulse 3) that the "hold" request is about to end and that the SAB 8086 can reclaim the local bus at the next CLK.
Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active low.
If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met:
1. Request occurs on or before T2.
2. Current cycle is not the low byte of a word (on an odd address).
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.</td></tr>
</table>

Pin Definitions and Functions (cont'd)

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{\text{LOCK}}$</td><td>29</td><td>O</td><td>The $\overline{\text{LOCK}}$ output indicates that other system bus masters are not to gain control of the system bus while $\overline{\text{LOCK}}$ is active low. The $\overline{\text{LOCK}}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active low, and floats to tristate OFF in "hold acknowledge".</td></tr>
<tr><td>QS1, QS0</td><td>24–25</td><td>O</td><td>QS1 and QS0 provide status to allow external tracking of the internal SAB 8086 instruction queue.
<table>
<tr><th>QS1</th><th>QS0</th><th>Characteristics</th></tr>
<tr><td>0 (low)</td><td>0</td><td>No Operation</td></tr>
<tr><td>0</td><td>1</td><td>First Byte of Op Code from Queue</td></tr>
<tr><td>1 (high)</td><td>0</td><td>Empty the Queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent Byte from Queue</td></tr>
</table>
The queue status is valid during the CLK cycle after which the queue operation is performed.</td></tr>
</table>

Pin Definitions and Functions (cont'd)

The following pin definitions are for the SAB 8086 **minimum mode** (i. e. MN/$\overline{MX}$ = VCC). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described before.

Symbol	Pin	Input (I) Output (O)	Function
M/$\overline{IO}$	28	O	This status line is logically equivalent to S 2 in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (M = high, $\overline{IO}$ = low). M/$\overline{IO}$ floats to tristate OFF in local bus "hold acknowledge".
$\overline{WR}$	29	O	Write strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T2, T3 and TW of any write cycle. It is active low, and floats to tristate OFF in local bus "hold acknowledge".
$\overline{INTA}$	24	O	$\overline{INTA}$ is used as a read strobe for interrupt acknowledge cycles. It is active low during T2, T3 and TW of each interrupt acknowledge cycle.
ALE	25	O	Address latch enable is provided by the processor to latch the address into the SAB 8282A/SAB 8283A address latch. It is a high pulse active during T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	Data transmit/receive is needed in minimum system that desires to use a SAB 8286A/SAB 8287A data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/$\overline{R}$ is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for M/$\overline{IO}$. (T=high, $\overline{R}$=low). This signal floats to tristate OFF in local bus "hold acknowledge".
$\overline{DEN}$	26	O	Data enable is provided as an output enable for the SAB 8286A/SAB 8287A in a minimum system which uses the transceiver. $\overline{DEN}$ is active low during each memory and I/O access and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle it is active from the middle of T2 until the middle of T4, while for a write cycle it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ floats to tristate OFF in local bus "hold acknowledge".
HOLD HLDA	30–31	I O	HOLD indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active high. The processor receiving the "hold" request will issue HLDA (high) as an acknowledgement in the middle of T4 or T1. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being low, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time. The same rules as for $\overline{RQ}$/$\overline{GT}$ apply regarding when the local bus will be released.

Figure 3 Functional Block Diagram

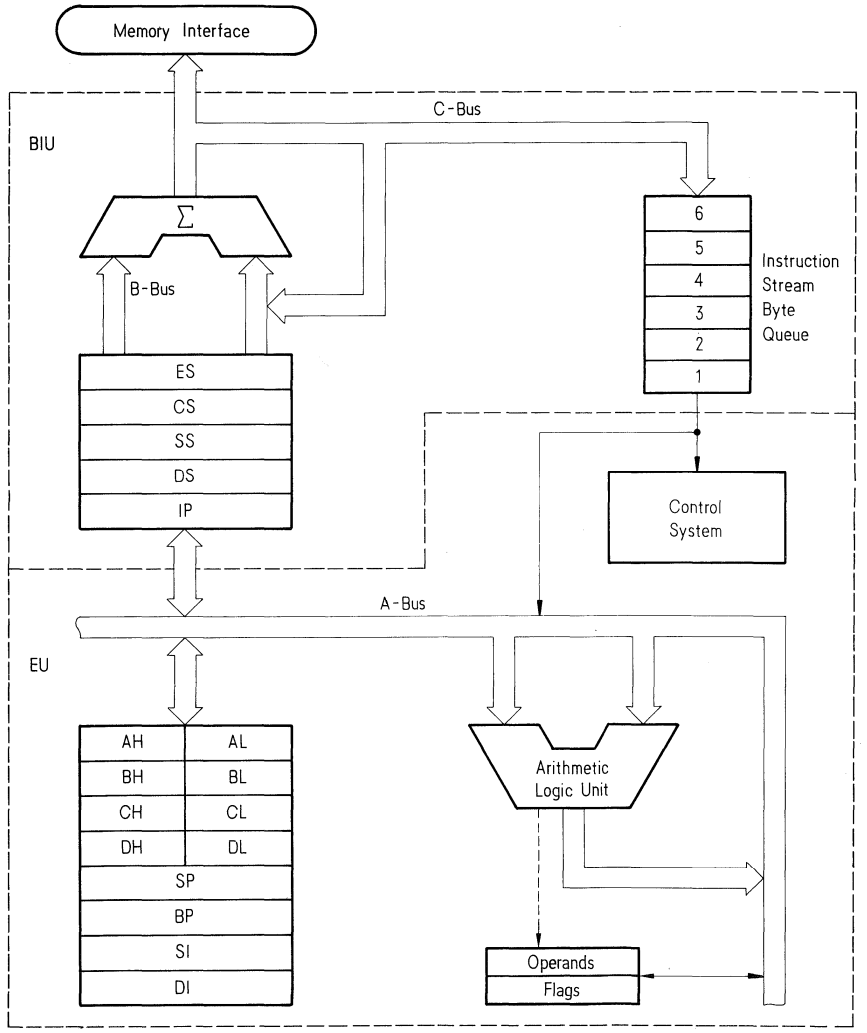
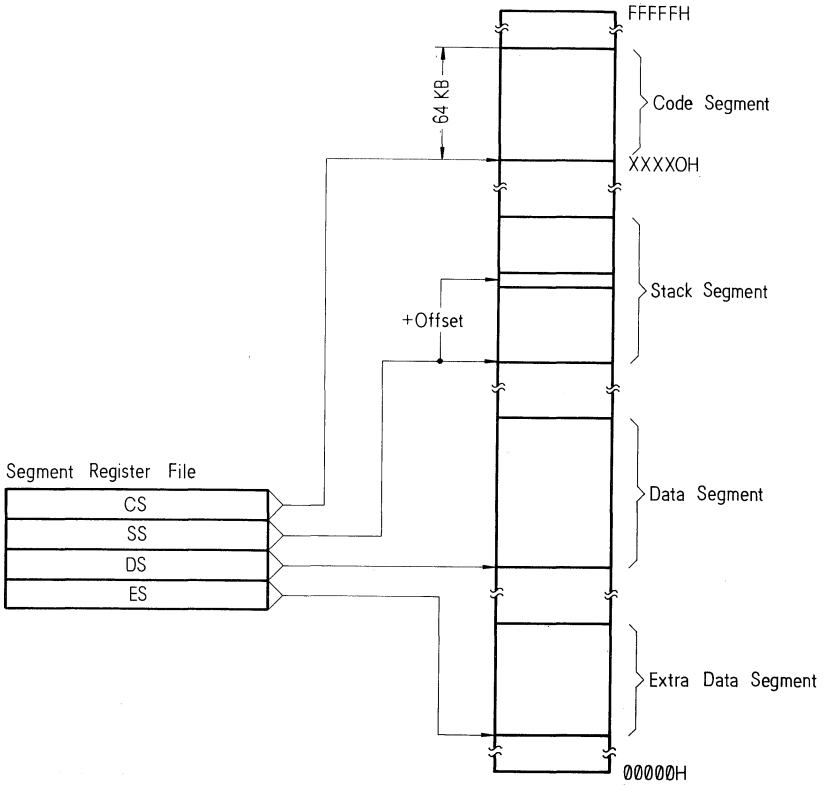


Figure 4 Memory Organization



Functional Description

The internal functions of the SAB 8086 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the block diagram of figure 3.

The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces „dead time" on the memory bus.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is logically organized as a linear array of 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory can further be logically divided into code, data, alternate data, and stack segments of up to 64 Kbytes each, with each segment falling on 16-byte boundaries (see figure 4).

Minimum and Maximum Modes

The requirements for supporting minimum and maximum SAB 8086 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the SAB 8086 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration.

The definition of a certain subset of the pins changes dependent on the condition of the strap pin.

When MN/$\overline{MX}$ pin is strapped to GND, the SAB 8086 treats pins 24 through 31 in maximum mode. An SAB 8288A bus controller interprets status information coded into $\overline{S0}$, $\overline{S1}$, $\overline{S2}$ to generate bus timing and control signals.

When the MN/$\overline{MX}$ pin is strapped to VCC, the SAB 8086 generates bus control signals itself on pins 24 through 31, as shown in parentheses in figure 1.

Bus Operation

The SAB 8086 has a combined address and data bus commonly referred to as a time multiplexed bus.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4 (see figure 5). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "wait" states (TW) are inserted between T3 and T4. Each inserted wait state is of the same duration as a CLK cycle. Periods can occur between SAB 8086 bus cycles. These are referred to as "idle" states (Ti) or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T1 of any bus cycle the ALE (Address Latch Enable) signal is emitted (by either the processor or the SAB 8288A bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

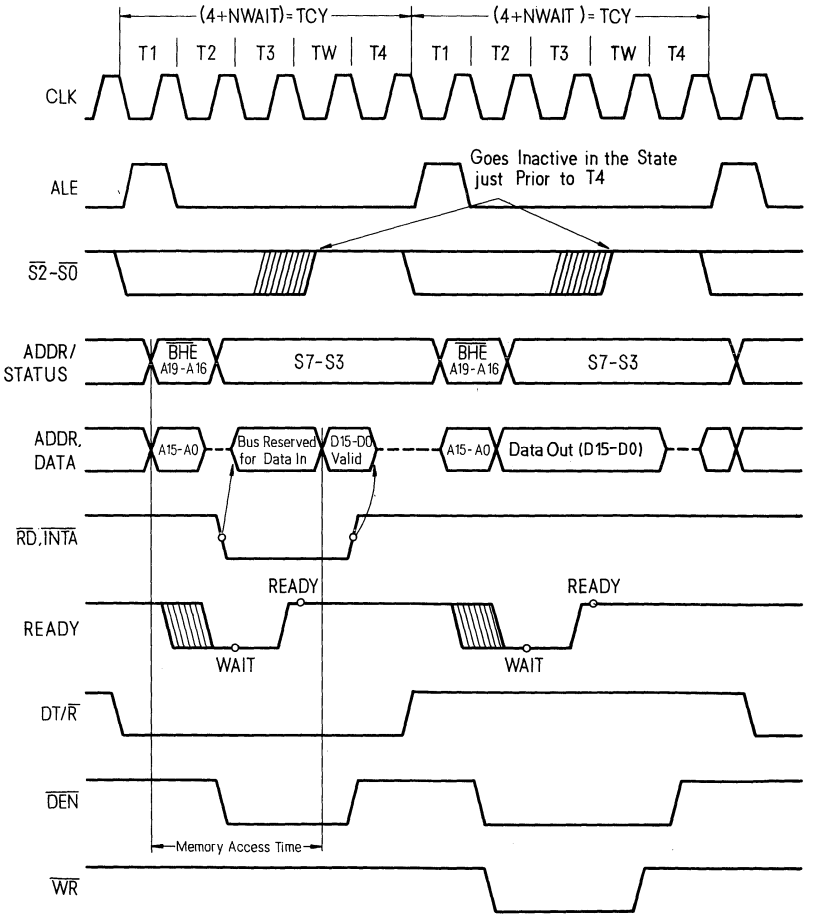
$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (Low)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (High)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S3 through S7 are multiplexed with high-order address bits and the $\overline{BHE}$ signal, and are therefore valid during T2 through T4. S3 and S4 indicate which segment register (see Instruction Set Description) was used for this bus cycle in forming the address, according to the following table:

S4	S3	Characteristics
0 (Low)	0	Alternate Data (extra segment)
0	1	Stack
1 (High)	0	Code or None
1	1	Data

S5 is a reflection of the PSW interrupt enable bit. S6 = 0 and S7 is a spare status bit.

Figure 5 Basic System Timing



I/O Addressing

In the SAB 8086, I/O operations can address up to a maximum of 64 K I/O byte registers or 32 K I/O word registers.
The I/O address appears in the same format as the memory address on bus lines A15 to A0. The address lines A19 to A16 are zero in I/O operations.
The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

System Components

SAB 8282A	Octal Latch
SAB 8283A	Octal Latch (inverting)
SAB 8284B	Clock Generator and Driver
SAB 8286A	Octal Bus Transceiver
SAB 8287A	Octal Bus Transceiver (inverting)
SAB 8288A	Bus Controller
SAB 8289	Bus Arbiter
SAB 8259A	Programmable Interrupt Controller

Typical Applications

SAB 8086 is a general-purpose 16-bit microprocessor which can be used for applications ranging from process control to data processing. Figures 6 and 7 show typical system configurations for SAB 8086 familiy components.

Figure 6 Minimum Mode SAB 8086 Typical System Configuration

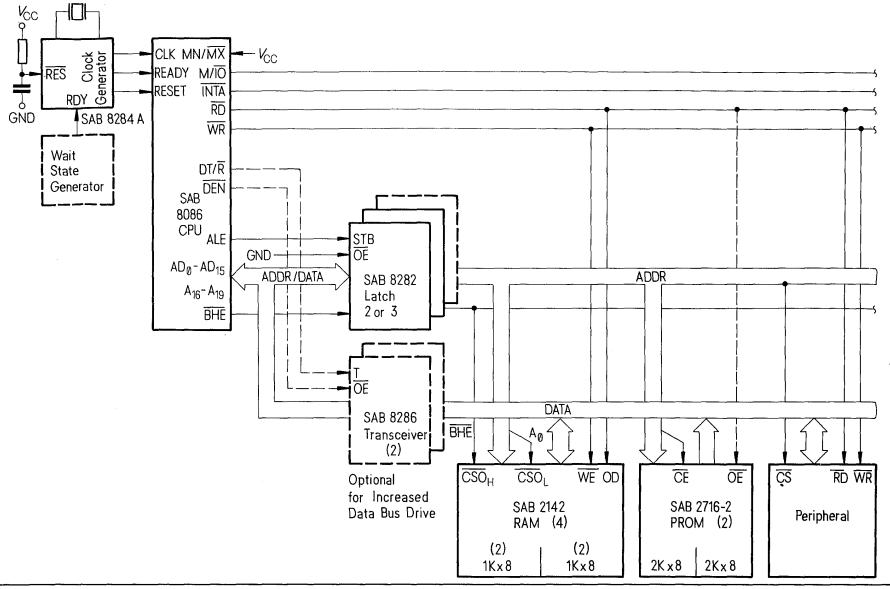
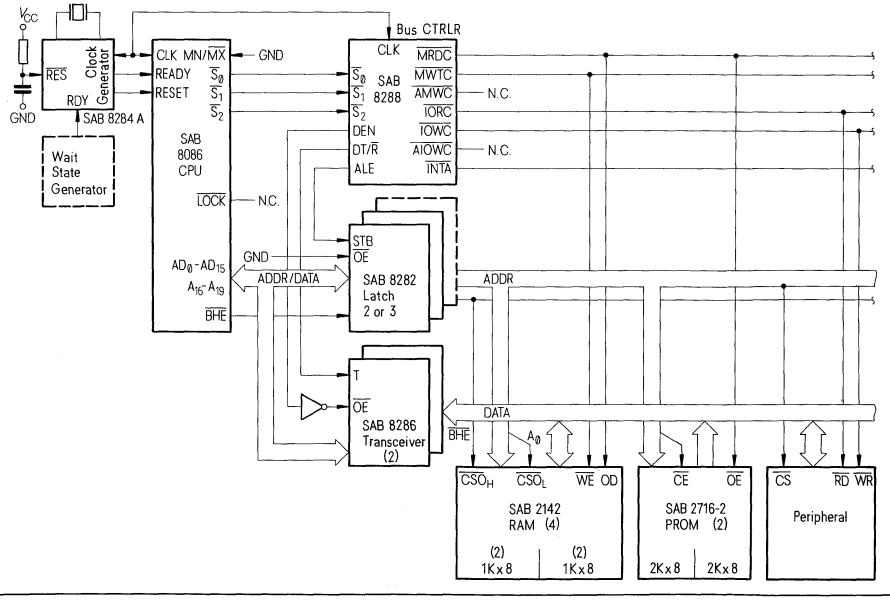


Figure 7 Maximum Mode SAB 8086 Typical System Configuration



Instruction Set Summary

Data Transfer

MOV = Move:	**76543210**	**76543210**	**76543210**	**76543210**
Register / memory to / from register	100010dw	mod reg r/m		
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1
Immediate to register	1011w reg	data	data if w=1	
Memory to accumulator	1010000w	addr-low	addr-high	
Accumulator to memory	1010001w	addr-low	addr-high	
Register/memory to segment register	10001110	mod 0 reg r/m		
Segment register to register/memory	10001100	mod 0 reg r/m		
PUSH = Push:				
Register/memory	11111111	mod 110 r/m		
Register	01010 reg			
Segment register	000 reg 110			
POP = Pop:				
Register/memory	10001111	mod 000 r/m		
Register	01011 reg			
Segment register	000 reg 111			
XCHG = Exchange:				
Register/memory with register	1000011w	mod reg r/m		
Register with accumulator	10010 reg			
IN = Input from:				
Fixed port	1110010w	port		
Variable port	1110110w			

OUT = Output to:	76543210	76543210	76543210	76543210
Fixed port	1110011w	port		
Variable port	1110111w			
XLAT = Translate byte to AL	11010111			
LEA = Load EA to register	10001101	mod reg r/m		
LDS = Load pointer to DS	11000101	mod reg r/m		
LES = Load pointer to ES	11000100	mod reg r/m		
LAHF = Load AH with flags	10011111			
SAHF = Store AH into flags	10011110			
PUSHF = Push flags	10011100			
POPF =Pop flags	10011101			

Arithmetic
ADD = Add:

Reg./memory with register to either	000000dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s:w=01
Immediate to accumulator	0000010w	data	data if w=1	

ADC = Add with carry:

Reg./memory with register to either	000100dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s:w=01
Immediate to accumulator	0001010w	data	data if w=1	

INC = Increment:

Register/memory	1111111w	mod 000 r/m
Register	01000reg	
AAA = ASCII adjust for add	00110111	
DAA = Decimal adjust for add	00100111	

SUB = Subtract:	76543210	76543210	76543210	76543210
Reg./memory and register to either	001010dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s:w=01
Immediate from accumulator	0010110w	data	data if w=1	

SBB = Subtract with borrow:				
Reg./memory and register to either	000110dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s:w=01
Immediate from accumulator	0001110w	data	data if w=1	

DEC = Decrement:	76543210	76543210	76543210	76543210
Register/memory	1111111w	mod 001 r/m		
Register	01001reg			
NEG = Change sign	1111011w	mod 011 r/m		

CMP = Compare:				
Register/memory and register	001110dw	mod reg r/m		
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s:w=01
Immediate with accumulator	0011110w	data	data if w=1	
AAS = ASCII adjust for subtract	00111111			
DAS = Decimal adjust for subtract	00101111			
MUL = Multiply (unsigned)	1111011w	mod 100 r/m		
IMUL = Integer multiply (signed)	1111011w	mod 101 r/m		
AAM = ASCII adjust for multiply	11010100	00001010		
DIV = Divide (unsigned)	1111011w	mod 110 r/m		
IDIV = Integer divide (signed)	1111011w	mod 111 r/m		
AAD = ASCII adjust for divide	11010101	00001010		
CBW = Convert byte to word	10011000			
CWD = Convert word to double word	10011001			

Logic	76543210	76543210	76543210	76543210
NOT = Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL = Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR = Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR = Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL = Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR = Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL = Rotate through carry flag left	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR = Rotate through carry flag right	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND = And:				
Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w=1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w=1	
TEST = And function to flags, no result:				
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w=1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w=1	
OR = Or:				
Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w=1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w=1	
XOR = Exclusive Or:				
Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w=1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w=1	

String Manipulation	**76543210**	**76543210**	**76543210**
REP = Repeat	1111001z		
MOVS = Move byte/word	1010010w		
CMPS = Compare byte/word	1010011w		
SCAS = Scan byte/word	1010111w		
LODS = Load byte/word to AL/AX	1010110w		
STOS = Store byte/word from AL/A	1010101w		

Control Transfer

CALL = Call:			
Direct within segment	11101000	disp-low	disp-high
Indirect within segment	11111111	mod 010 r/m	
Direct intersegment	10011010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 011 r/m	

JMP = Unconditional jump:			
Direct within segment	11101001	disp-low	disp-high
Direct within segment short	11101011	disp	
Indirect within segment	11111111	mod 100 r/m	
Direct intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 101 r/m	

RET = Return from CALL:	**76543210**	**76543210**	**76543210**
Within segment	11000011		
Within seg. adding immediate to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment adding immediate to SP	11001010	data-low	data-high
JE/JZ = Jump on equal/zero	01110100	disp	
JL/JNGE = Jump on less/not greater or equal	01111100	disp	
JLE/JNG = Jump on less or equal/not greater	01111110	disp	
JB/JNAE = Jump on below/not above or equal	01110010	disp	
JBE/JNA = Jump on below or equal/ not above	01110110	disp	
JP/JPE = Jump on parity/parity even	01111010	disp	
JO = Jump on overflow	01110000	disp	
JS = Jump on sign	01111000	disp	
JNE/JNZ = Jump on not equal/not zero	01110101	disp	
JNL/JGE = Jump on not less/greater or equal	01111101	disp	
JNLE/JG = Jump on not less or equal/ greater	01111111	disp	
JNB/JAE = Jump on not below/above or equal	01110011	disp	
JNBE/JA = Jump on not below or equal/above	01110111	disp	
JNP/JPO = Jump on not parity/parity odd	01111011	disp	
JNO = Jump on not overflow	01110001	disp	
JNS = Jump on not sign	01111001	disp	
LOOP = Loop CX times	11100010	disp	
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp	
JCXZ = Jump on CX zero	11100011	disp	

INT = **Interrupt**	**76543210**	**76543210**
Type specified	11001101	type
Type 3	11001100	
INTO = Interrupt on overflow	11001110	
IRET = Interrupt return	11001111	

Processor Control

CLC = Clear carry	11111000	
CMC = Complement carry	11110101	
STC = Set carry	11111001	
CLD = Clear direction	11111100	
STD = Set direction	11111101	
CLI = Clear interrupt	11111010	
STI = Set interrupt	11111011	
HLT = Halt	11110100	
WAIT = Wait	10011011	
ESC = Escape (to external device)	11011xxx	mod x x x r/m
LOCK = Bus lock prefix	11110000	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction
if s:w = 01 then 16-bits of immediate data from the operand
it s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparsion with ZF FLAG

Segment Override Prefix

0 0 1 reg 1 1 0

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp high is absent
if mod = 10 then DISP = disp-high: disp low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) +DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

* except if mod = 00 and r/m = 110 then EA = disp-high:disp-low.

REG is assigned according to the following table

16-bit (w=1)	8-bit (w=0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instruction which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Absolute Maximum Ratings *)

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−1.0 to +7V
Power dissipation	2.5 W

DC Characteristics

SAB 8086: TA = 0 to 70°C, VCC = 5 V ±10%
SAB 8086-1/8086-2: TA = 0 to 70°C, VCC = 5 V ±5%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
VIL	Input low voltage	−0.5	+0.8	V	–
VIH	Input high voltage	2.0	VCC+0.5		
VOL	Output low voltage	–	0.45		IOL = 2.5 mA
VOH	Output high voltage	2.4	–		IOH = −400 µA
ICC	Power supply current SAB 8086 SAB 8086-2 SAB 8086-1	–	 340 350 360	mA	TA = 25°C
ILI	Input leakage current		±10	µA	0V ≤ VIN ≤ VCC
ILO	Output leakage current				0.45 V ≤ VOUT ≤ VCC
VCL	Clock input low voltage	−0.5	+0.6	V	–
VCH	Clock input high voltage	3.9	VCC+1.0		
CIN	Capacitance of input buffer (all inputs except AD0 to AD15, $\overline{RQ}/\overline{GT}$)	–	15	pF	fc = 1 MHz
CIO	Capacitance of I/O buffer (AD0 to AD15, $\overline{RQ}/\overline{GT}$)				

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics for SAB 8086/8086-2

SAB 8086: TA = 0 to 70°C, VCC = 5 V ± 10%
SAB 8086-2: TA = 0 to 70°C, VCC = 5 V ± 5%

Minimum Complexity System (figures 8, 9, 12, 15)
Timing Requirements

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 8086		SAB 8086-2			
		min.	max.	min.	max.		
TCLCL	CLK cycle period SAB 8086	200	500	125	500	ns	–
TCLCH	CLK low time	118	–	68	–		
TCHCL	CLK high time	69		44			
TCH1CH2	CLK rise time	–	10	–	10		from 1.0 to 3.5V
TCL2CL1	CLK fall time						from 3.5 to 1.0V
TDVCL	Data in setup time	30	–	20	–		–
TCLDX	Data in hold time	10		10			
TR1VCL	RDY setup time into SAB 8284A [1] [2]	35		35			
TCLR1X	RDY hold time into SAB 8284A [1] [2]	0		0			
TRYHCH	READY setup time into SAB 8086	118		68			
TCHRYX	READY hold time into SAB 8086	30		20			
TRYLCL	READY inactive to CLK [3]	−8		−8			
THVCH	HOLD setup time	35		20			
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ setup time [2]	30		15			
TILIH	Input rise time (except CLK)	–	20	–	20		from 0.8 to 2.0V
TIHIL	Input fall time (except CLK)		12		12		from 2.0 to 0.8V

[1]) Signal at SAB 8284B shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T2 state (8 ns into T3).

Timing Responses

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 8086		SAB 8086-2			
		min.	max.	min.	max.		
TCLAV	Address valid delay	10	110	10	60	ns	CL = 20 to 100 pF for all SAB 8086 outputs (in addition to SAB 8086 self-load)
TCLAX	Address hold time		–		–		
TCLAZ	Address float delay	TCLAX	80	TCLAX	50		
TLHLL	ALE width	TCLCH–20	–	TCLCH–10	–		
TCLLH	ALE active delay	–	80	–	50		
TCHLL	ALE inactive delay		85		55		
TLLAX	Address hold time to ALE inactive	TCHCL–10	–	TCHCL–10	–		
TCLDV	Data valid delay	10	110	10	60		
TCHDX	Data hold time		–		–		
TWHDX	Data hold time after WR	TCLCH–30		TCLCH–30			
TCVCTV	Control active delay 1	10	110	10	70		
TCHCTV	Control active delay 2				60		
TCVCTX	Control inactive delay				70		
TAZRL	Address float to READ active	0	–	0	–		
TCLRL	$\overline{RD}$ active delay	10	165	10	100		
TCLRH	$\overline{RD}$ inactive delay		150		80		
TRHAV	$\overline{RD}$ inactive to next address active	TCLCL–45	–	TCLCL–40	–		
TCLHAV	HLDA valid delay	10	160	10	100		
TRLRH	$\overline{RD}$ width	2TCLCL–75	–	2TCLCL–50	–		
TWLWH	$\overline{WR}$ width	2TCLCL–60		2TCLCL–40			
TAVAL	Address valid to ALE low	TCLCH–60		TCLCH–40			
TOLOH	Output rise time	–	20	–	20		from 0.8 to 2.0V
TOHOL	Output fall time		12		12		from 2.0 to 0.8V

Maximum Mode System (using SAB 8288A bus controller) (figures 10 to 14)
Timing Requirements

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 8086		SAB 8086-2			
		min.	max.	min.	max.		
TCLCL	CLK cycle period SAB 8086	200	500	125	500	ns	–
TCLCH	CLK low time	118	–	68	–		
TCHCL	CLK high time	69		44			
TCH1CH2	CLK rise time	–	10	–	10		from 1.0 to 3.5V
TCL2CL1	CLK fall time						from 3.5 to 1.0V
TDVCL	Data in setup time	30	–	20	–		–
TCLDX	Data in hold time	10		10			
TR1VCL	RDY setup time into SAB 8284A [1] [2]	35		35			
TCLR1X	RDY hold time into SAB 8284A [1] [2]	0		0			
TRYHCH	READY setup time into SAB 8086	118		68			
TCHRYX	READY hold time into SAB 8086	30		20			
TRYLCL	READY inactive to CLK [4]	−8		−8			
TINVCH	Setup time for recognition ($\overline{INTR}$, NMI, $\overline{TEST}$) [2]	30		15			
TGVCH	$\overline{RQ}/\overline{GT}$ setup time						
TCHGX	$\overline{RQ}$ hold time into SAB 8086	40		30			
TILIH	Input rise time (except CLK)	–	20	–	20		from 0.8 to 2.0V
TIHIL	Input fall time (except CLK)		12		12		from 2.0 to 0.8V

[1]) Signal at SAB 8284B or SAB 8288A shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T3 and wait states.
[4]) Applies only to T2 state (8 ns into T3).

Timing Responses

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 8086		SAB 8086-2			
		min.	max.	min.	max.		
TCLML	Command active delay [1])	10	35	10	35	ns	CL = 20 to 100 pF for all SAB 8086 outputs (in addition to SAB 8086 self-load)
TCLMH	Command inactive delay [1])						
TRYHSH	READY active to status passive [3])	–	110	–	65		
TCHSV	Status active delay	10		10	60		
TCLSH	Status inactive delay		130		70		
TCLAV	Address valid delay		110		60		
TCLAX	Address hold time		–		–		
TCLAZ	Address float delay	TCLAX	80	TCLAX	50		
TSVLH	Status valid to ALE high [1])	–	20	–	20		
TSVMCH	Status valid to MCE high [1])						
TCLLH	CLK low to ALE valid [1])						
TCLMCH	CLK low to MCE high [1])						
TCHLL	ALE inactive delay [1])	4	15	4	15		
TCLDV	Data valid delay	10	110	10	60		
TCHDX	Data hold time		–		–		
TCVNV	Control active delay [1])	5	45	5	45		
TCVNX	Control inactive delay [1])	10		10			

[1]) Signal at SAB 8284B or SAB 8288A shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T3 and wait states.
[4]) Applies only to T2 state (8 ns into T3).

Timing Responses (cont'd)

Symbol	Parameter	Limit values				Unit	Test condition
		SAB 8086		SAB 8086-2			
		min.	max.	min.	max.		
TAZRL	Address float to READ active	0	–	0	–		
TCLRL	$\overline{RD}$ active delay	10	165	10	100	ns	CL= 20 to 100 pF for all SAB 8086 outputs (in addition to SAB 8086 self-load)
TCLRH	$\overline{RD}$ inactive delay		150		80		
TRHAV	$\overline{RD}$ inactive to next address active	TCLCL–45	–	TCLCL–40	–		
TCHDTL	Direction control active delay [1])	–	50	–	50		
TCHDTH	Direction control inactive delay [1])		30		30		
TCLGL	$\overline{GT}$ active delay	0	85	0	50		
TCLGH	$\overline{GT}$ inactive delay						
TRLRH	$\overline{RD}$ width	2TCLCL–75	–	2TCLCL–50	–		
TOLOH	Output rise time	–	20	–	20		from 0.8 to 2.0V
TOHOL	Output fall time		12		12		from 2.0 to 0.8V

[1]) Signal at SAB 8284B or SAB 8288A shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T3 and wait states.
[4]) Applies only to T2 state (8 ns into T3).

AC Characteristics for SAB 8086-1

TA = 0 to 70°C, VCC = 5V ± 5%

Minimum Complexity System (figures 8, 9, 12, 15)
Timing Requirements (preliminary)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCLCL	CLK cyde period	100	500	ns	–
TCLCH	CLK low time	53	–		
TCHCL	CLK high time	39			
TCH1CH2	CLK rise time	–	10		from 1.0 to 3.5V
TCL1CL2	CLK fall time				from 3.5 to 1.0V
TDVCL	Data in setup time	5	–		–
TCLDX	Data in hold time	10			
TR1VCL	RDY setup time into SAB 8284A[1)2)]	35			
TCLR1X	RDY hold time into SAB 8284A[1)2)]	0			
TRYHCH	READY setup time into SAB 8086	53			
TCHRYX	READY hold time into SAB 8086	20			
TRYLCL	READY inactive to CLK[3)]	–10			
THVCH	HOLD setup time	20			
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ setup time [2)]	15			
TILIH	Input rise time (except CLK)	–	20		from 0.8 to 2.0V
TILHIL	Input fall time (except CLK)		12		from 2.0 to 0.8V

[1)] Signal at SAB 8284B shown for reference only.
[2)] Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3)] Applies only to T2 state (8 ns into T3).

Timing Responses SAB 8086-1 (preliminary)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCLAV	Address valid delay	10	50	ns	CL = 20 to 100 pF for all SAB 8086 outputs (in addition to SAB 8086 self-load)
TCLAX	Address hold time		–		
TCLAZ	Address float delay		40		
TLHLL	ALE width	TCLCH-10	–		
TCLLH	ALE active delay	–	40		
TCHLL	ALE inactive delay		45		
TLLAX	Address hold time to ALE inactive	TCHCL-10	–		
TCLDV	Data valid delay	10	50		
TCHDX	Data hold time		–		
TWHDX	Data hold time after WR	TCLCH-25			
TCVCTX	Control active delay 1	10	50		
TCHCTV	Control active delay 2		45		
TCVCTX	Control inactive delay		50		
TAZRL	Address float to READ active	0	–		
TCLRL	$\overline{RD}$ active delay	10	70		
TCLRH	$\overline{RD}$ inactive delay		60		
TRHAV	$\overline{RD}$ inactive to next address active	TCLCL-35	–		
TCLHAV	HLDA valid delay	10	60		
TRLRH	$\overline{RD}$ width	2TCLCL-40	–		
TWLWH	$\overline{WR}$ width	2TCLCL-35			
TAVAL	Address valid to ALE low	TCLCH-35			
TOLOH	Output rise time	–	20		from 0.8 to 2.0V
TOHOL	Output fall time		12		from 2.0 to 0.8V

Maximum Mode System (using SAB 8288A bus controller) (figures 10-14)
Timing Requirements SAB 8086-1 (preliminary)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCLCL	CLK cycle period	100	500	ns	
TCLCH	CLK low time	53	–		–
TCHCL	CLK high time	39			
TCH1CH2	CLK rise time	–	10		from 1.0 to 3.5V
TCL2CL1	CLK fall time				from 3.5 to 1.0V
TDVCL	Data in setup time	5	–		
TCLDX	Data in hold time	10			
TR1VCL	RDY setup time into SAB 8284A[1][2])	35			
TCLR1X	RDY hold time into SAB 8284A[1][2])	0			
TRYHCH	READY setup time into SAB 8086	53			
TCHRYX	READY hold time into SAB 8086	20			
TRYLCL	READY inactive to CLK[3])	–10			
TINVCH	Setup time for recognition (INTR, NMI, $\overline{\text{TEST}}$)[2])	15			
TGVCH	$\overline{\text{RQ}}/\overline{\text{GT}}$ setup time	12			
TCHGX	$\overline{\text{RQ}}$ hold time into SAB 8086	20			
TILIH	Input rise time (except CLK)	–	20		from 0.8 to 2.0V
TIHIL	Input fall time (except CLK)		12		from 2.0 to 0.8V

[1]) Signal at SAB 8284B or SAB 8288A shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T2 state (8 ns into T3).

Timing Responses SAB 8086-1 (preliminary)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TCLML	Command active delay[1])	10	35	ns	CL = 20 to 100 pF for all SAB 8086 outputs (in addition to SAB 8086 self-load)
TCLMH	Command inactive delay[1])				
TRYHSH	READY active to status passive[2])	–	45		
TCHSV	Status active delay	10			
TCLSH	Status inactive delay		55		
TCLAV	Address valid delay		50		
TCLAX	Address hold time		–		
TCLAZ	Address float delay		40		
TSVLH	Status valid to ALE high[1])	–	15		
TSVMCH	Status valid to MCE high[1])				
TCLLH	CLK low to ALE valid[1])				
TCLMCH	CLK low to MCE high[1])				
TCHLL	ALE inactive delay[1])				
TCLDV	Data valid delay	10	50		
TCHDX	Data hold time		–		
TCVNV	Control active delay[1])	5	45		
TCVNX	Control inactive delay[1])	10			

[1]) Signal at SAB 8284B or SAB 8288A shown for reference only.
[2]) Applies only to T3 and wait states.

Timing Responses SAB 8086-1 (cont'd)
(preliminary)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
TAZRL	Address float to READ active	0	–	ns	CL = 20 to 100 pF for all SAB 8086 outputs (in addition to SAB 8086 self-load)
TCLRL	$\overline{RD}$ active delay	10	70		
TCLRH	$\overline{RD}$ inactive delay		60		
TRHAV	$\overline{RD}$ inactive to next address active	TCLCL-35	–		
TCHDTL	Direction control active delay[1])	–	50		
TCHDTH	Direction control inactive delay[1])		30		
TCLGL	$\overline{GT}$ active delay	0	45		
TCLGH	$\overline{GT}$ inactive delay				
TRLRH	$\overline{RD}$ width	2TCLCL-40	–		
TOLOH	Output rise time	–	20		from 0.8 to 2.0V
TOHOL	Output fall time		12		from 2.0 to 0.8V

[1]) Signal at SAB 8284B or SAB 8288A shown for reference only.
[2]) Applies only to T3 and wait states.

Figure 8 Bus Timing – Minimum Mode System

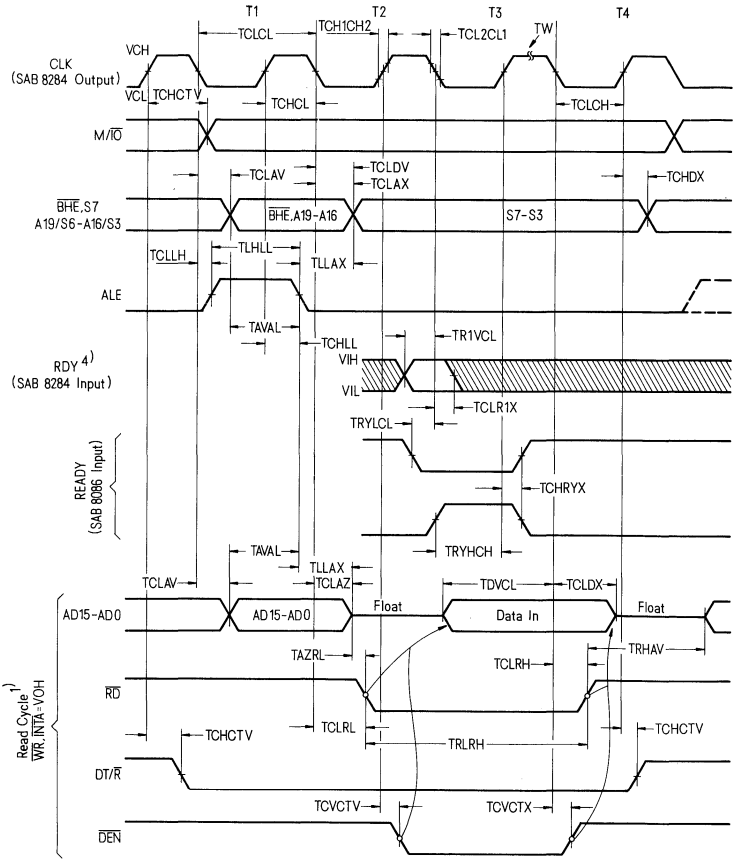
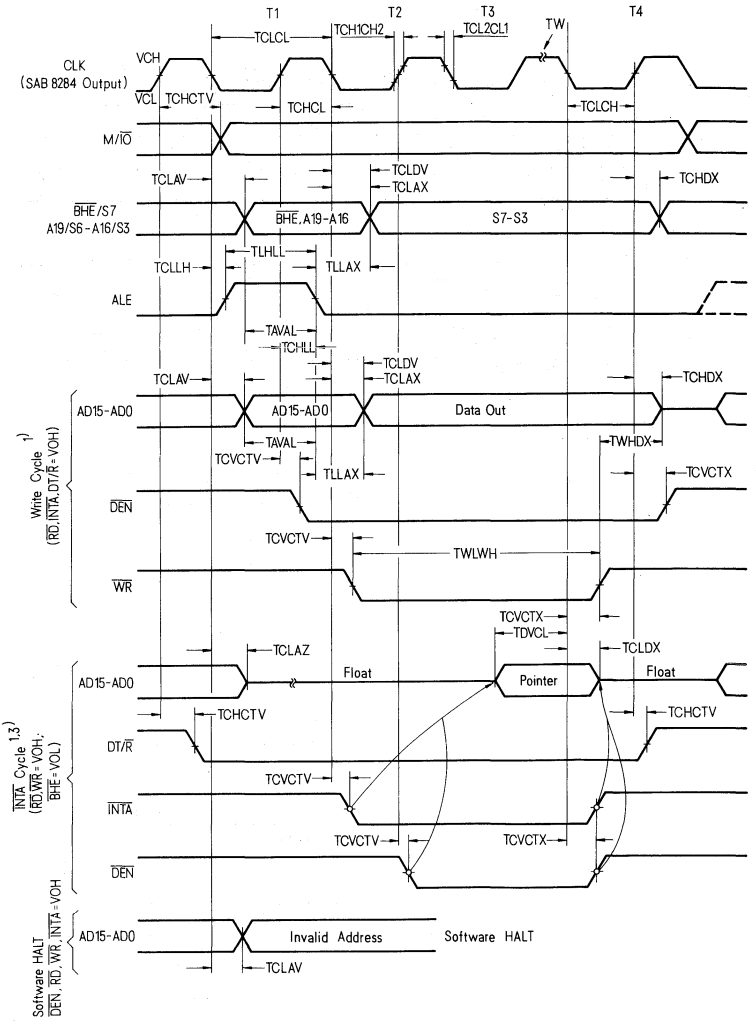


Figure 9 SAB 8086 Bus Timing – Minimum Mode System (cont'd)



1) All signals switch between VOH and VOL unless otherwise specified.
2) RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
3) Two INTA cycles run back to back. The SAB 8086 local ADDR/DATA bus is floating during both INTA cycles. Control signals shown for second INTA cycle.
4) Signals at SAB 8284B are shown for reference only.
5) All timing measurements are made at 1.5 V unless otherwise noted.

Figure 10 SAB 8086 Bus Timing – Maximum Mode System (using SAB 8288A)

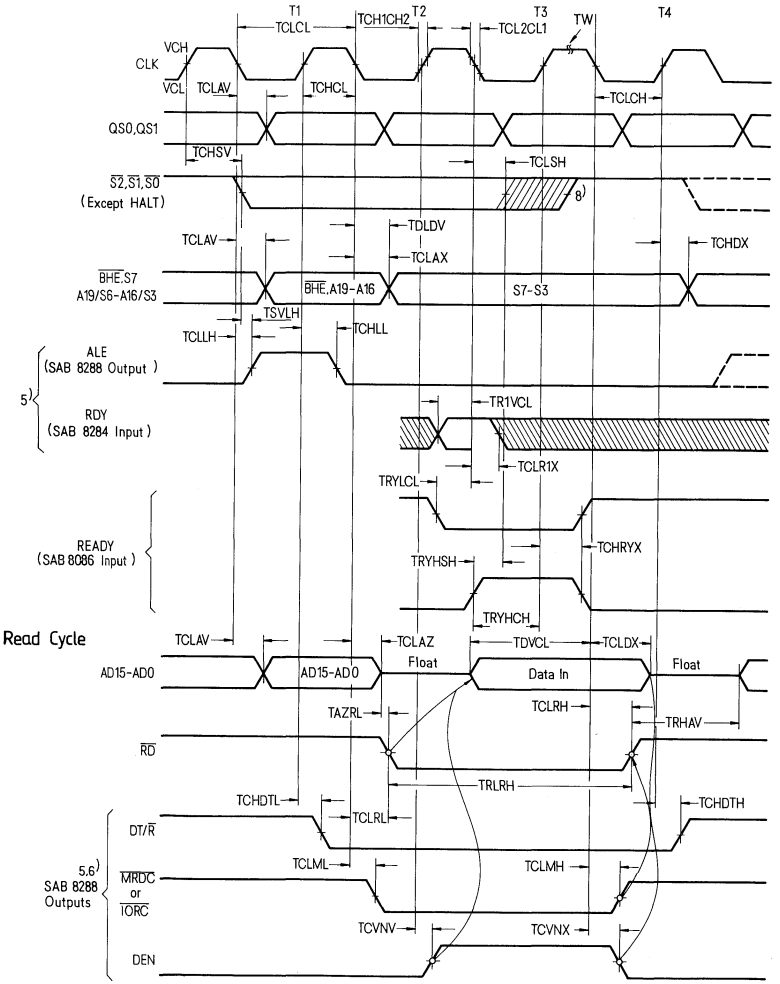
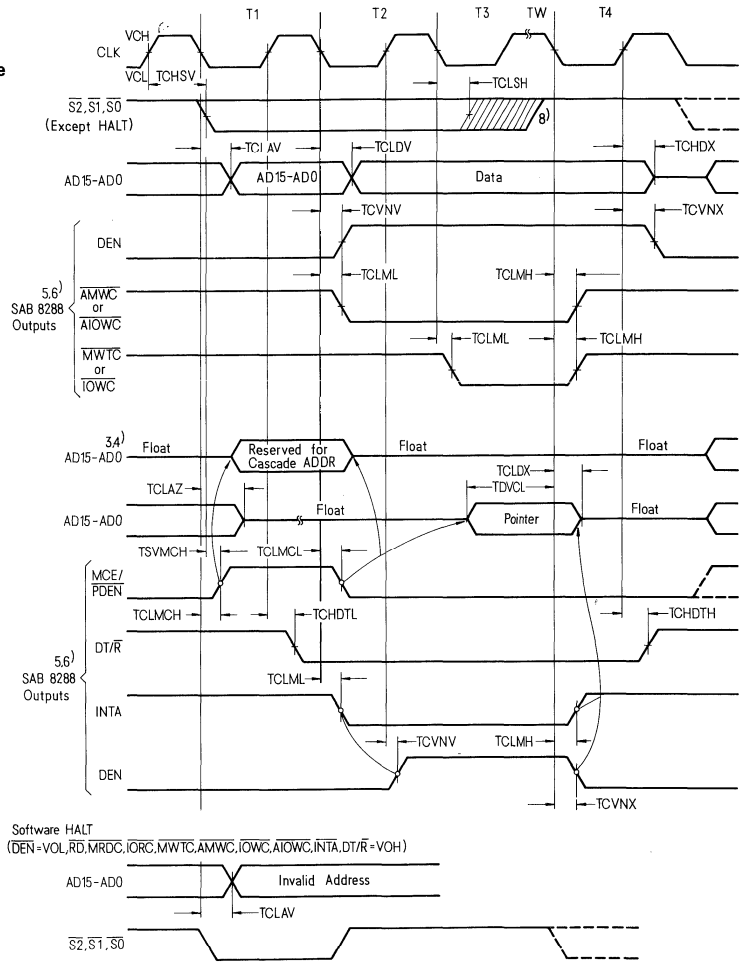
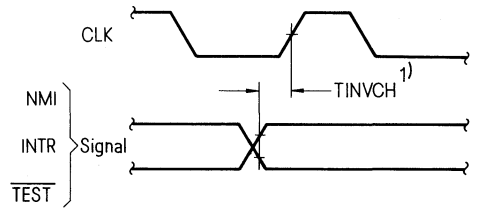


Figure 11 SAB 8086 Bus Timing – Maximum Mode System (using SAB 8288A) (cont'd)



[1]) All signals switch between VOH and VOL unless otherwise specified.
[2]) RDY is sampled near the end of T2, T3, TW to determine if TW machines states are to be inserted.
[3]) Cascade address is valid between first and second INTA cycle.
[4]) Two INTA cycles run back-to-back. The SAB 8086 local ADDR/DATA bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
[5]) Signals at SAB 8284B or SAB 8288A are shown for reference only.
[6]) The issuance of the SAB 8288A command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ and DEN) lags the active high SAB 8288A DEN.
[7]) All timing measurements are made at 1.5 V unless otherwise noted.
[8]) Status inactive in state just prior to T4.

Figure 12 Asynchronous Signal Recognition



[1]) Setup requirements for asynchronous signals only to guarantee recognition at next CLK

Figure 13 Bus Lock Signal Timing (maximum mode only)

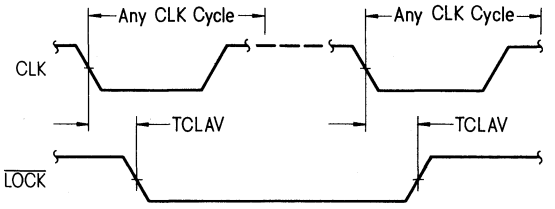
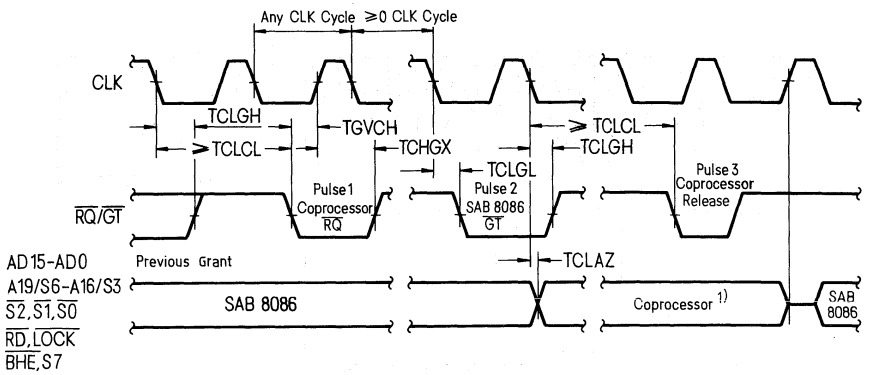
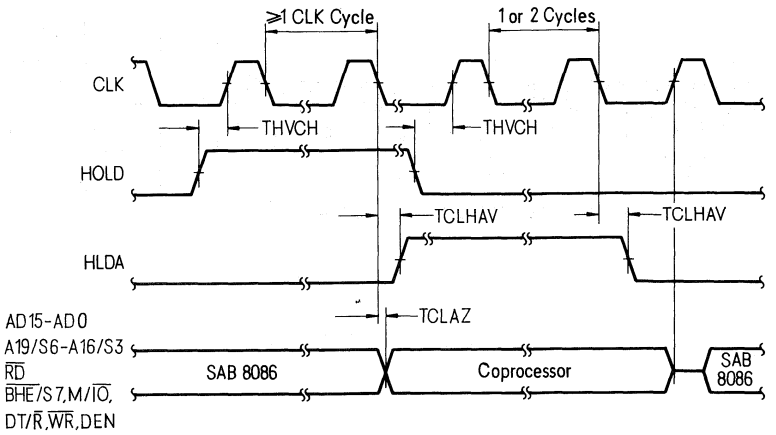


Figure 14 Request/Grant Sequence Timing (maximum mode only)



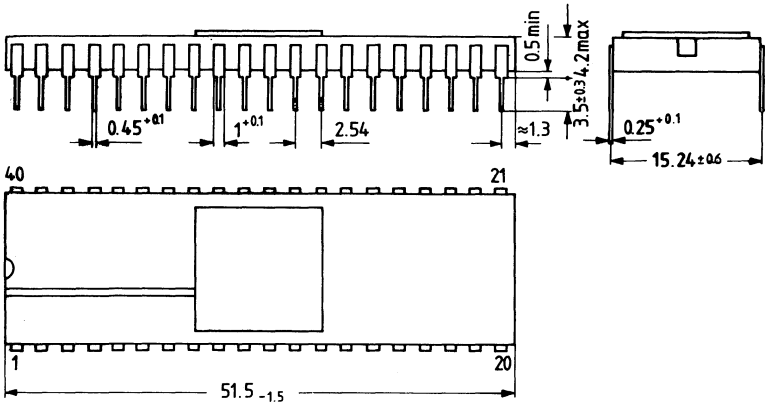
1) The coprocessor may not drive the buses outside the region shown without risking contention

Figure 15 Hold/Hold Acknowledge Timing (minimum mode only)

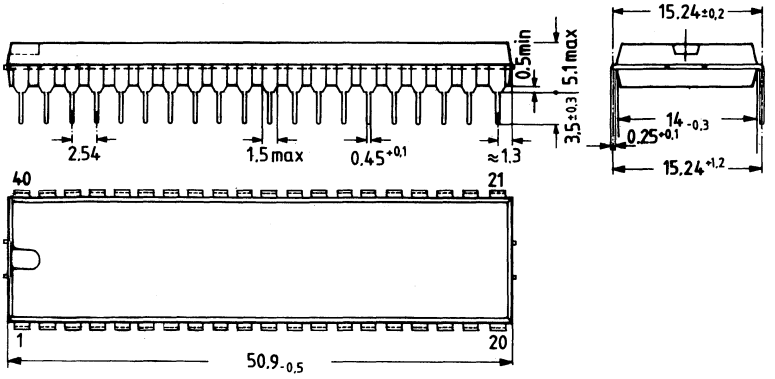


Package Outlines

40-Pin Ceramic Package Type C



40-Pin Plastic Package Type P



Dimensions in mm

Ordering Information

Type	Description	Ordering code
SAB 8086 C	16-bit microprocessor – 5 MHz ceramic	Q67120-C45
SAB 8086-2-C	16-bit microprocessor – 8 MHz ceramic	Q67120-C60
SAB 8086-1-C	16-bit microprocessor – 10 MHz ceramic	Q67120-C104
SAB 8086 P	16-bit microprocessor – 5 MHz plastic	Q67120-C116
SAB 8086-2-P	16-bit microprocessor – 8 MHz plastic	Q67120-C142
SAB 8086-1-P	16-bit microprocessor – 10 MHz plastic	Q67120-C141

Preliminary

SAB 80186 High-Integration 16-Bit Microprocessor

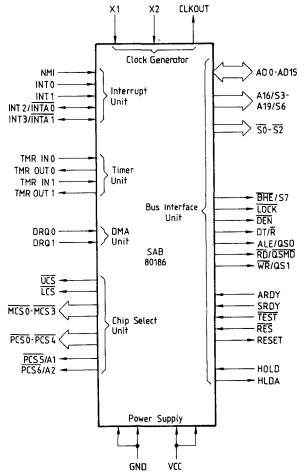
SAB 80186 8 MHz

- Integrated feature set
  - enhanced SAB 8086-2 CPU
  - clock generator
  - 2 independent high-speed DMA channels
  - programmable interrupt controller
  - 3 programmable 16-bit timers
  - programmable memory and peripheral chip-select logic
  - programmable wait state generator
  - local bus controller
- High-performance processor
  - twice the performance of the standard SAB 8086 at 8 MHz
  - 4 Mbyte/s bus bandwidth interface at 8 MHz

SAB 80186-1 10 MHz

- Direct addressing capability to 1 Mbyte of memory
- Completely object-code compatible with all existing SAB 8086/8088 software
  - 10 new instruction types
- Optional numerical processor extension
- Compatible with the bus support components SAB 8282A/8283A/8286A/8287A and SAB 8288A/8289
- Compatible with industry standard 80186 processor
- Available in 10 MHz (SAB 80186-1) and 8 MHz (SAB 80186) versions

Logic Symbol



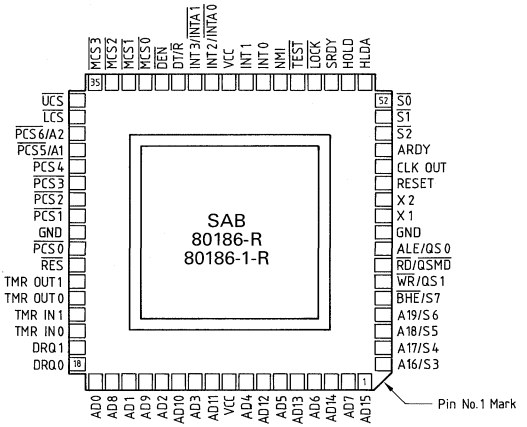
Pin Names

AD0–AD15	Address/Data Bus
A16/S3–A19/S6	Address Bus/Status Lines
S0–S2	Status Lines
$\overline{\text{BHE}}$/S7	Bus High Enable/Status Line
$\overline{\text{LOCK}}$	Bus Lock
$\overline{\text{DEN}}$	Data Enable
DT/$\overline{\text{R}}$	Data Transmit/Receive
ALE/QS0	Address Latch Enable/Queue Status
$\overline{\text{RD}}$/QSMD	Read Strobe/Queue Status Mode
$\overline{\text{WR}}$/QS1	Write Strobe/Queue Status
ARDY	Asynchronous Ready
SRDY	Synchronous Ready
$\overline{\text{TEST}}$	Test Line
$\overline{\text{RES}}$	Reset Input
RESET	Reset Output
HOLD	Hold Request
HLDA	Hold Acknowledge
NMI	Non-Maskable Interrupt
INT0, INT1	Interrupt Request
INT2/INTA0	Interrupt Request/Acknowledge
INT3/INTA1	Interrupt Request/Acknowledge
TMR IN0/TMR OUT0	Timer 0 Input/Output
TMR IN1/TMR OUT1	Timer 1 Input/Output
DRQ0, DRQ1	Data Request
$\overline{\text{UCS}}$, $\overline{\text{LCS}}$	Upper/Lower Chip Select
$\overline{\text{MCS0}}$–$\overline{\text{MCS3}}$	Memory Chip Select
$\overline{\text{PCS0}}$–$\overline{\text{PCS4}}$	Peripheral Chip Select
PCS5/A1, PCS6/A2	Peripheral Chip Select/Address
VCC	Power Supply (+5 V)
GND	Ground (0 V)

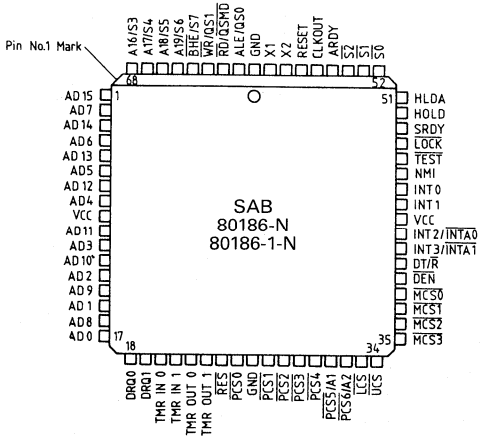
The SAB 80186 is a highly integrated 16-bit microprocessor implemented in +5 V advanced Siemens MYMOS technology. It effectively combines 15 to 20 of the most common SAB 8086 system components onto one chip. The 8 MHz SAB 80186 provides twice the throughput of the standard 5 MHz SAB 8086. The SAB 80186 is upward-compatible with SAB 8086 and SAB 8088 software, and adds 10 new instruction types to the existing set. The SAB 80186 comes in a 68-pin ceramic chip carrier (C-CC-68) package or in a plastic leaded chip carrier (PL-CC-68) package and requires single +5 V power supply.

Pin Configuration

C-CC Package
Component pad view – as viewed from underside of component when mounted on the board.



PL-CC Package (top view)



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
AD15–AD0	10–17, 1–8	I/O	**ADDRESS/DATA BUS (0 TO 15)** These signals constitute the time-multiplexed memory or I/O address (T1) and data (T2, T3, TW, and T4) bus. The bus is active high. A0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D7 through D0. It is low during T1 when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations.
DRQ0 DRQ1	18 19	I I	**DMA REQUEST** Is driven high by an external device when it desires that a DMA channel (channel 0 or 1) performs a transfer. These signals are active high, level-triggered, and internally synchronized.
TMR IN 0, TMR IN 1	20 21	I I	**TIMER INPUTS** Are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active high (or low-to-high transitions are counted) and internally synchronized.
TMR OUT 0, TMR OUT 1	22 23	O O	**TIMER OUTPUTS** Are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected.
$\overline{RES}$	24	I	**$\overline{SYSTEM\ RESET}$** Causes the SAB 80186 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the SAB 80186 clock. The SAB 80186 begins fetching instructions approximately 7 clock cycles after $\overline{RES}$ is returned high. $\overline{RES}$ is required to be low for greater than 4 clock cycles and is internally synchronized. For proper initialization, the low-to-high transition of $\overline{RES}$ must occur no sooner than 50 microseconds after power up. This input is provided with a Schmitt trigger to facilitate power-on $\overline{RES}$ generation via an RC network. When $\overline{RES}$ occurs, the SAB 80186 will drive the status lines to an inactive level for one clock, and then tristate them.
$\overline{PCS0}$ $\overline{PCS1–4}$	25 27, 28, 29, 30	O O	**$\overline{PERIPHERAL\ CHIP\ SELECT\ 0\ TO\ 4}$** These signals are active low when a reference is made to the defined peripheral area (64 Kbyte I/O space). These lines are not tristated during bus hold. The address ranges activating $\overline{PCS0–4}$ are software-programmable.
$\overline{PCS5}$/A1	31	O	**$\overline{PERIPHERAL\ CHIP\ SELECT}$ 5/LATCHED A1** May be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software-programmable. When programmed to provide latched A1, rather than $\overline{PCS5}$, this pin will retain the previously latched value of A1 during a bus HOLD. A1 is active high.
$\overline{PCS6}$/A2	32	O	**$\overline{PERIPHERAL\ CHIP\ SELECT}$ 6/LATCHED A2** May be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software-programmable. When programmed to provide latched A2, rather than $\overline{PCS6}$, this pin will retain the previously latched value of A2 during a bus HOLD. A2 is active high.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{LCS}$	33	O	**$\overline{LOWER\ MEMORY\ CHIP\ SELECT}$** Is active low whenever a memory reference is made to the defined lower portion (1 K to 256 K) of memory. This line is not tristated during bus HOLD. The address range activating $\overline{LCS}$ is software-programmable.
$\overline{UCS}$	34	O	**$\overline{UPPER\ MEMORY\ CHIP\ SELECT}$** Is an active low output whenever a memory reference is made to the defined upper portion (1 K to 256 K block) of memory. This line is not tristated during bus HOLD. The address range activating $\overline{UCS}$ is software-programmable.
$\overline{MCS0-3}$	38, 37, 36, 35	O	**$\overline{MIDRANGE\ MEMORY\ CHIP\ SELECT\ 0\ TO\ 3}$** These signals are active low when a memory reference is made to the defined midrange portion of memory (8 K to 512 K). These lines are not tristated during bus HOLD. The address ranges activating $\overline{MCS0-3}$ are software-programmable.
$\overline{DEN}$	39	O	**$\overline{DATA\ ENABLE}$** Is provided as an SAB 8286A/8287A data bus transceiver output enable. $\overline{DEN}$ is active low during each memory and I/O access. $\overline{DEN}$ is high whenever DT/$\overline{R}$ changes its state.
DT/$\overline{R}$	40	O	**DATA TRANSMIT/$\overline{RECEIVE}$** Controls the direction of data flow through the external SAB 8286A/8287A data bus transceiver. When low data is transferred to the SAB 80186. When high the SAB 80186 places write data on the data bus.
INT0, INT1, INT2/$\overline{INTA0}$ INT3/$\overline{INTA1}$	45, 44 42 41	I I/O I/O	**MASKABLE INTERRUPT REQUEST** Can be requested by strobing one of these pins. When configured as inputs, these pins are active high. Interrupt requests are synchronized internally. INT2 and INT3 may be configured via software to provide active low interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When iRMX mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).
NMI	46	I	**NON-MASKABLE INTERRUPT** Is an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from low to high initiates the interrupt at the next instruction boundary. NMI is latched internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized.
$\overline{TEST}$	47	I	**$\overline{TEST}$** Is examined by the WAIT instruction. If the $\overline{TEST}$ input is high when "WAIT" execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled until it goes low, at which time execution will be resumed. If interrupts are enabled while the SAB 80186 is waiting for $\overline{TEST}$, interrupts will be serviced. This input is synchronized internally.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{LOCK}$	48	O	**$\overline{LOCK}$** This output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active low. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the $\overline{LOCK}$ prefix. It remains active until the completion of the instruction following the $\overline{LOCK}$ prefix. No pre-fetches will occur while $\overline{LOCK}$ is asserted. $\overline{LOCK}$ is active low, is driven high for one clock during reset, and then tristated.
SRDY	49	I	**SYNCHRONOUS READY** Must be synchronized externally to the SAB 80186. The use of SRDY provides a relaxed system-timing specification on the ready input. This is accomplished by eliminating the one-half clock cycle which is required for internally resolving the signal level when using the ARDY input. This line is active high. If this line is connected to VCC no wait states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active before a bus cycle is terminated. If unused, this line should be tied low.
HOLD HLDA	50 51	I O	**HOLD/HOLD ACKNOWLEDGE** Indicates that another bus master is requesting the local bus. The HOLD input is active high. HOLD may be asynchronous with respect to the SAB 80186 clock. The SAB 80186 will issue a HLDA (high) in response to a HOLD request at the end of T4 or T1. Simultaneous with issuing HLDA, the SAB 80186 will tristate the local bus and control lines. After HOLD is detected as being low, the SAB 80186 will lower HLDA. When the SAB 80186 needs to run another bus cycle, it will again drive the local bus and control lines.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	52–54	O	**$\overline{BUS\ CYCLE\ STATUS}$** $\overline{S0}$ to $\overline{S2}$ are encoded to provide bus transaction information: SAB 80186 Bus Cycle Status Information

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

The status pins are tristated during "HOLD."
$\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.
The status lines are driven high for one clock during reset, and then tristated until a bus cycle begins.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
ARDY	55	I	**ASYNCHRONOUS READY** Informs the SAB 80186 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input and is active high. Only the rising edge is internally synchronized by the SAB 80186. This means that the falling edge of ARDY must be synchronized to the SAB 80186 clock. If connected to VCC no wait states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active to terminate a bus cycle. If unused, this line should be tied low.
CLKOUT	56	O	**CLOCK OUTPUT** Provides the system with a 50% duty cycle waveform. All device pin timings are specified relative in CLKOUT.
RESET	57	O	**RESET** This output indicates that the SAB 80186 CPU is being reset, and can be used as a system reset. It is active high, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal.
X1, X2	59, 58	I	**CRYSTAL INPUTS** X1 and X2 provide an external connection for a fundamental-mode parallel resonant crystal for the internal crystal oscillator. X1 can interface to an external clock instead of a crystal. In this case, minimize the capacitance on X2 or drive X2 with complemented X1. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
ALE/QS0	61	O	**ADDRESS LATCH ENABLE/QUEUE STATUS 0** Is provided by the SAB 80186 to latch the address into the SAB 8282A/8283A address latches. ALE is active high. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T1 of the associated bus cycle, effectively half a clock cycle earlier than in the standard SAB 8086. The trailling edge is generated off the CLKOUT rising edge in T1 like in the SAB 8086. Note that ALE is never tristated.
$\overline{RD}$/$\overline{QSMD}$	62	O	**$\overline{READY\ STROBE}$** Indicates that the SAB 80186 is performing a memory or I/O read cycle. $\overline{RD}$ is active low for T2, T3 and TW of any read cycle. It is guaranteed not to go low in T2 until after the address bus is tristated. $\overline{RD}$ is active low and tristated during "HOLD". $\overline{RD}$ is driven high for one clock during reset, and then the output driver is tristated. A weak internal pullup mechanism on the $\overline{RD}$ line holds it high when the line is not driven. During reset, the pin is sampled to determine whether the SAB 80186 should provide ALE, $\overline{WR}$ and $\overline{RD}$, or if the queue status should be provided. $\overline{RD}$ should be connected to GND to provide queue status data.

Pin Definitions and Functions (cont'd)

$\overline{WR}$/QS1	63	O	**$\overline{WRITE\ STROBE}$/QUEUE STATUS 1** Indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T2, T3, and TW of any write cycle. It is active low and tristated during "HOLD." It is driven high for one clock during reset, and then tristated. When the SAB 80186 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.

QS1	QS0	Queue Operation
0	0	No Queue Operation
0	1	First Op Code Byte Fetched from the Queue
1	1	Subsequent Byte Fetched from the Queue
1	0	Empty the Queue

$\overline{BHE}$/S7	64	O	**BUS HIGH ENABLE** During T1 this signal should be used to determine if data is to be enabled onto the most significant half of the data bus, pins D15 to D8. $\overline{BHE}$ is low during T1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the higher half of the bus. The S7 status information is available during T2, T3, and T4. S7 is logically equivalent to $\overline{BHE}$. The signal is active low, and is tristated off during bus HOLD.

$\overline{BHE}$ and A0 Encodings

$\overline{BHE}$ Value	A0 Value	Function
0	0	Word Transfer
0	1	Byte Transfer on Upper Half of Data Bus (D15 to D8)
1	0	Byte Transfer on Lower Half of Data Bus (D7 to D0)
1	1	Reserved

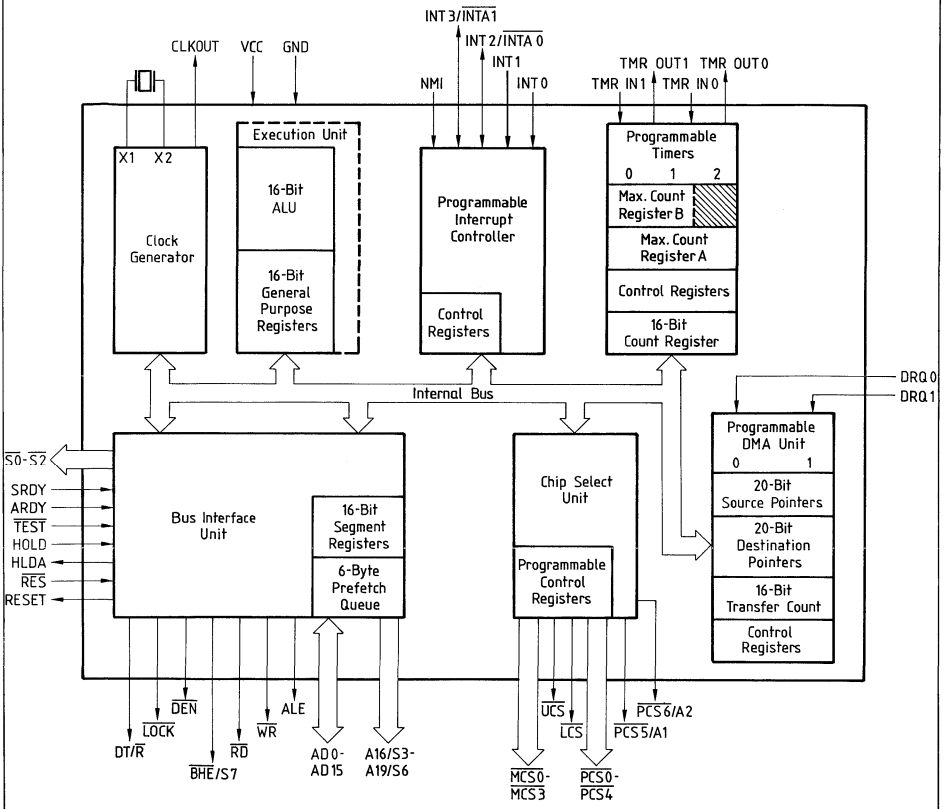
A19/S6, A18/S5, A17/S4, A16/S3	65 66 67 68	O O O O	**ADDRESS BUS OUTPUTS** (16 to 19) and **BUS CYCLE STATUS** (3 to 6) They reflect the four most significant address bits during T1. These signals are active high. During T2, T3, TW, and T4, status information is available on these lines as encoded below:

	Low	High
S6	Processor Cycle	DMA Cycle

S3, S4, and S5 are defined as being low during T2 to T4.

V_{CC}	9, 43	I	**POWER SUPPLY** (+5 V)
GND	26, 60	I	**GROUND** (0 V)

Block Diagram



Functional Description

The SAB 8086,8088, 80186, 80188 and 80286 families all contain the same basic set of registers, instructions, and addressing modes. The SAB 80186 processor is upward-compatible with the SAB 8086 and SAB 8088 CPUs.

Register Set

The SAB 80186 base architecture has fourteen registers. These registers are grouped into the following categories.

General registers

Eight 16-bit general-purpose registers may be used to contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

Segment registers

Four 16-bit special-purpose registers select, at any time given, the segments of memory that are immediately addressable for code, stack, and data.

Base and index registers

Four of the general-purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

Status and control registers

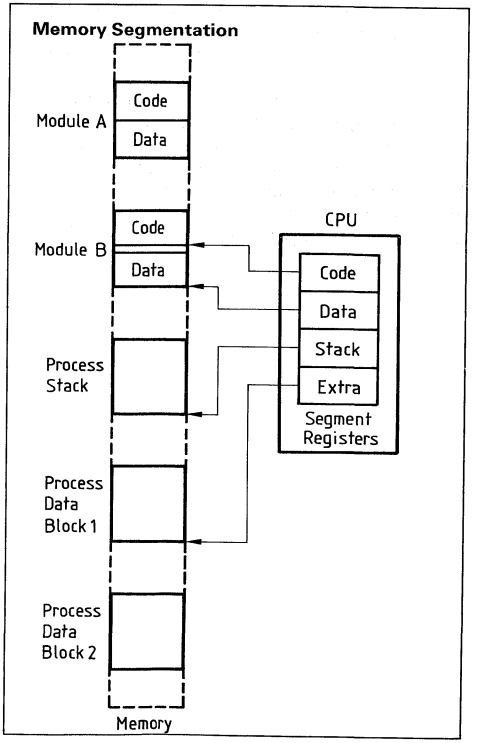
Two 16-bit special-purpose registers record or alter certain aspects of the SAB 80186 processor state. These are the instruction pointer register, which contains the offset address of the next sequential instruction to be executed, and the status word register, which contains status and control flag bits.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64 K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment registers (code, data, stack, extra). The physical address is calculated by shifting the base value left by four bits and adding the 16-bit offset value to yield a 20-bit physical address. This allows for a 1 Mbyte physical address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used. These rules follow the way programs are written as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs.



I/O Space

The I/O space consists of 64 K 8-bit or 32 K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero-extended such that A15 to A8 are low I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (status word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware-initiated, INT instructions, and instruction exceptions. Hardware-initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.

Interrupt Sources

The SAB 80186 can service interrupts generated by software or hardware. The software interrupts are generated by specific instructions (INT, ESC, unused OP, etc.) or the results of conditions specified by instructions (array bounds check, INT0, DIV, IDIV, etc.). All interrupt sources are serviced by an indirect call through an element of a vector table. This vector table is indexed by using the interrupt vector type, multiplied by four. All hardware-generated interrupts are sampled at the end of each instruction. Thus, the software interrupts will begin service first. Once the service routine is entered and interrupts are enabled, any hardware source of sufficient priority can interrupt the service routine in progress.

Interrupt Vector Table

Interrupt Name	Vector Type	Default Priority [5]	Related Instructions
Divide Error Exception	0	1 [1]	DIV, IDIV
Single-Step Interrupt	1	12 [2] 2	All
NMI	2	1	All
Breakpoint Interrupt	3	1 [1]	INT
INT0 Detected Overflow Exception	4	1 [1]	INT0
Array Bounds Exception	5	1 [1]	BOUND
Unused Op Code Exception	6	1 [1]	Undefined Op Codes
ESC Op Code Exception	7	1 [1] [3]	ESC Op Codes
Timer 0 Interrupt	8	2A [4]	
Timer 1 Interrupt	18	2B [4]	
Timer 2 Interrupt	19	2C [4]	
Reserved	9	3	
DMA 0 Interrupt	10	4	
DMA 1 Interrupt	11	5	
INT0 Interrupt	12	6	
INT1 Interrupt	13	7	
INT2 Interrupt	14	8	
INT3 Interrupt	15	9	

[1] These are generated as the result of an instruction execution.

[2] This is handled as in the SAB 8086.

[3] An escape op code will cause a trap only if the proper bit is set in the peripheral control block relocation register.

[4] All three timers constitute one source of request to the interrupt controller. The timer interrupts all have the same default priority level with respect to all other interrupt sources. However, they have a defined priority ordering amongst themselves. (Priority 2A is higher priority than 2B.) Each timer interrupt has a separate vector type number.

[5] Default priorities for the interrupt sources are used only if the user does not program each source into a unique priority level.

Initialization and Processor Reset

Processor initialization or startup is accomplished by driving the $\overline{RES}$ input pin low. $\overline{RES}$ forces the SAB 80186 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as $\overline{RES}$ is active. After $\overline{RES}$ becomes inactive and an internal processing interval elapses, the SAB 80186 begins execution with the instruction at physical location FFFF0(H). $\overline{RES}$ also sets some registers to predefined values.

Initial Register State after RESET

Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation Register	20FF(H)
UMCS	FFFB(H)

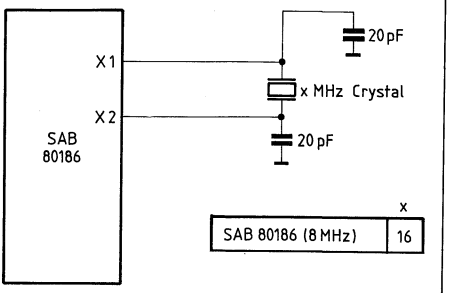
Clock Generator

The SAB 80186 provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs and reset circuitry.

Oscillator

The oscillator circuit of the SAB 80186 is designed to be used with a parallel resonant fundamental mode crystal. This is used as the time base for the SAB 80186. The crystal frequency selected will be twice the CPU clock frequency. Use of an LC or RC circuit is not recommended with this oscillator. If an external oscillator is used, it can be connected directly to input pin X1 in lieu of a crystal. The output of the oscillator is not directly available outside the SAB 80186.

Recommended SAB 80186 Crystal Configuration



The following parameters may be used for choosing a crystal:

Temperature range	0 to 70 °C
ESR (equivalent series resistance)	30 Ω max.
C0 (shunt capacitance of crystal)	7.0 pF max.
C1 (load capacitance)	20 pF ± 2 pF
Drive level	1 mW max.

Ready Synchronization

The SAB 80186 provides both synchronous and asynchronous ready inputs. Asynchronous ready synchronization is accomplished by circuitry which samples ARDY in the middle of T2, T3 and again in the middle of each TW until ARDY is sampled high.

A second ready input (SRDY) is provided to interface with externally synchronized ready signals. This input is sampled at the end of T2,T3 and again at the end of each TW until it is sampled high.

Reset Logic

The SAB 80186 provides both a $\overline{RES}$ input pin and a synchronized reset pin for use with other system components. The $\overline{RES}$ input pin on the SAB 80186 is provided with hysteresis in order to facilitate power-on reset generation via an RC network.

Local Bus Controller

The SAB 80186 provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides control lines that can be used to enable external buffers and to direct the flow of data on and off the local bus.

When the SAB 80186 relinquishes control of the local bus, it tristates $\overline{DEN}$, $\overline{RD}$, $\overline{WR}$, $\overline{S0}$ to $\overline{S2}$, $\overline{LOCK}$, AD0 to AD15, A16 to A19, $\overline{BHE}$, and DT/$\overline{R}$ to allow another master to drive these lines directly.

Local bus controller and reset

Upon receipt of a reset pulse from the $\overline{RES}$ input, the local bus controller will perform the following actions:

- Drive $\overline{DEN}$, $\overline{RD}$, and $\overline{WR}$ high for one clock cycle, then float.

  Note: $\overline{RD}$ is also provided with an internal pullup device to prevent the processor from inadvertently entering queue status mode during reset.
- Drive $\overline{S0}$ to $\overline{S2}$ to the passive state (all high) and then float.
- Drive $\overline{LOCK}$ high and then float.
- Tristate AD0 to AD15, A16 to A19, $\overline{BHE}$, DT/$\overline{R}$.
- Drive ALE low (ALE is never tristated).
- Drive HLDA low.

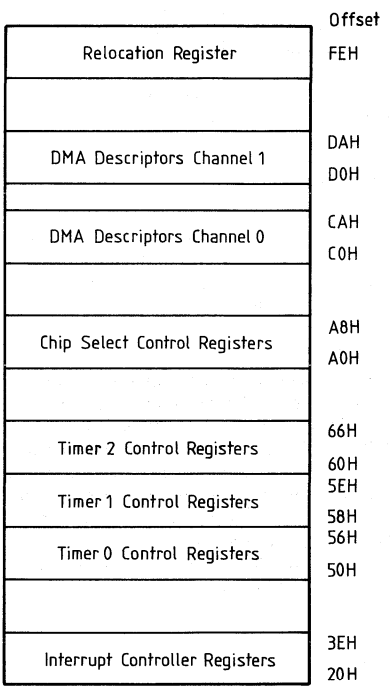
Internal Peripheral Interface

All the SAB 80186 integrated peripherals are controlled via 16-bit registers contained within an internal 256 byte control block. This control block may be mapped into either memory or I/O space. Internal logic will recognize the address and respond to the bus cycle. During bus cycles to internal registers, the bus controller will signal the operation externally (i.e., the $\overline{RD}$, $\overline{WR}$, status, address, data, etc., lines will be driven as in a normal bus cycle), but D15 to D0, SRDY, and ARDY will be ignored.

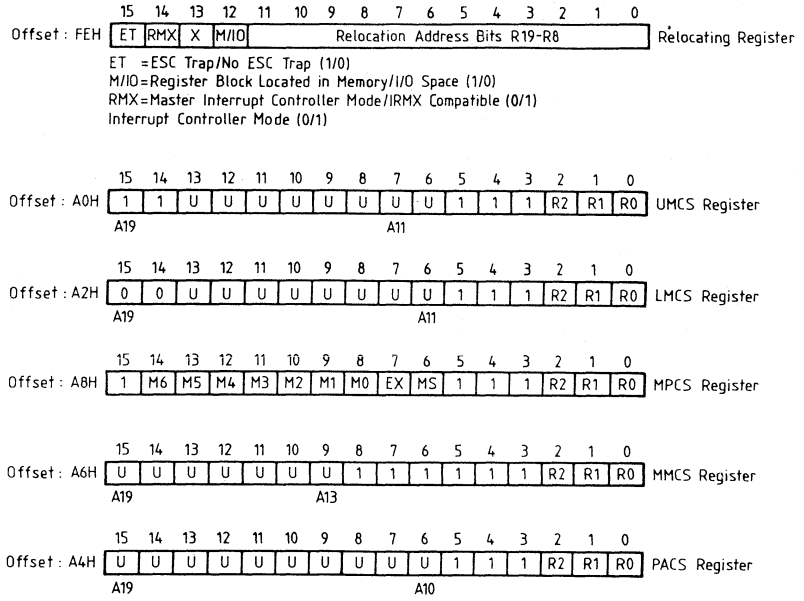
The control block base address is programmed via a 16-bit relocation register contained within the control block at offset FEH from the base address of the control block. It provides the upper 12 bits of the base address of the control block.

The integrated SAB 80186 peripherals operate semi-autonomously from the CPU. Access to them for the most part is via software read/write of the control and data locations in the control block. Most of these registers can be both read and written. A few dedicated lines, such as interrupts and DMA request provide real-time communication between the CPU and peripherals as in a more conventional system utilizing discrete peripheral blocks.

Internal Register Map



Chip Select Registers



UMCS Programming Values

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0=R1=R2=0)
FFC00	1 K	FFF8H
FF800	2 K	FFB8H
FF000	4 K	FF38H
FE000	8 K	FE38H
FC000	16 K	FC38H
F8000	32 K	F838H
F0000	64 K	F038H
E0000	128 K	E038H
C0000	256 K	C038H

LMCS Programming Values

Upper Address	Memory Block Size	LMCS Value (Assuming R0=R1=R2=0)
003FFH	1 K	0038H
007FFH	2 K	0078H
00FFFH	4 K	00F8H
01FFFH	8 K	01F8H
03FFFH	16 K	03F8H
07FFFH	32 K	07F8H
0FFFFH	64 K	0FF8H
1FFFFH	128 K	1FF8H
3FFFFH	256 K	3FF8H

MPCS Programming Values

Total Block Sice	Individual Select Size	MPCS Bits 14 to 8
8 K	2 K	0000001B
16 K	4 K	0000010B
32 K	8 K	0000100B
64 K	16 K	0001000B
128 K	32 K	0010000B
256 K	64 K	0100000B
512 K	128 K	1000000B

MS, EX Programming Values

Bit	Description
MS	1=Peripherals Mapped into Memory Space. 0=Peripherals Mapped into I/O Space.
EX	0=5 $\overline{\text{PCS}}$ Lines. A1, A2 Provided. 1=7 $\overline{\text{PCS}}$ Lines. A1, A2 Are Not Provided.

Ready Bits Programming

R2	R1	R0	Number of Wait States Generated
0	0	0	0 Wait States, External RDY Also Used
0	0	1	1 Wait State Inserted, External RDY Also Used.
0	1	0	2 Wait States Inserted, External RDY Also Used.
0	1	1	3 Wait States Inserted, External RDY Also Used
1	0	0	0 Wait States, External RDY Ignored.
1	0	1	1 Wait State Inserted, External RDY Ignored.
1	1	0	2 Wait States Inserted, External RDY ignored.
1	1	1	3 Wait States Inserted, External RDY Ignored.

Chip Select Logic

The SAB 80186 contains logic which provides programmable chip select generation for both, memories and peripherals. In addition, it can be programmed to provide ready (or wait state) generation. It can also provide latched address bits A1 and A2. The chip select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

Memory Chip Selects

The SAB 80186 provides 6 memory chip select outputs for 3 address areas: upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

Upper Memory $\overline{CS}$

The SAB 80186 provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the SAB 80186 begins executing at memory location FFFF0H. After reset, the UMCS register is programmed for a 1 K area. It must be reprogrammed if a larger upper memory area is desired.

Lower Memory $\overline{CS}$

The SAB 80186 provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H. After reset, the LMCS register value is undefined. However, the $\overline{LCS}$ chip select line will not become active until the LMCS register is accessed.

Midrange Memory $\overline{CS}$

The SAB 80186 provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located anywhere within the 1 Mbyte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

Each of the four chip select lines is active for one of the four equal contiguous divisions of the midrange block. Thus, if the total block size is 32 K, each chip select is active for 8 K of memory with $\overline{MCS0}$ being active for the first range and $\overline{MCS3}$ being active for the last range. After reset, the contents of both of these registers is undefined.

However, none of the $\overline{MCS}$ lines will be active until both the MMCS and MPCS registers are accessed.

Peripheral Chip Selects

The SAB 80186 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. This base address may be located in either memory or I/O space.

Seven $\overline{CS}$ lines called $\overline{PCS0-6}$ are generated by the SAB 80186. The base address is user-programmable; however it can only be a multiple of 1 Kbytes, i.e. the least significant 10 bits of the starting address are always 0.

$\overline{PCS5}$ and $\overline{PCS6}$ can also be programmed to provide latched address bits A1, A2. If so programmed, they cannot be used as peripheral selects.

The starting address of the peripheral chip select block is defined by the PACS register. This register is located at offset A4H in the internal control block. Bits 15 to 6 of this register correspond to bits 19 to 10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block.

PCS Address Ranges

PCS Line	Active between Locations
PCS0	PBA – PBA+127
PCS1	PBA+128 – PBA+255
PCS2	PBA+256 – PBA+383
PCS3	PBA+384 – PBA+511
PCS4	PBA+512 – PBA+639
PCS5	PBA+640 – PBA+767
PCS6	PBA+768 – PBA+895

Ready Generation Logic

The SAB 80186 can generate a ready signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of wait states to be inserted for each peripheral or memory is programmable to provide 0 to 3 wait states for all accesses to the area for which the chip select is active. In addition, the SAB 80186 may be programmed to either ignore external ready for each chip select range individually or to factor external ready with the integrated ready generator.

Ready control consists of 3 bits for each $\overline{CS}$ line or group of lines generated by the SAB 80186.

Chip Select/Ready Logic and Reset

Upon reset, the chip select/ready logic will perform the following actions:

- All chip select outputs will be driven high.
- Upon leaving reset, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1 K block with the accompanying ready control bits set at 011 to allow the maximum number of internal wait states in conjunction with external ready consideration (i.e. UMCS resets to FFFBH).
- No other chip select or ready control registers have any predefined values after reset. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the $\overline{PCS}$ lines will become active.

DMA Channels

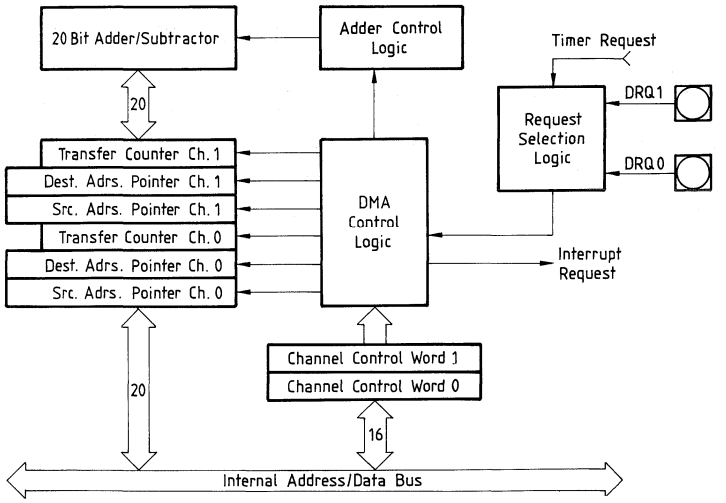
The SAB 80186 DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory-to-I/O) or within the same space (e.g., Memory-to-Memory or I/O-to-I/O). Data can be transferred either in bytes (8 bits) or in words (16 bits) to or from even or odd addresses. Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer (by one or two depending on byte or word transfers). Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data. This provides a maximum data transfer rate of one Mword/s or 2 Mbytes/s.

DMA Channel Control Word Register

Each DMA channel control word determines the mode of operation for the particular SAB 80186 DMA channel.

The DMA channel control registers may be changed while the channel is operating. However, any changes made during operation will affect the current DMA transfer.

DMA Unit Block Diagram



DMA Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M/$\overline{IO}$	Destination DEC	INC	M/$\overline{IO}$	Source DEC	INC	TC	INT	SYN		P	TDRQ	X	CHG/$\overline{NOCHG}$	ST/$\overline{STOP}$	$\overline{B}$/W

X=Don't Care

DMA Memory Pointer Register Format

Higher Register Address	XXX	XXX	XXX	A19-A16
Lower Register Address	A15-A12	A11-A8	A7-A4	A3-A0

15 0

XXX=Don't Care

DMA Control Block Format

Register Name	Register Address	
	Chan. 0	Chan. 1
Control Word	CAH	DAH
Transfer Count	C8H	D8H
Destination Pointer (upper 4 bits)	C6H	D6H
Destination Pointer	C4H	D4H
Source Pointer (upper 4 bits)	C2H	D2H
Source Pointer	C0H	D0H

DMA Control Word Bit Description

$\overline{B}$/W — Byte/word (0/1) transfers.

ST/$\overline{STOP}$ — Start/stop (1/0) channel.

CHG/$\overline{NOCHG}$ — Change/do not change (1/0) ST/$\overline{STOP}$ bit. If this bit is set when writing to the control word, the ST/$\overline{STOP}$ bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/$\overline{STOP}$ bit will not be altered. This bit is not stored; it will always be a 0 on read.

INT — Enable interrupts to CPU on tranfer count termination.

TC — If set, DMA will terminate when the contents of the transfer count register reach zero. The ST/$\overline{STOP}$ bit will also be reset at this point if TC is set. If this bit is cleared, the DMA unit will decrement the transfer count register for each DMA cycle, but the DMA transfer will not stop when the contents of the TC register reach zero.

SYN (2 bits) — 00 No synchronization.
Note: The ST bit will be cleared automatically when the contents of the TC register reach zero regardless of the state of the TC bit.
01 Source synchronization.
10 Destination synchronization.
11 Unused.

TDRQ — 0: Disable DMA requests from timer 2.
1: Enable DMA requests from timer 2.

Bit 3 — Bit 3 is not used.

Source: INC — Increment source pointer by 1 or 2 (depends on $\overline{B}$/W) after each transfer.

M/$\overline{IO}$ — Source pointer is in M/IO space (1/0).

DEC — Decrement source pointer by 1 or 2 (depends on $\overline{B}$/W) after each transfer.

Destin.: INC — Increment destination pointer by 1 or 2 ($\overline{B}$/W) after each transfer.

M/$\overline{IO}$ — Destination pointer is in M/IO space (1/0).

DEC — Decrement destination pointer by 1 or 2 (depending on $\overline{B}$/W) after each transfer.

P — Channel priority – relative to other channel.
0 low priority.
1 high priority.
Channels will alternate cycles if both set at same priority level.

DMA Destination and Source Pointer Register

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address.

DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). This register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA control register.

DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is, the transfer will take place continually until the correct number of transfers has occurred.

DMA Priority

The DMA channels may be programmed such that one channel is always given priority over the other, or they may be programmed such as to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses or word accesses to odd memory locations; however, an external bus hold takes priority over an internal DMA cycle.

DMA Channels and Reset

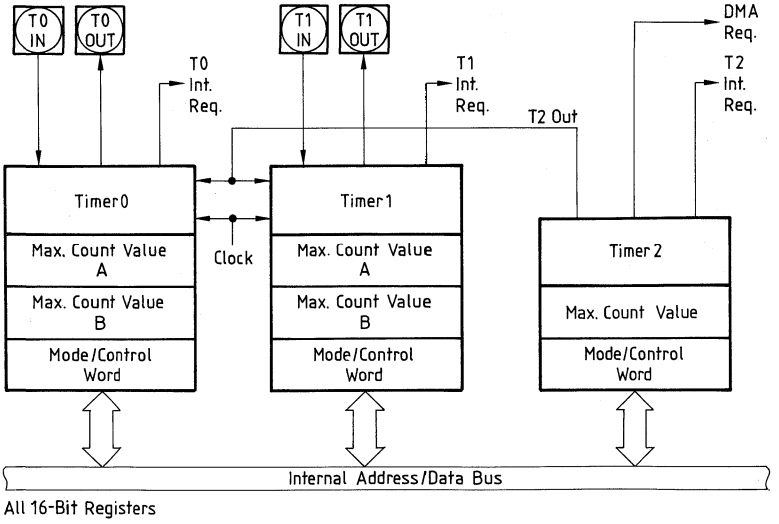
Upon reset, the DMA channels will perform the following actions:

- The start/stop bit for each channel will be reset to STOP.
- Any transfer in progress is aborted.

Timers

The SAB 80186 provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, this third timer can be used as a prescaler to the other two, or as a DMA request source.

Timer Block Diagram



Timer Mode/Control Register

15	14	13	12	11	·····	5	4	3	2	1	0
EN	$\overline{INH}$	INT	RIU	0	·····	MC	RTG	P	EXT	ALT	CONT

Timer Control Block Format

Register Name	Register Offset		
	TMR 0	TMR 1	TMR 2
Mode/Control Word	56H	5EH	66H
Max. Count B	54H	5CH	not present
Max. Count A	52H	5AH	62H
Count Register	50H	58H	60H

Timer Operation

The timers are controlled by eleven 16-bit registers in the internal peripheral control block. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incremented for each timer event. Each of the timers is equipped with a max. count register, which defines the maximum count the timer will reach. After reaching the max. count register value, the timer count value will be reset to zero during that same clock.

Each timer gets serviced every fourth CPU clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU clock rate (2 MHz for an 8 MHz CPU clock).

The timers have several programmable options.

- All three timers can be set to halt or continue on a terminal count.
- Timers 0 and 1 can select between internal and external clocks, alternate between max. count registers and be set to retrigger on external events.
- The timers may be programmed to cause an interrupt on terminal count.

Count Registers

Each of the three timers has a 16-bit count register. The current contents of this register may be read or written by the processor at any time. If the register is written into while the timer is counting, the new value will take effect in the current count cycle.

Max. Count Registers

Timers 0 and 1 have two max.count registers, while timer 2 has a single max.count register. These contain the number of events the timer will count. In timers 0 and 1, the max.count register used can alternate between the two max.count values whenever the current maximum count is reached.

Timer Mode/Control Register

The mode/control register allows the user to program the specific mode of operation or check the current programmed status for any of the three integrated timers.

ALT:
The ALT bit determines which of two max. count registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one max.count register while the other is being used, and thus provides a method of generating nonrepetitive waveforms. Square waves and pulse outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is zero, the output pin will go low for one clock, the clock after the maximum count is reached. If ALT is one, the output pin will reflect the current max.count register being used (0/1 for B/A).

CONT:
Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the max. count register A value, be reset, count to the register B value, be reset, and halt.

EXT:
The external bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the SAB 80186 clock. If EXT is set, the timer will count low-to-high transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input-to-output transition latency time may be as much as 6 clocks. However, clock inputs may be pipelined as closely together as every 4 clocks without losing clock pulses.

P:
The prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a zero, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a one, the output of timer 2 will be used as a clock for the timer. Note that the user must initialize and start timer 2 to obtain the prescaled clock.

RTG:
Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is high, the timer will count; if the input pin is low, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the SAB 80186 clock.

When RTG = 1, the input pin detects low-to-high transitions. The first transition starts the timer running, clearing the timer value to zero on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to zero, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

EN:
The enable bit provides programmer control over the timer's RUN/HALT status. When set, the timer is enabled to increment subject to the input pin constraints in the internal clock mode (discussed previously). When cleared, the timer will be inhibited from counting. All input pin transitions during which the time EN is zero will be ignored. If CONT is zero, the EN bit is automatically cleared upon maximum count.

INH:
The inhibit bit allows for selective updating of the enable (EN) bit. If INH is a one during the write to the mode/control word, then the state of the EN bit will be modified by the write. If INH is a zero during the write, the EN bit will be unaffected by the operation. This bit is not stored; it will always be a 0 on a read.

INT:
When set, the INT bit enables interrupts from the timer, which will be generated on every terminal count. If the timer is configured in dual max.count register mode, an interrupt will be generated each time the value in max.count register A is reached, and each time the value in max.count register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the interrupt controller.)

MC:
The maximum count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual max.count register mode, this bit will be set each time the value in max.count register A is reached, and each time the value in max.count register B is reached. This bit is set regardless of the timer's interrupt enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts.
Programmer intervention is required to clear this bit.

RIU:
The register in use bit indicates which max.count register is currently being used for comparison to the timer count value. A zero indicates register A. The RIU bit cannot be written, i.e. its value is not affected when the control register is written. It is always cleared when the ALT bit is zero.
Not all mode bits are provided for timer 2. Certain bits are hardwired as indicated below:

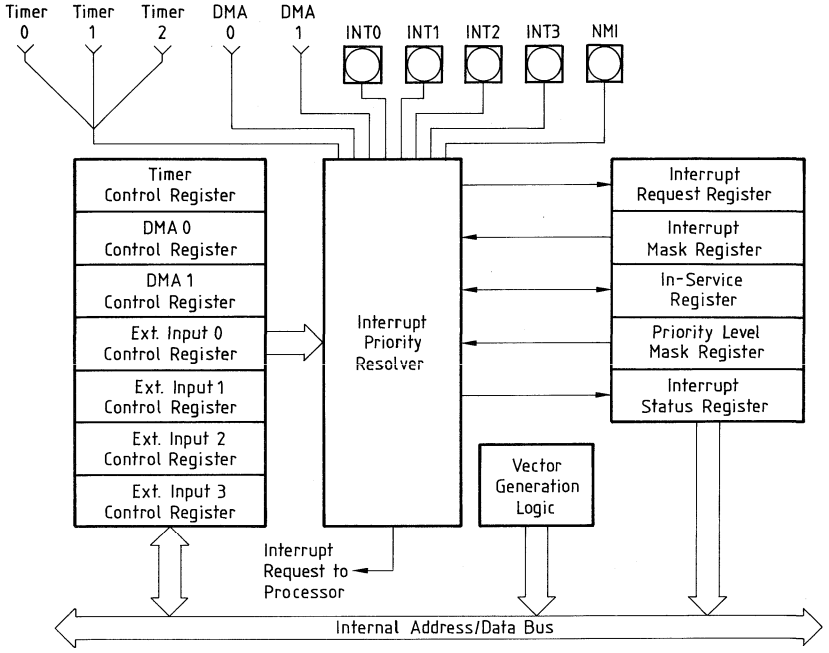
ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

Timers and Reset

Upon reset, the timers will perform the following actions:

- All EN (enable) bits are reset preventing timer counting.
- All SEL (select) bits are reset to zero. This selects max. count register A, resulting in the timer-out pins going high upon reset.

Interrupt Controller Block Diagram



Interrupt Controller

The SAB 80186 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU. Internal interrupt sources (timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The SAB 80186 interrupt controller has its own control registers that set the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may themselves be interrupted by higher priority interrupts.
The interrupt controller has a special iRMX 86 compatibility mode that allows the use of the SAB 80186 within the iRMX 86 operating system interrupt structure.

Master Mode Operation

Interrupt Controller External Interface

For external interrupt sources, five dedicated pins are provided. One of these pins is dedicated to NMI, non-maskable interrupt. This is typically used for power-fail interrupts, etc. The other four pins may function either as four interrupt input lines with internally generated interrupt vectors, as an interrupt line and an interrupt acknowledge line (called the "cascade mode") along with two other input lines with internally generated interrupt vectors, or as two interrupt input lines and two dedicated interrupt acknowledge output lines. When the interrupt lines are configured in cascade mode, the SAB 80186 interrupt controller will not generate internal interrupt vectors.

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in master mode are similar to the SAB 8259A. The interrupt controller responds identical to internal interrupts in all three modes: the difference is only in the interpretation of function of the four external interrupt pins.

Fully nested mode
When in fully nested mode, four pins are used as direct interrupt requests. The vectors for these four inputs are generated internally. An in-service bit (IS) is provided for every interrupt source. If a lower priority device requests an interrupt while the in-service bit is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the in-service bit is set, no interrupt will be generated by the interrupt controller.
When a service routine is completed, the proper IS bit must be reset by writing the proper pattern to the EOI register.

Cascade mode
The SAB 80186 has four interrupt pins and two of them have dual functions. In fully nested mode, the four pins are used as direct interrupt inputs and the corresponding vectors are generated internally. In cascade mode, the four pins are configured into interrupt input-dedicated acknowledge signal pairs. INT0 is an interrupt input interfaced to an SAB 8259A, while INT2/$\overline{\text{INTA0}}$ serves as the dedicated interrupt acknowledge signal to the peripheral. The same is true for INT1 and INT3/$\overline{\text{INTA1}}$. Each pair can selectively be placed in the cascade or non-cascade mode by programming the proper value INT0 and INT1 control registers.
The primary cascade mode allows the capability to serve up to 128 external interrupt sources through the use of external master and slave SAB 8259As.

Special fully nested mode
This mode is entered by setting the SFNM bit in INT0 or INT1 control register. It enables complete nestability with external SAB 8259A masters. In special fully nested mode, the SAB 80186 interrupt controller will allow interrupts from an external pin regardless of the state of the in-service bit for an interrupt source in order to allow multiple interupts from a single pin.

Polling operation
The controller may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the interrupt controller whenever it is convenient. Polling the interrupt controller is accomplished by reading the poll word. Bit 15 in the poll word indicates to the processor that an interrupt of high enough priority is requesting service.

Interrupt Controller Registers (non-iRMX 86 mode)

	Offset
INT3 Control Register	3EH
INT2 Control Register	3CH
INT1 Control Register	3AH
INT0 Control Register	38H
DMA1 Control Register	36H
DMA0 Control Register	34H
Timer Control Register	32H
Interrupt Status Register	30H
Interrupt Request Register	2EH
In-Service Register	2CH
Priority Mask Register	2AH
Mask Register	28H
Poll Status Register	26H
Poll Register	24H
EOI Register	22H

Timer/DMA Control Register Formats

15	14	...	4	3	2	1	0
0	0	...	0	MSK	PR2	PR1	PR0

INT0/INT1 Control Register Formats

15	14	...	7	6	5	4	3	2	1	0
0	0	...	0	SFNM	C	LTM	MSK	PR2	PR1	PR0

INT2/INT3 Control Register Formats

15	14	...	5	4	3	2	1	0
0	0	...	0	LTM	MSK	PR2	PR1	PR0

In-Service, Interrupt Request, and Mask Register Formats

15	14	...	10	9	8	7	6	5	4	3	2	1	0
0	0	...	0	0	0	I3	I2	I1	I0	D1	D0	0	TMR

Priority Mask Register Format

15	14	...	3	2	1	0
0	0	...	0	PRM2	PRM1	PRM0

Interrupt Status Register Format

15	14	...	7	6	5	4	3	2	1	0
DHLT	0	...	0	0	0	0	0	IRT2	IRT1	IRT0

EOI Register Format

15	14	13	...	5	4	3	2	1	0
SPEC/NSPEC	0	0	...	0	S4	S3	S2	S1	S0

Poll Register Format

15	14	13	...	5	4	3	2	1	0
INT REQ.	0	0	...	0	S4	S3	S2	S1	S0

Master Mode Features

Programmable priority
The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0 to 7) in the control register of each interrupt source.

End-of-interrupt command
The end-of-interrupt (EOI) command is used by the programmer to reset the in-service (IS) bit when an interrupt service routine is completed. The EOI command is issued by writing the proper pattern to the EOI register. There are two types of EOI commands, specific and nonspecific. The non-specific command does not specify which IS bit is reset.

Trigger mode
The four external interrupt pins can be programmed in either edge or level-trigger mode. The control register for each external source has a level-trigger mode (LTM) bit. All interrupt inputs are active high. In the edge-sense mode or the level-trigger mode, the interrupt request must remain active (high) until the interrupt request is acknowledged by the SAB 80186 CPU. In the edge-sense mode, if the level remains high after the interrupt is acknowledged, the input is disabled and no further requests will be generated. The input level must go low for at least one clock cycle to reenable the input.

Interrupt vectoring
The SAB 80186 interrupt controller will generate interrupt vectors for the integrated DMA channels and the integrated timers. In addition, the interrupt controller will generate interrupt vectors for the external interrupt lines if they are not configured in cascade or special fully nested mode.

Interrupt Controller Registers

In-service register
This register contains the in-service bit for each of the interrupt sources. The in-service bit is set to indicate that a source's service routine is in progress. When an in-service bit is set, the interrupt controller will not generate interrupts to the CPU when it receives interrupt requests from devices with a lower programmed priority level. The TMR bit is the in-service bit for all three timers; the D0 and D1 bits are the in-service bits for the two DMA channels; the I0 – I3 bits are the in-service bits for the external interrupt pins.

Interrupt request register
The internal interrupt sources have interrupt request bits inside the interrupt controller. A read from this register yields the status of these bits. The TMR bit is the logical OR of all timer interrupt requests. D0 and D1 are the interrupt request bits for the DMA channels.

Mask register
This is a 16-bit register that contains a mask bit for each interrupt source. A one in a bit position corresponding to a particular source serves to mask the source from generating interrupts. These mask bits are exactly the same bits which are used in the individual control registers.

Priority mask register
This register is used to mask all interrupts below particular interrupt priority levels. The code in the lower three bits of this register inhibits interrupts of priority lower (a higher priority number) than the code specified.

Interrupt status register
This register contains general interrupt controller status information. The bits in the status register have the following functions:

DHLT: DMA halt transfer; setting this bit halts all DMA transfers. It is automatically set whenever a non-maskable interrupt occurs, and it is reset when an IRET instruction is executed.

IRTx: These three bits represent the individual timer interrupt request bits. These bits are used to differentiate the timer interrupts, since the timer IR bit in the interrupt request register is the "OR" function of all timer interrupt requests.

Timer, DMA 0, 1 control registers
These registers are the control words for all the internal interrupt sources. The three bit positions PR0, PR1, and PR2 represent the programmable priority level of the interrupt source. The MSK bit inhibits interrupt requests from the interrupt source. The MSK bits in the individual control registers are exactly the same bits as are in the mask register; modifying them in the individual control registers will also modify them in the mask register, and vice versa.

INT0 to INT3 control registers
These registers are the control words for the four external input pins. In cascade mode or special fully nested mode, the control words for INT2 and INT3 are not used.

PR0-2: Priority programming information. Highest priority = 000, lowest priority = 111

LTM: Level-trigger mode bit. 1 = level-triggered; 0 = edge-triggered. Interrupt input levels are active high. In level-triggered mode, an interrupt is generated whenever the external line is high. In edge-triggered mode, an interrupt will be generated only when this level is preceded by an inactive-to-active transition on the line. In both cases, the level must remain active until the interrupt is acknowledged.

MSK: Mask bit, 1 = mask; 0 = nonmask.

C: Cascade mode bit, 1 = cascade; 0 = direct

SFNM: Special fully nested mode bit, 1 = SFNM

EOI register
The end-of-interrupt register is a command register which can only be written into. It initiates an EOI command when written to by the SAB 80186 CPU.

S_x: Encoded information that specifies an interrupt source vector type

NSPEC/SPEC: A bit that determines the type of EOI command. Nonspecific = 1, specific = 0.

Poll and poll status registers
These registers contain polling information. They can only be read. Reading the poll register constitutes a software poll. This will set the IS bit of the highest priority pending interrupt.

S_x: Encoded information that indicates the vector type of the highest priority interrupting source. Valid only when INTREQ = 1.

INTREQ: This bit determines if an interrupt request is present. Interrupt request = 1; no interrupt request = 0.

iRMX 86 Compatibility Mode

This mode allows iRMX 86-SAB 80186 compatibility. The interrupt model of iRMX 86 requires one master and multiple slave SAB 8259As in cascaded mode. When iRMX mode is used, the internal SAB 80186 interrupt controller will be used as a slave controller to an external master interrupt controller.
Upon reset, the SAB 80186 interrupt controller will be in the non-iRMX 86 mode of operation. To set the controller in the iRMX 86 mode, bit 14 of the relocation register should be set.

The iRMX 86 operating system requires peripherals to be assigned fixed priority levels. This is incompatible with the normal operation of the SAB 80186 interrupt controller. Therefore, the initialization software must program the proper priority levels for each source.

Required iRMX Internal Source Priority Levels

Priority Level	Interrupt Source
0	Timer 0
1	(reserved)
2	DMA 0
3	DMA 1
4	Timer 1
5	Timer 2

iRMX 86 Mode External Interface

In the iRMX 86 configuration of the SAB 80186 the INT0 input is used as the SAB 80186 CPU interrupt input. INT3 functions as an output to send the SAB 80186 slave-interrupt-request to one of the 8 master PIC inputs. Correct master-slave interface requires decoding of the slave addresses (CAS0–2). Slave SAB 8259As do this internally. Because of pin limitations, the SAB 80186 slave address will have to be decoded externally. $\overline{INT1}$ is used as a slave-select input.

$\overline{INT2}$ is used as an acknowledge output, suitable to drive the $\overline{INTA}$ input of an SAB 8259A.

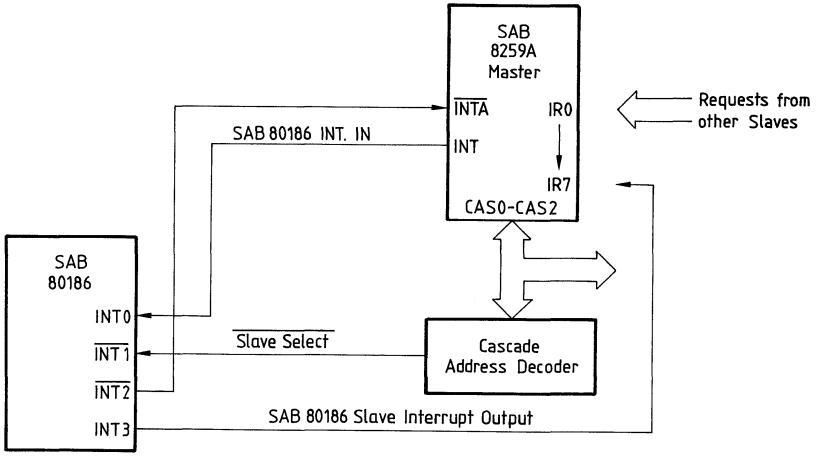
Vector Generation in the iRMX 86 Mode

Vector generation in iRMX mode is exactly like that of an SAB 8259A slave. The interrupt controller generates an 8-bit vector which the CPU multiplies by four and uses as an address into a vector table. The significant five bits of the vector are user-programmable while the lower three bits are generated by the priority logic.

Specific End-of-Interrupt

In iRMX mode the specific EOI command operates to reset an in-service bit of a specific priority. The user supplies a 3-bit priority-level value that points to an in-service bit to be reset.

iRMX 86 Interrupt Controller Interconnection



Interrupt Controller Registers (iRMX 86 mode)

	Offset
Level 5 Control Register (Timer 2)	3AH
Level 4 Control Register (Timer 1)	38H
Level 3 Control Register (DMA 1)	36H
Level 2 Control Register (DMA 0)	34H
Level 0 Control Register (Timer 0)	32H
Interrupt Status Register	30H
Interrupt-Request Register	2EH
In-Service Register	2CH
Priority-Level Mask Register	2AH
Mask Register	28H
Specific EOI Register	22H
Interrupt Vector Register	20H

Specific EOI Register Format

15	14	13	· · · · · · · ·	8	7	6	5	4	3	2	1	0
0	0	0		0	0	0	0	0	0	L2	L1	L0

In-Service, Interrupt Request, and Mask Register Format

15	14	13	· · · · · · · ·	8	7	6	5	4	3	2	1	0
0	0	0		0	0	0	TMR 2	TMR 1	D1	D0	0	TMR 0

Control Word Format

15	14	13	· · · · · · · ·	8	7	6	5	4	3	2	1	0
0	0	0		0	0	0	0	0	MSK	PR2	PR1	PR0

Interrupt Vector Register Format

15	14	13	· · · · · · · ·	8	7	6	5	4	3	2	1	0
0	0	0		0	t4	t3	t2	t1	t0	0	0	0

Priority Level Mask Register

15	14	13	· · · · · · · ·	8	7	6	5	4	3	2	1	0
0	0	0		0	0	0	0	0	0	m2	m1	m0

Interrupt Controller Registers in the iRMX 86 Mode

End-of-interrupt register
The end-of-interrupt register is a command register which can only be written to. It initiates an EOI command when written to by the SAB 80186 CPU.

Lx: Encoded value indicating the priority of the IS bit to be reset.

In-service register
This register contains the in-service bit for each of the internal interrupt sources. Bit positions 2 and 3 correspond to the DMA channels; positions 0, 4, and 5 correspond to the integral timers.

Interrupt request register
This register indicates which internal peripherals have interrupt requests pending. The interrupt request bits are set when a request arrives from an internal source, and are reset when the processor acknowledges the request.

Mask register
This register contains a mask bit for each interrupt source. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked.

Control registers
These registers are the control words for all the internal interrupt sources.

PRx: 3-bit encoded field indicating a priority level for the source; note that each source must be programmed at specified levels.

MSK: Mask bit for the priority level indicated by PRx bits.

Interrupt vector register
This register provides the upper five bits of the interrupt vector address. The interrupt controller itself provides the lower three bits of the interrupt vector as determined by the priority level of the interrupt request.
The format of the bits in this register is:
tx: 5-bit field indicating the upper five bits of the vector address.

Priority-level mask register
This register indicates the lowest priority-level interrupt which will be serviced.

The encoding of the bits in this register is:
mx: 3-bit encoded field indication priority-level value. All levels of lower priority will be masked.

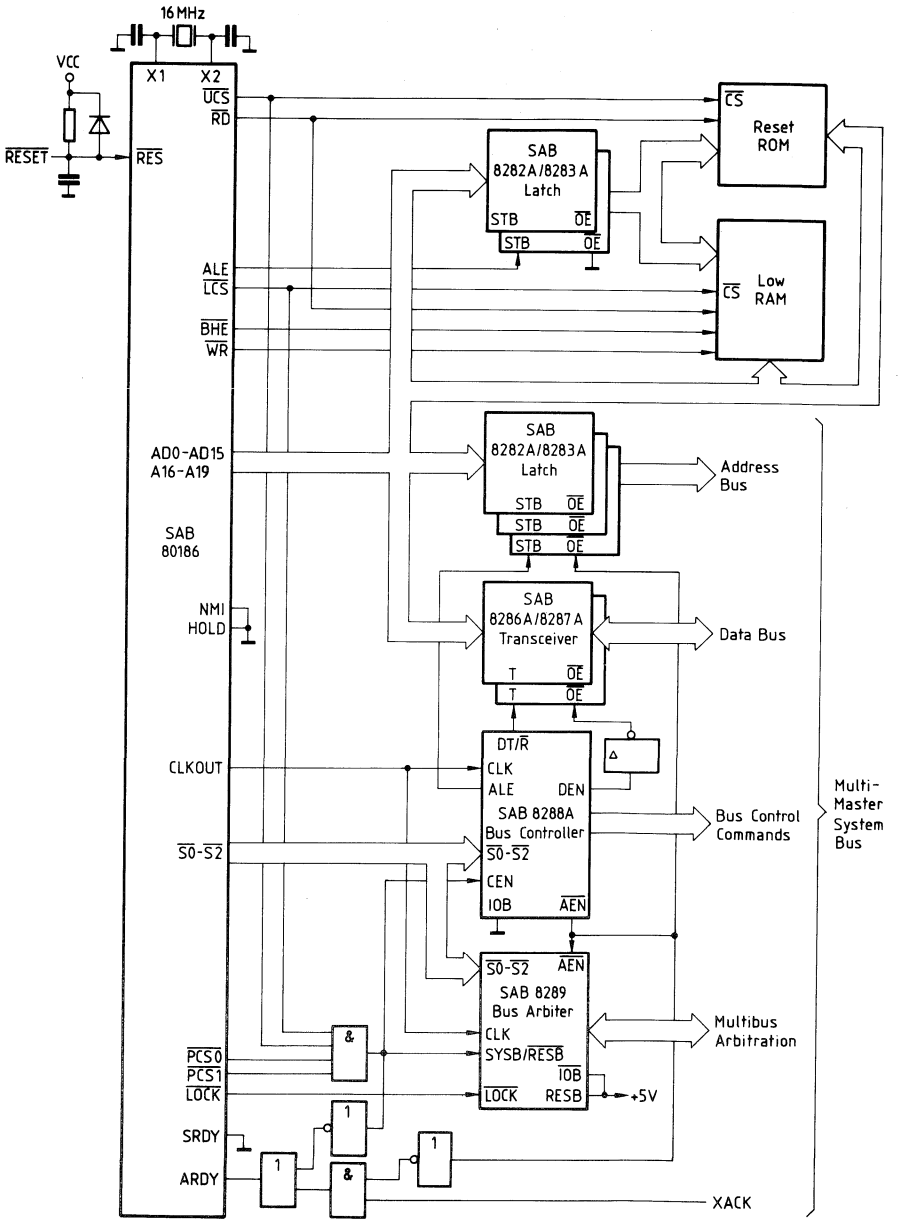
Interrupt status register
This register is defined exactly as in non-iRMX mode.

Interrupt Controller and Reset

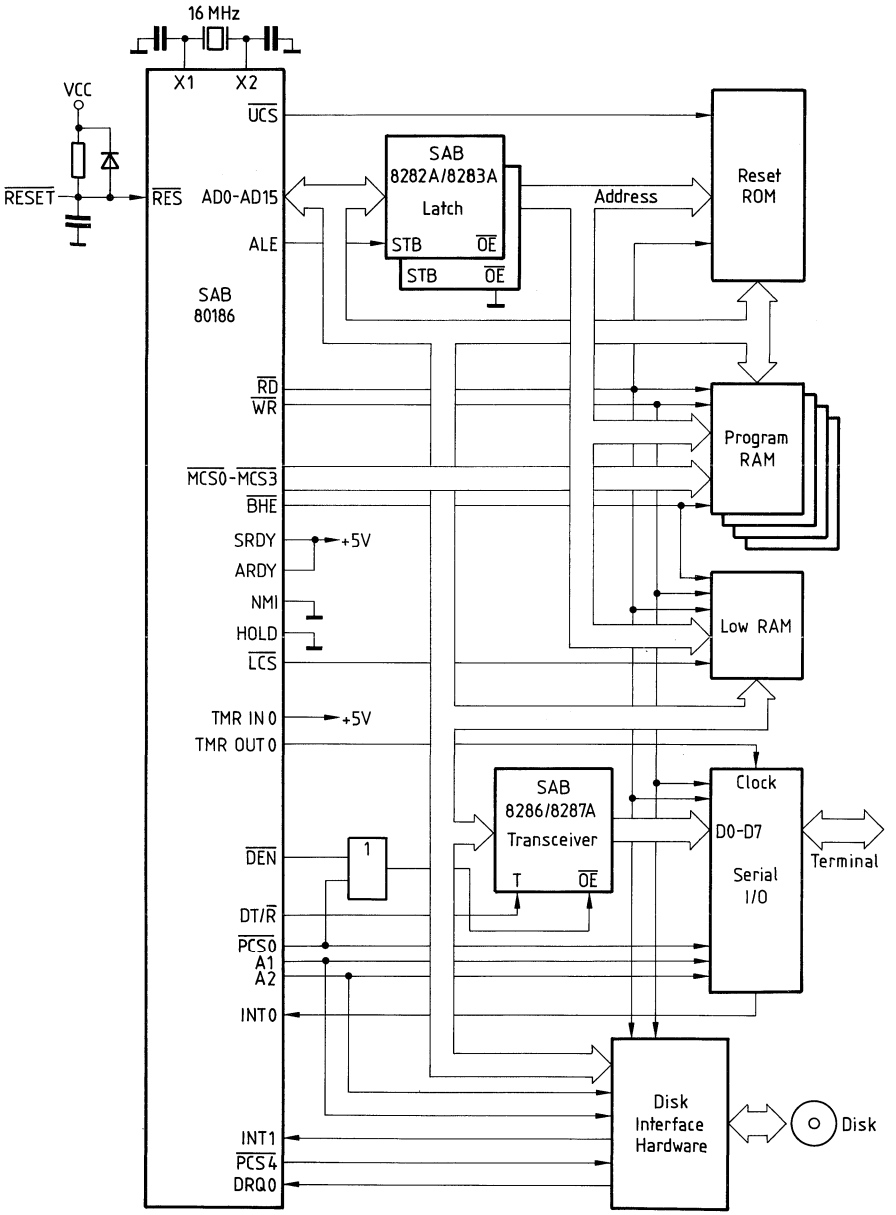
Upon reset, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying fully nested mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All interrupt service bits reset to 0.
- All interrupt request bits reset to 0.
- All MSK (interrupt mask) bits set to 1 (mask).
- All C (cascade) bits reset to 0 (non-cascade).
- All PRM (Priority mask) bits set to 1, implying no levels masked.
- Initialized to non-iRMX 86 mode.

Typical SAB 80186 Multimaster Bus Interface



Typical SAB 80186 System Configuration



Instruction Timings

The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The op code, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDs occur.
- All word data is located on even-address boundaries.

All jumps and calls include the time required to fetch the op code of the next instruction at the destination address.

All instructions which involve memory reference can require one (and in some cases, two) additional clocks above the minimum timings shown. This is due to the asynchronous nature of the handshake between the BIU and the execution unit.

Notes:

The effective address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

If r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

* except if mod = 00 and r/m = 110 then EA = disp-high: disp-low

Note: EA calculation time is 4 clock cycles for all modes, and is included in the execution times given whenever appropriate.

Segment override prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-bit (w = 1)	8-bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

Instruction Set Summary

Function	Format	Clock Cycles	Comments
Data Transfer			
MOV = Move:			
Register to register/memory	1000100w | mod reg r/m	2/12	
Register/memory to register	1000101w | mod reg r/m	2/9	
Immediate to register/memory	1100011w | mod 000 r/m | data | data if w = 1	12–13	8/16-bit
Immediate to register	1011w reg | data | data if w = 1	3–4	8/16-bit
Memory to accumulator	1010000w | addr-low | addr-high	9	
Accumulator to memory	1010001w | addr-low | addr-high	8	
Register/memory to segment register	10001110 | mod 0 reg r/m	2/9	
Segment register to register/memory	10001100 | mod 0 reg r/m	2/11	
PUSH = Push:			
Memory	11111111 | mod 110 r/m	16	
Register	01010 reg	10	
Segment register	000 reg 110	9	
Immediate	011010s0 | data | data if s = 0	10	
PUSHA = Push All	01100000	36	
POP = Pop:			
Memory	10001111 | mod 000 r/m	20	
Register	01011 reg	10	
Segment register	000 reg 111 (reg ≠ 01)	8	

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format			Clock Cycles	Comments
Data Transfer (cont'd)					
POPA = Pop All	01100001			51	
XCHG = **Exchange:**					
Register/memory with register	1000011w	mod reg r/m		4/17	
Register with accumulator	10010 reg			3	
IN = **Input from:**					
Fixed port	1110010w	port		10	
Variable port	1110110w			8	
OUT = **Output to:**					
Fixed port	1110011w	port		9	
Variable port	1110111w			7	
XLAT = Translate byte to AL	11010111			11	
LEA =Load EA to register	10001101	mod reg r/m		6	
LDS = Load pointer to DS	11000101	mod reg r/m	(mod ≠ 11)	18	
LES = Load pointer to ES	11000100	mod reg r/m	(mod ≠ 11)	18	
LAHF = Load AH with flags	10011111			2	
SAHF = Store AH into flags	10011110			3	
PUSHF = Push flags	10011100			9	
POPF = Pop flags	10011101			8	
SEGMENT = **Segment override:**					
CS	00101110			2	
SS	00110110			2	
DS	00111110			2	
ES	00100110			2	

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Arithmetic			
ADD = Add:			
Reg./memory with register to either	00000dw | mod reg. r/m	3/10	
Immediate to register/memory	100000sw | mod 000 r/m | data | data if s w = 01	4/16	
Immediate to accumulator	0000010w | data | data if w = 1	3/4	8/16-bit
ADC = Add with carry:			
Reg./memory with register to either	000100dw | mod reg r/m	3/10	
Immediate to register/memory	100000sw | mod 010 r/m | data | data if s w = 01	4/16	
Immediate to accumulator	0001010w | data | data if w = 1	3/4	8/16-bit
INC = Increment			
Register/memory	1111111w | mod 000 r/m	3/15	
Register	01000 reg	3	
SUB = Subtract			
Reg./memory and register to either	001010dw | mod reg r/m	3/10	
Immediate from register/memory	100000sw | mod 101 r/m | data | data if s w = 01	4/16	
Immediate from accumulator	0010110w | data | data if w = 1	3/4	8/16-bit
SBB = Subtract with borrow:			
Reg./memory and register to either	000110dw | mod reg r/m	3/10	
Immediate from register/memory	100000sw | mod 011 r/m | data | data if s w = 01	4/16	
Immediate from accumulator	0001110w | data | data if w = 1	3/4	8/16-bit

Function	Format	Clock Cycles	Comments
Arithmetic (cont'd):			
DEC = **Decrement:**			
Register/memory	1 1 1 1 1 1 1 w | mod 0 0 1 r/m	3/15	
Register	0 1 0 0 1 reg	3	
CMP = **Compare:**			
Register/memory with register	0 0 1 1 1 0 1 w | mod reg r/m	3/10	
Register with register/memory	0 0 1 1 1 0 0 w | mod reg r/m	3/10	
Immediate with register/memory	1 0 0 0 0 0 s w | mod 1 1 1 r/m | data | data if s w=01	3/10	
Immediate with accumulator	0 0 1 1 1 1 0 w | data | data if w = 1	3/4	8/16-bit
NEG = Change sign	1 1 1 1 0 1 1 w | mod 0 1 1 r/m	3	
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1	8	
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1	4	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1	7	
DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1	4	
MUL = Multiply (unsigned):	1 1 1 1 0 1 1 w | mod 1 0 0 r/m		
register–byte		26–28	
register–word		35–37	
memory–byte		32–34	
memory–word		41–43	
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w | mod 1 0 1 r/m		
register–byte		25–28	
register–word		34–37	
memory–byte		31–34	
memory–word		40–43	

Function	Format	Clock Cycles	Comments
Arithmetic (cont'd):			
IMUL = Integer immediate multiply (signed)	011010s1 | mod reg r/m | data | data if s = 0	22–25/29–32	
DIV = Integer divide (unsigned):	1111011w | mod 110 r/m		
register–byte		29	
register–word		38	
memory–byte		35	
memory–word		44	
IDIV = Integer divide (signed):	1111011w | mod 111 r/m		
register–byte		44–52	
register–word		53–61	
memory–byte		50–58	
memory–word		59–67	
AAM = ASCII adjust for multiply	11010100 | 00001010	19	
AAD = ASCII adjust for divide	11010101 | 00001010	15	
CBW = Convert byte to word	10011000	2	
CWD = Convert word to double word	10011001	4	
Logic			
Shift/rotate instructions:			
Register/memory by 1	1101000w | mod TTT r/m	2/15	
Register/memory by CL	1101001w | mod TTT r/m	5+n/17+n	
Register/memory by count	1100000w | mod TTT r/m | count	5+n/17+n	

TTT	Instruction
000	ROL
001	ROR
010	RCL
011	RCR
100	SHL/SAL
101	SHR
111	SAR

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Logic (cont'd):			
AND = **And:**			
Reg./memory and register to either	0 0 1 0 0 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 1 0 0 r/m | data | data if w = 1	4/16	
Immediate to accumulator	0 0 1 0 0 1 0 w | data | data f w = 1	3/4	8/16-bit
TEST = **And function to flags, no result:**			
Register/memory and register	1 0 0 0 0 1 0 w | mod reg r/m	3/10	
Immediate data and register/memory	1 1 1 1 0 1 1 w | mod 0 0 0 r/m | data | data if w = 1	4/10	
Immediate data and accumulator	1 0 1 0 1 0 0 w | data | data if w = 1	3/4	8/16-bit
OR = **Or:**			
Reg./memory and register to either	0 0 0 0 1 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 0 0 1 r/m | data | data if w = 1	4/16	
Immediate to accumulator	0 0 0 0 1 1 0 w | data | data if w = 1	3/4	8/16-bit
XOR = **Exclusive Or:**			
Reg./memory and register to either	0 0 1 1 0 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 1 1 0 r/m | data | data if w = 1	4/16	
Immediate to accumulator	0 0 1 1 0 1 0 w | data | data if w = 1	3/4	8/16-bit
NOT = Invert register/memory	1 1 1 1 0 1 1 w | mod 0 1 0 r/m	3	

Function	Format	Clock Cycles	Comments
String Manipulation:			
MOVS = Move byte/word	1010010w	14	
CMPS = Compare byte/word	1010011w	22	
SCAS = Scan byte/word	1010111w	15	
LODS = Load byte/word to AL/AX	1010110w	12	
STOS = Store byte/word from AL/AX	1010101w	10	
INS = Input byte/word from DX port	0110110w	14	
OUTS = Output byte/word to DX port	0110111w	14	
Repeated by count in CX			
MOVS = Move string	11110010 1010010w	8 + 8n	
CMPS = Compare string	1111001z 1010011w	5 + 22n	
SCAS = Scan string	1111001z 1010111w	5 + 15n	
LODS = Load string	11110010 1010110w	6 + 11n	
STOS = Store string	11110010 1010101w	6 + 9n	
INS = Input string	11110010 0110110w	8 + 8n	
OUTS = Output string	11110010 0110111w	8 + 8n	

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Control Transfer:			
CALL = Call:			
Direct within segment	11101000 | disp-low | disp-high	15	
Register/memory indirect within segment	11111111 | mod 010 r/m	13/19	
Direct intersegment	10011010 | segment offset | segment selector	23	
Indirect intersegment	11111111 | mod 011 r/m (mod ≠ 11)	38	

Function	Format	Clock Cycles	Comments
Control Transfer (cont'd):			
JMP = Unconditional jump:			
Short/long	11101011 | disp-low	14	
Direct within segment	11101001 | disp-low | disp-high	14	
Register/memory indirect within segment	11111111 | mod 100 r/m	11/17	
Direct intersegment	11101010 | segment offset | segment selector	14	
Indirect intersegment	11111111 | mod 101 r/m (mod ≠ 11)	26	
RET = Return from CALL:			
Within segment	11000011	16	
Within seg. adding immediate to SP	11000010 | data-low | data-high	18	
Intersegment	11001011	22	
Intersegment adding immediate to SP	11001010 | data-low | data-high	25	

Function	Format		Clock Cycles	Comments
Control Transfer (cont'd):				
JE/JZ = Jump on equal/zero	01110100	disp	4/13	JMP not taken/JMP taken
JL/JNGE = Jump on less/not greater or equal	01111100	disp	4/13	
JLE/JNG = Jump on less or equal/not greater	01111110	disp	4/13	
JB/JNAE = Jump on below/not above or equal	01110010	disp	4/13	
JBE/JNA = Jump on below or equal/not above	01110110	disp	4/13	
JP/JPE = Jump on parity/parity even	01111010	disp	4/13	
JO = Jump on overflow	01110000	disp	4/13	
JS = Jump on sign	01111000	disp	4/13	
JNE/JNZ = Jump on not equal/not zero	01110101	disp	4/13	
JNL/JGE = Jump on not less/greater or equal	01111101	disp	4/13	
JNLE/JG = Jump on not less or equal/greater	01111111	disp	4/13	
JNB/JAE = Jump on not below/above or equal	01110011	disp	4/13	
JNBE/JA = Jump on not below or equal/above	01110111	disp	4/13	
JNP/JPO = Jump on not parity/parity odd	01111011	disp	4/13	
JNO = Jump on not overflow	01110001	disp	4/13	
JNS = Jump on not sign	01111001	disp	4/13	
JCXZ = Jump on CX zero	11100011	disp	5/15	
LOOP = Loop CX times	11100010	disp	6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp	6/16	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp	6/16	

Function	Format	Clock Cycles	Comments
Control Transfer (cont'd):			
ENTER = Enter procedure	11001000 | data-low | data-high | L		
L = 0		15	
L = 1		25	
L > 1		22 + 16(n−1)	
LEAVE = Leave procedure	11001001	8	
INT = **Interrupt:**			
Type specified	11001101 | type	47	
Type 3	11001100	45	
INTO = Interrupt on overflow	11001110	48/4	if INT taken/ if INT not taken
IRET = Interrupt return	11001111	28	
BOUND = Detect value out of range	01100010 | mod reg r/m	33–35	

Shaded areas indicate instructions not available on SAB 8086/8088 processors.

Function	Format	Clock Cycles	Comments
Processor Control			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{TEST}$ = 0
LOCK = Bus lock prefix	11110000	2	
ESC = Processor extension escape	11011TTT | mod LLL r/m (TTT LLL are op codes to processor extension)	6	

Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to +7V
Power dissipation	3 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±10%

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input low voltage	V_{IL}	−0.5	+0.8	V	–
Input high voltage (all except X1 and $\overline{RES}$)	V_{IH}	2.0	V_{CC} +0.5	V	–
Input high voltage ($\overline{RES}$)	V_{IH1}	3.0	V_{CC} +0.5	V	–
Output low voltage	V_{OL}	–	0.45	V	Ia = 2.5 mA for $\overline{S0}$-$\overline{S2}$ Ia = 2.0 mA for all other outputs
Output high voltage	V_{OH}	2.4	–	V	I_{OA} = −400 µA
Power supply current	I_{CC}	–	550	mA	T_A = 0°C; All outputs disconnected
		–	450	mA	T_A = 70°C; All outputs disconnected
Input leakage current	I_{LI}	–	±10	µA	0 V < V_{IN} < V_{CC}
Output leakage current	I_{LO}	–	±10	µA	0.45 V < V_{OUT} < V_{CC}
Clock output low	V_{CLO}	–	0.6	V	I_A = 4.0 mA
Clock output high	V_{CHO}	4.0	–	V	I_{OA} = −200 µA
Clock input low voltage	V_{CLI}	−0.5	0.6	V	–
Clock input high voltage	V_{CHI}	3.9	V_{CC} +1.0	V	–
Input capacitance	C_{IN}	–	10	pF	–
I/O capacitance	C_{IO}	–	20	pF	–

AC Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ±10%

Timing Requirements: all timings measured at 1.5 V unless otherwise specified

Parameter	Symbol	SAB 80186		SAB 80186-1		Unit	Test conditions
		min.	max.	min.	max.		
Data in setup (A/D)	t_{DVCL}	20	–	15	–	ns	–
Data in hold (A/D)	t_{CLDX}	10	–	8	–	ns	–
Asynchronous ready (ARDY) active setup time [1]	t_{ARYHCH}	20	–	15	–	ns	–
ARDY inactive setup time	t_{ARYLCL}	35	–	25	–	ns	–
ARDY hold time	t_{CHARYX}	15	–	15	–	ns	–
Asynchronous ready inactive hold time	t_{ARYCHL}	15	–	15	–	ns	–
Synchronous ready (SRDY) transition setup time	t_{SRYCL}	20	–	20	–	ns	–
SRDY transition hold time	t_{CLSRY}	15	–	15	–	ns	–
HOLD setup [1]	t_{HVCL}	25	–	20	–	ns	–
INTR, NMI, $\overline{\text{TEST}}$, TIMERIN, setup [1]	t_{INVCH}	25	–	25	–	ns	–
DRQ0, DRQ1, setup [1]	t_{INVCL}	25	–	20	–	ns	–

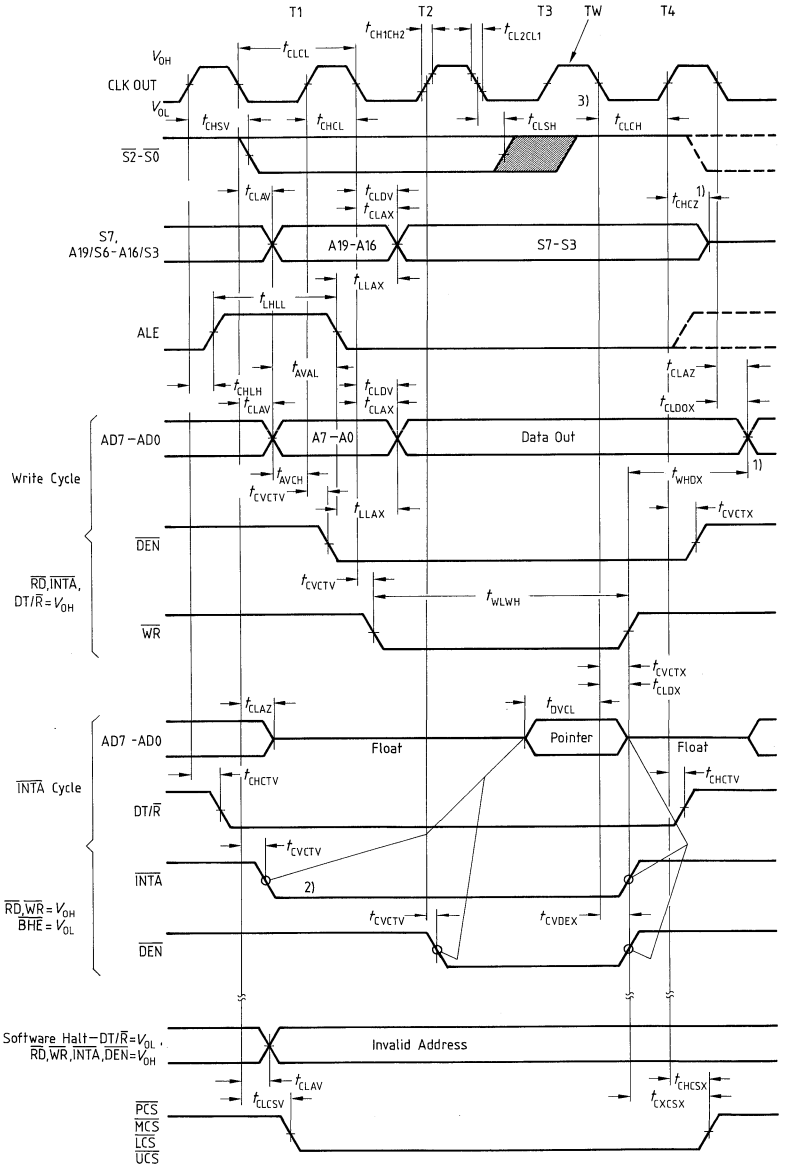
[1] To guarantee recognition at next clock.

Parameter	Symbol	SAB 80186		SAB 80186-1		Unit	Test conditions
		min.	max.	min.	max.		
Master Interfaces Timing Responses							
Address valid delay	t_{CLAV}	5	55	5	44	ns	C_L = 20 to 200 pF all outputs
Address hold	t_{CLAX}	10	–	10	–	ns	–
Address float delay	t_{CLAZ}	t_{CLAX}	35	t_{CLAX}	30	ns	–
Command lines float delay	t_{CHCZ}	–	45	–	40	ns	–
Command lines valid delay (after float)	t_{CHCV}	–	55	–	45	ns	–
ALE width	t_{LHLL}	t_{CLCL} -35	–	t_{CLCL} -30	–	ns	–
ALE active delay	t_{CHLH}	–	35	–	30	ns	–
ALE inactive delay	t_{CHLL}	–	35	–	30	ns	–
Address hold to ALE inactive	t_{LLAX}	t_{CHCL} -25	–	t_{CHCL} -20	–	ns	–
Data valid delay	t_{CLDV}	10	44	10	40	ns	–
Data hold time	t_{CLDOX}	10	–	10	–	ns	–
Data hold after WR	t_{WHDX}	t_{CLCL} -40	–	t_{CLCL} -34	–	ns	–
Control active delay 1	t_{CVCTV}	10	70	5	40	ns	–
Control active delay 2	t_{CHCTV}	10	55	10	44	ns	–
Control inactive delay	t_{CVCTX}	5	55	5	44	ns	–
$\overline{DEN}$ inactive delay (non-write cycle)	t_{CVDEX}	10	70	10	56	ns	–
Address float to $\overline{RD}$ active	t_{AZRL}	0	–	0	–	ns	–
$\overline{RD}$ active delay	t_{CLRL}	10	70	10	56	ns	–
$\overline{RD}$ inactive delay	t_{CLRH}	10	55	10	44	ns	–
$\overline{RD}$ inactive to address active	t_{RHAV}	t_{CLCL} -40	–	t_{CLCL} -40	–	ns	–
HLDA valid delay	t_{CLHAV}	5	50	5	40	ns	–
$\overline{RD}$ width	t_{RLRH}	2 t_{CLCL} -50	–	2 t_{CLCL} -46	–	ns	–
$\overline{WR}$ width	t_{WLWH}	2 t_{CLCL} -40	–	2 t_{CLCL} -34	–	ns	–
Address valid to ALE low	t_{AVAL}	t_{CLCH} -25	–	t_{CLCH} -19	–	ns	–
Status active delay	t_{CHSV}	10	55	10	45	ns	–
Status inactive delay	t_{CLSH}	10	65	10	50	ns	–
Timer output delay	t_{CLTMV}	–	60	–	48	ns	100 pF max.
Reset delay	t_{CLRO}	–	60	–	48	ns	–
Queue status delay	t_{CHQSV}	–	35	–	28	ns	–
Status hold time	t_{CHDX}	10	–	10	–	ns	–
Address valid to clock high	t_{AVCH}	10	–	10	–	ns	–
$\overline{LOCK}$ valid/invalid delay	t_{CLLV}	5	65	5	60	ns	–

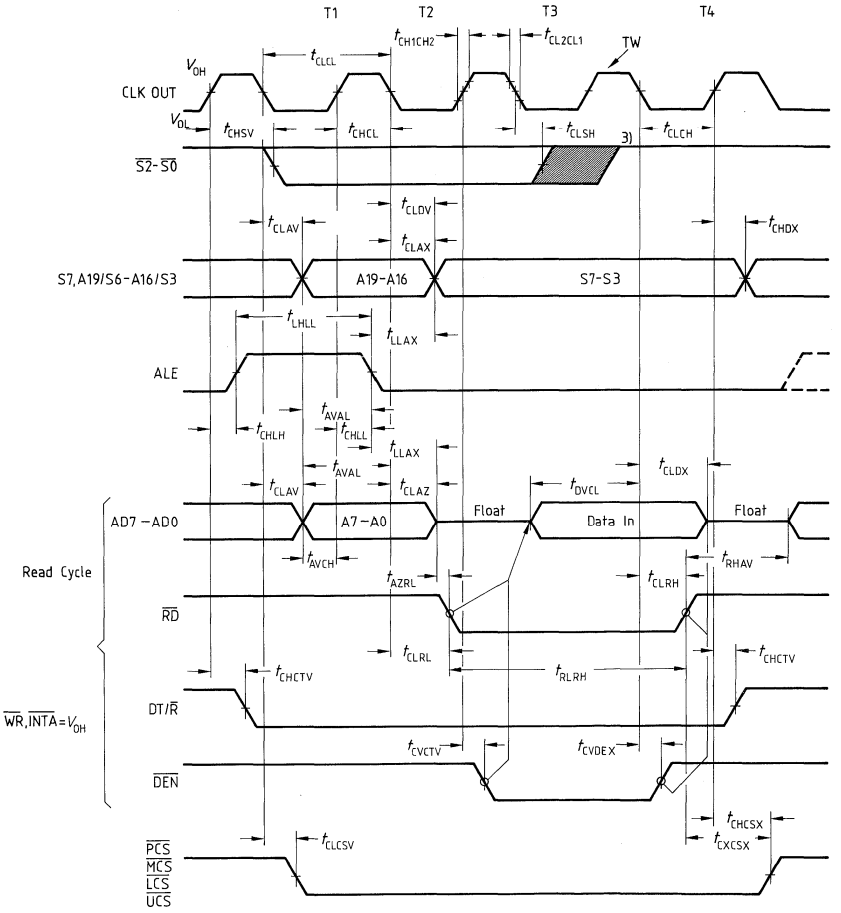
Parameter	Symbol	SAB 80186		SAB 80186-1		Unit	Test conditions
		min.	max.	min.	max.		
Chip Select Timing Responses							
Chip select active delay	t_{CLCSV}	–	66	–	45	ns	–
Chip select hold from command inactive	t_{CXCSX}	35	–	35	–	ns	–
Chip select inactive delay	t_{CHCSX}	5	35	5	32	ns	–
CLKIN Requirements							
CLKIN period	t_{CKIN}	62.5	250	50	250	ns	–
CLKIN fall time	t_{CKHL}	–	10	–	10	ns	3.5 to 1.0 V
CLKIN rise time	t_{CKLH}	–	10	–	10	ns	1.0 to 3.5 V
CLKIN low time	t_{CLCK}	25	–	20	–	ns	1.5 V
CLKIN high time	t_{CHCK}	25	–	20	–	ns	1.5 V
CLKOUT Timing (200 pF load)							
CLKIN to CLKOUT skew	t_{CICO}	–	50	–	25	ns	–
CLKOUT period	t_{CLCL}	125	500	100	500	ns	–
CLKOUT low time	t_{CLCH}	$1/2\ t_{CLCL} - 7.5$	–	$1/2\ t_{CLCL} - 6.0$	–	ns	1.5 V
CLKOUT high time	t_{CHCL}	$1/2\ t_{CLCL} - 7.5$	–	$1/2\ t_{CLCL} - 6.0$	–	ns	1.5 V
CLKOUT rise time	t_{CH1CH2}	–	15	–	12	ns	1.0 to 3.5 V
CLKOUT fall time	t_{CL2CL1}	–	15	–	12	ns	3.5 to 1.0 V

Waveforms

Major Cycle Timing



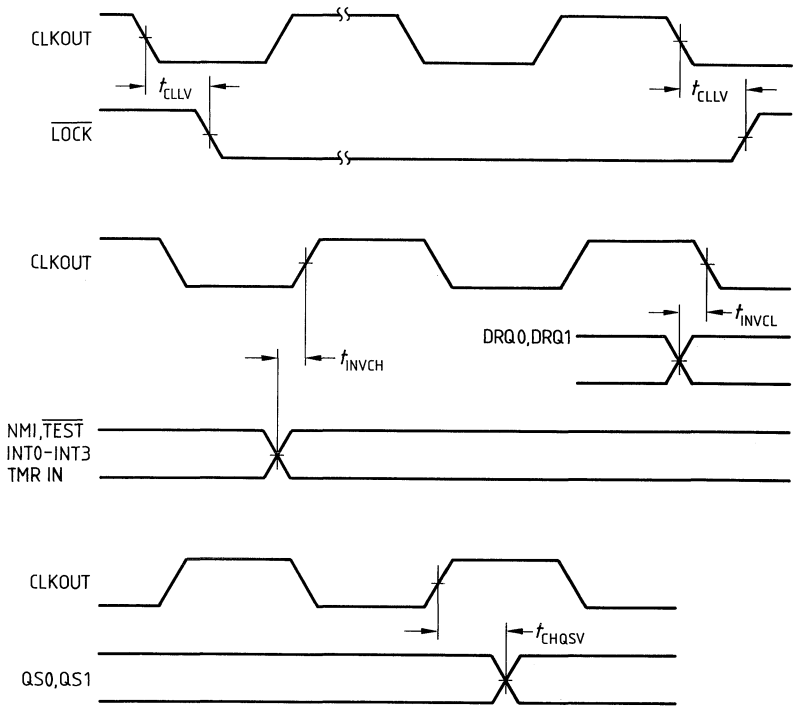
Major Cycle Timing (cont'd)



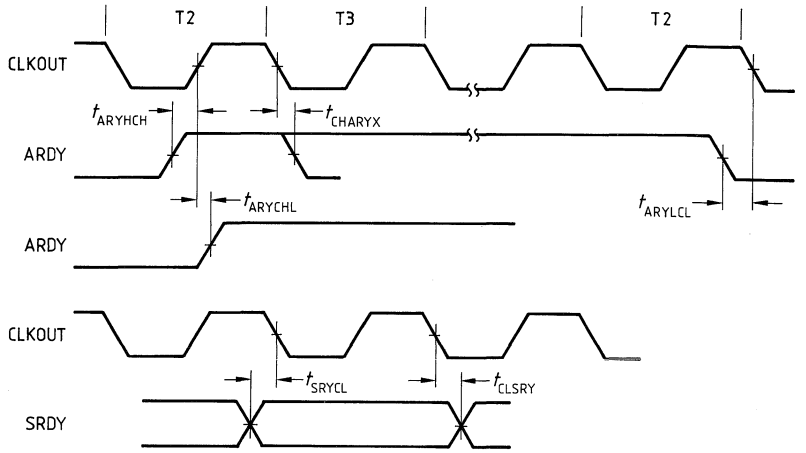
Notes

1) Following a write cycle, the local bus is tristated by the SAB 80186 only when the SAB 80186 enters a "hold acknowledge" state.
2) INTA occurs one clock later in iRMX mode.
3) Status inactive just prior to T4.

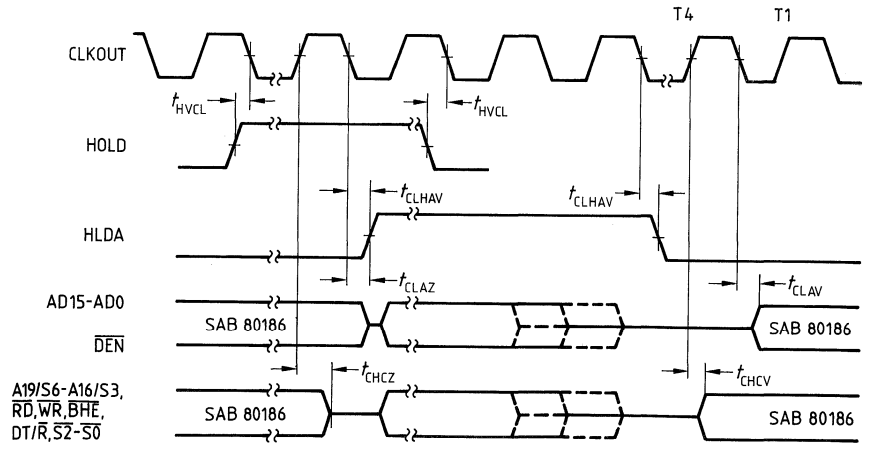
CLKOUT Timing Relationships



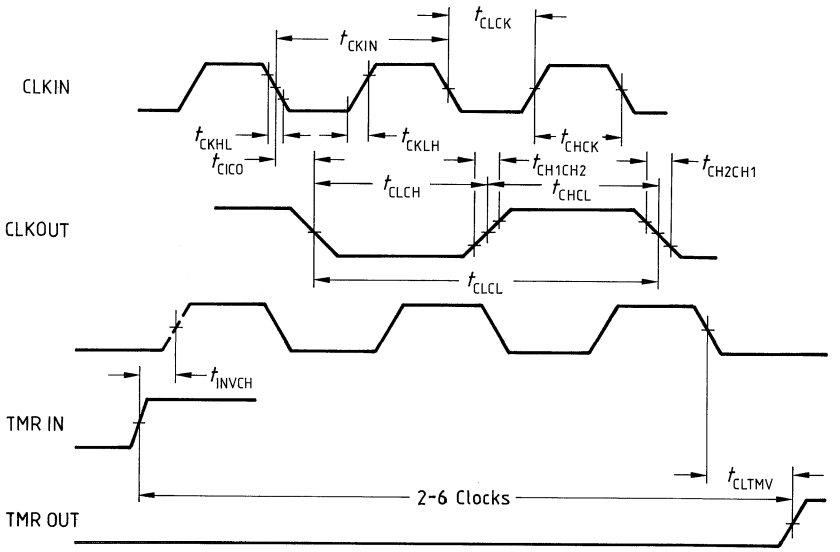
Ready Timing



HOLD-HLDA Timing

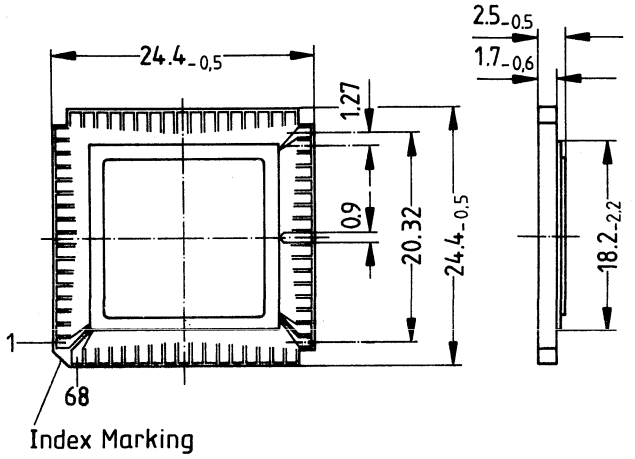


Timer Timing



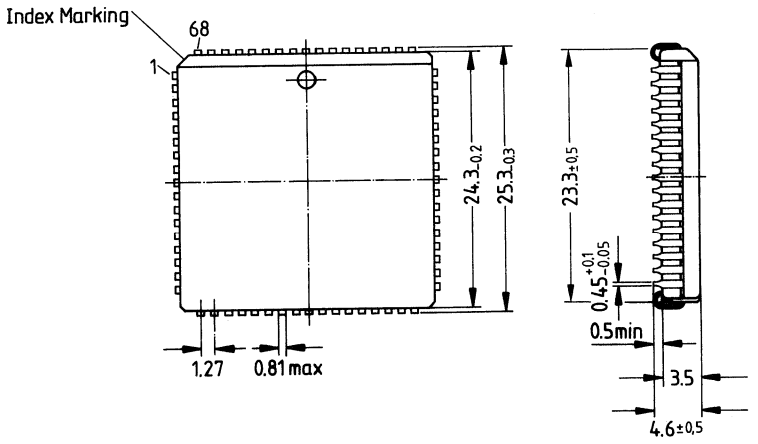
Package Outlines

68-pin Ceramic Package, C-CC-68



Dimensions in mm

68-pin Plastic Package, PL-CC-68, (SMD)



Dimensions in mm

Ordering Information

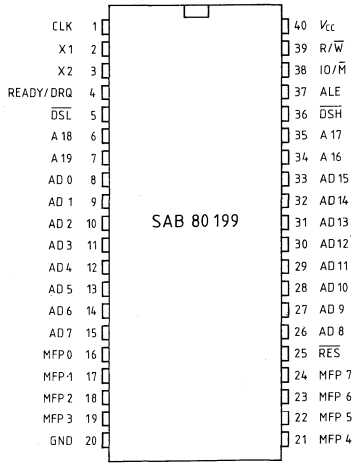
Type	Ordering code	Function
SAB 80186-N	Q67120-C250	16-bit microprocessor, 8 MHz (PL-CC)
SAB 80186-R	Q67120-C150	16-bit microprocessor, 8 MHz (C-CC)
SAB 80186-1-N	Q67120-C306	16-bit microprocessor, 10 MHz (PL-CC)
SAB 80186-1-R	Q67120-C291	16-bit microprocessor, 10 MHz (C-CC)

Advance Information

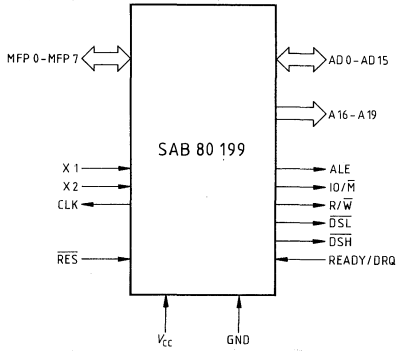
SAB 80199
16-Bit Terminal Processor

- High-performance 16-bit microprocessor
- Hardware-implemented task scheduler
- Multibank execution unit
- Handles up to eight concurrent tasks
- User-programmable multifunction I/O unit
- 1 Mbyte memory address space
- Instruction cycle 0.5 µs
- Very fast system response

Pin Configuration



Logic Symbol



General Description

The SAB 80199 is a new, high-performance 16-bit NMOS microprocessor dedicated to applications with extremely time-critical demands. It can control all functions of such devices as high-speed, letter-quality matrix printers.

The SAB 80199 can handle up to eight concurrent tasks, sufficient for the real-time control of many high-speed devices. It is the first microprocessor with a true hardware-implemented task scheduler and with a multibank execution unit. The integrated multifunction I/O unit is a very flexible, user-programmable mixture of three often needed peripherals: interrupt controller, multi-timer and serial communication controller.

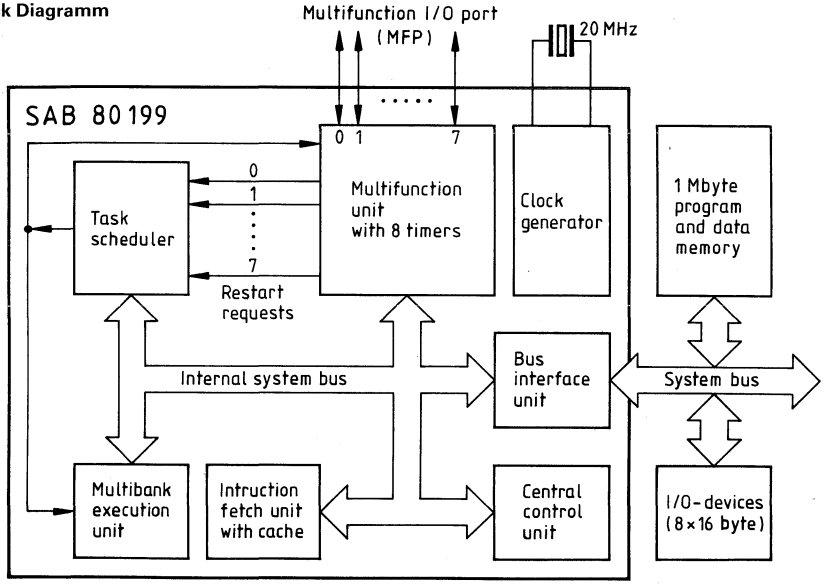
Program-Development Support Package

- Macroassembler, linker locater, library manager
- C-compiler
- Debug tools
  - System design kit
  - Software debugger
  - In-circuit emulator (ICE)
- Required host software/hardware:
  All programs run on 16-bit microcomputers supporting the universal development interface UDI/SRI 86 e.g.:
  - IBM-PC with UDI
  - Siemens PMS/SYS 900
  - Siemens PC-D, PC-16
  - Siemens/Intel MDS series III/IV

Applications

- Dedicated to critical real-time applications e.g.
  - High-speed letter-quality matrix printers
  - Printer-head control
  - Line-motor control
  - Carriage-motor control
  - Print-character generation
  - Extended communication capabilities

Block Diagramm



Ordering Information

Type	Ordering code	Description
SAB 80199	Q67100-A1961	P-DIP-40

ceramic package on request

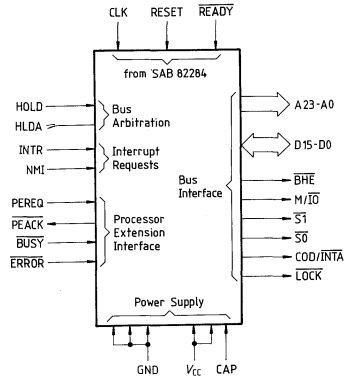
Preliminary

SAB 80286

High-Performance Microprocessor with Memory Management and Protection for Clock Rates up to 8 MHz, 10 MHz or 12.5 MHz

- High-performance processor (up to six times the SAB 8086)
- Large address space:
  - 16 megabytes physical
  - 1 gigabyte virtual per task
- High bandwidth bus interface (8 megabyte/s at 16 MHz system clock)
- Two SAB 8086 upward-compatible operating modes:
  - SAB 8086 real address mode
  - protected virtual address mode
- Integrated memory management, four-level memory protection and support for virtual memory and multitasking operating systems
- Full hardware and software support

Logic Symbol



Pin Names

A23-A0	Address Bus	HOLD	Bus.Hold Request
D15-D0	Data Bus	HLDA	Bus Hold Acknowledge
$\overline{S1}$, $\overline{S0}$	Bus Cycle Status	INTR	Interrupt Request
$\overline{BHE}$	Bus High Enable	NMI	Non-Maskable Interrupt Request
M/$\overline{IO}$	Memory/IO Select	PEREQ	Processor Extension Operand Request
COD/$\overline{INTA}$	Code/Interrupt Acknowledge		
$\overline{LOCK}$	Bus Lock	$\overline{PEACK}$	Processor Extension Operand Acknowledge
CLK	System Clock		
RESET	System Reset	$\overline{BUSY}$	Processor Extension Busy
$\overline{READY}$	Bus Ready	$\overline{ERROR}$	Processor Extension Error
CAP	Substrate Filter Capacitor	V_{CC}	Power Supply (+5 V)
		GND	Ground (0 V)

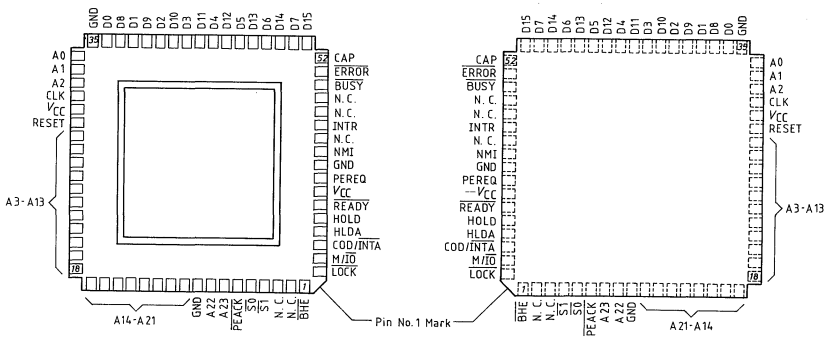
The SAB 80286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multitasking systems. The SAB 80286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. An 8 MHz SAB 80286 provides up to six times greater throughput than the standard 5 MHz SAB 8086. The SAB 80286 includes memory management capabilities that map up to 2^{30} (one gigabyte) of virtual address space per task into 2^{24} bytes (16 megabytes) of physical memory.
The SAB 80286 is upward-compatible with SAB 8086/8088 software. Using SAB 8086 real address mode, the SAB 80286 is object-code compatible with existing SAB 8086/8088 software. In protected virtual address mode, the SAB 80286 is source code compatible with SAB 8086/8088 software and may require upgrading to use virtual addresses supported by SAB 80286's integrated memory management and protection mechanism. Both modes operate at full SAB 80286 performance and execute a superset of the SAB 8086/8088 instructions.
The SAB 80286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The SAB 80286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.

Pin Configurations

C-CC Package

Component pad view – as viewed from underside of component when mounted on the board.

PC board view – as viewed from the component side of the pc board.

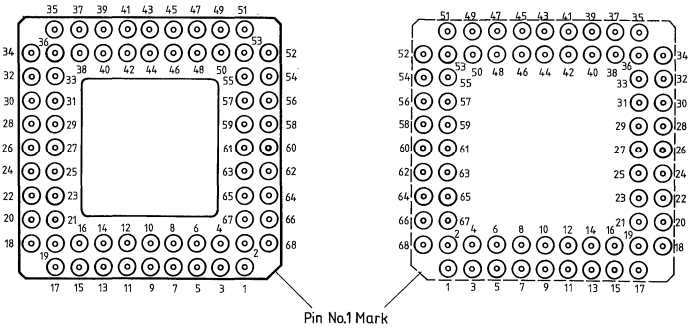


Note: N.C. pads must not be connected.

Pin Grid Array Package

Bottom view

Top view (PCB footprint)



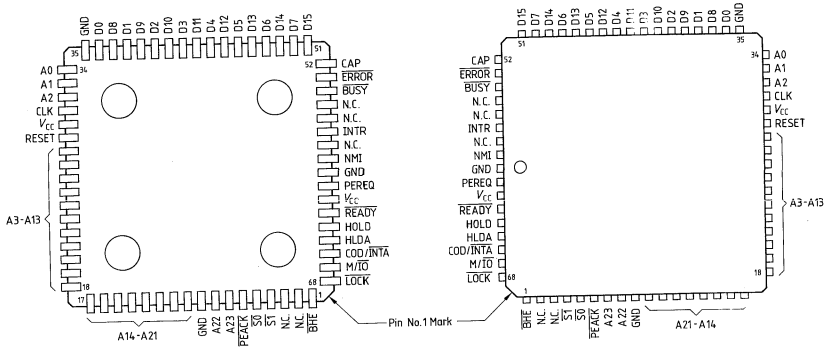
Note: The PGA footprint is identical with the C-CC package socket and PL-CC socket footprints.

Pin Configurations (cont'd)

PL-CC Package

Compact pad view – as viewed from underside of component when mounted on the board.

PC board view – as viewed from the component side of the pc board.



Note: N.C. pads must not be connected.

Pin Definitions and Functions

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{BHE}$</td><td>1</td><td>O</td><td>BUS HIGH ENABLE indicates transfer of data on the upper byte of the data bus D15-8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is active low and floats to tristate off during bus hold acknowledge.
<table>
<tr><th colspan="3">$\overline{BHE}$ and A0 encodings</th></tr>
<tr><th>$\overline{BHE}$ value</th><th>A0 value</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Word transfer</td></tr>
<tr><td>0</td><td>1</td><td>Byte transfer on upper half of data bus (D15-8)</td></tr>
<tr><td>1</td><td>0</td><td>Byte transfer on lower half of data bus (D7-0)</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>$\overline{S1}$, $\overline{S0}$</td><td>4, 5</td><td>O</td><td>BUS CYCLE STATUS indicates initiation of a bus cycle and, along with M/$\overline{IO}$ and COD/$\overline{INTA}$, defines the type of bus cycle. The bus is in a TS state whenever one or both are low, $\overline{S1}$ and $\overline{S0}$ are active low and float to tristate off during bus hold acknowledge.
<table>
<tr><th colspan="5">Bus cycle status definition</th></tr>
<tr><th>COD/$\overline{INTA}$</th><th>M/$\overline{IO}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Bus cycle initiated</th></tr>
<tr><td>0 (low)</td><td>0</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>None; not a status cycle</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>IF A1 = 1 then halt; else shutdown</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Memory data read</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Memory data write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>None; not a status cycle</td></tr>
<tr><td>1 (high)</td><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>I/O read</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>I/O write</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>None; not a status cycle</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Memory instruction read</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>None; not a status cycle</td></tr>
</table></td></tr>
</table>

Pin Definitions and Functions (cont'd)

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>A23–A0</td><td>7 – 34</td><td>O</td><td>ADDRESS BUS outputs physical memory and I/O port addresses. A0 is low when data is to be transferred on pins D7–0. A23–A10 are low during I/O transfers. The address bus is active high and floats to tristate off during bus hold acknowledge.</td></tr>
<tr><td>RESET</td><td>29</td><td>I</td><td>SYSTEM RESET clears the internal logic of the SAB 80286 and is active high. The SAB 80286 may be reinitialized at any time with a low-to-high transition on RESET which remains active for more than 16 system clock cycles. During RESET active, the output pins of the SAB 80286 enter the state shown below:
<table><tr><th colspan="2">Pin state during reset</th></tr><tr><th>Pin value</th><th>Pin names</th></tr><tr><td>1 (high)
0 (low)
Tristate off</td><td>$\overline{S0}$, $\overline{S1}$, $\overline{PEACK}$, A23–A0, $\overline{BHE}$, $\overline{LOCK}$
M/$\overline{IO}$, COD/$\overline{INTA}$, HLDA
D15 – D0</td></tr></table>Operation of the SAB 80286 begins after a high-to-low transition on RESET. The high-to-low transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles from the trailing edge of RESET are required by the SAB 80286 for internal initialization before performing the first bus cycle to fetch code from the power-on execution address.
A low-to-high transition of RESET synchronous to the system clock will end a processor cycle at the second high-to-low transition of the system clock. The low-to-high transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous low-to-high transitions of RESET are required only for systems where the processor clock must be phase-synchronous to another clock.</td></tr>
<tr><td>CLK</td><td>31</td><td>I</td><td>SYSTEM CLOCK provides the fundamental timing for SAB 80286 systems. It is divided by two (inside the SAB 80286) to generate the processor clock. The internal divide-by-two circuitry can be synchronized to an external clock generator by a low-to-high transition on the RESET input.</td></tr>
<tr><td>D15 – D0</td><td>36 – 51</td><td>I
O</td><td>DATA BUS inputs data during memory, I/O, and interrupt acknowledge read cycles: outputs data during memory and I/O write cycles. The data bus is active high and floats to tristate off during bus hold acknowledge.</td></tr>
<tr><td>$\overline{BUSY}$
$\overline{ERROR}$</td><td>53, 54</td><td>I
I</td><td>PROCESSOR EXTENSION BUSY AND ERROR indicate the operating condition of a processor extension to the SAB 80286. An active $\overline{BUSY}$ input stops the SAB 80286 program execution on WAIT and some ESC instructions until $\overline{BUSY}$ becomes inactive (high). The SAB 80286 may be interrupted while waiting for $\overline{BUSY}$ to become inactive. An active $\overline{ERROR}$ input causes the SAB 80286 to perform a processor extension interrupt when executing WAIT or some ESC instructions. These inputs are active low and may be asynchronous to the system clock.</td></tr>
</table>

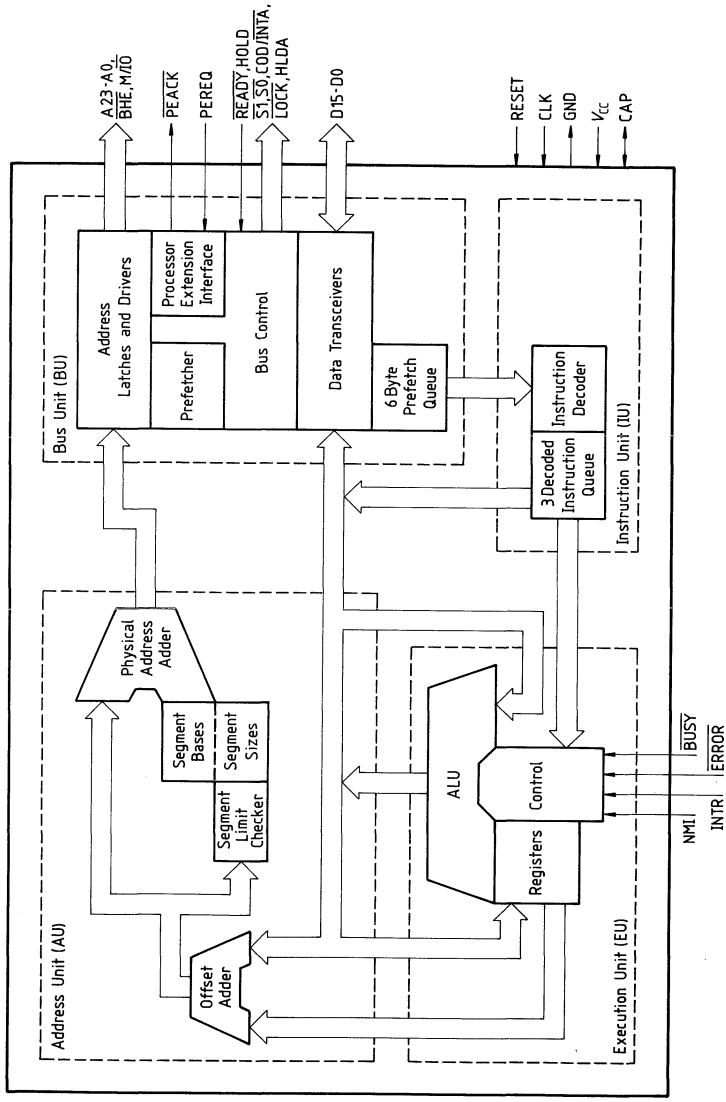
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
INTR	57	I	**INTERRUPT REQUEST** requests the SAB 80286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the SAB 80286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To assure program interruption, INTR must remain active until the first interrupt acknowledge cycle is completed. INTR is sampled at the beginning of each processor cycle and must be active high at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active high, and may be asynchronous to the system clock.
NMI	59	I	**NON-MASKABLE INTERRUPT REQUEST** interrupts the SAB 80286 with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the SAB 80286 flag word does not affect this input. The NMI input is active high, may be asynchronous to the system clock, and is edge-triggered after internal synchronization. For proper recognition, the input must have been previously low for at least four system clock cycles and remain high for at least four system clock cycles.
PEREQ $\overline{\text{PEACK}}$	1 6	I O	**PROCESSOR EXTENSION OPERAND REQUEST AND ACKNOWLEDGE** extend the memory management and protection capabilities of the SAB 80286 to processor extensions. The PEREQ input requests the SAB 80286 to perform a data operand transfer for a processor extension. The $\overline{\text{PEACK}}$ output signals the processor extension when the requested operand is being transferred. PEREQ is active high. $\overline{\text{PEACK}}$ is active low and floats to tristate off during bus hold acknowledge. $\overline{\text{PEACK}}$ may be asynchronous to the system clock.
$\overline{\text{READY}}$	63	I	**BUS READY** terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{\text{READY}}$ low. $\overline{\text{READY}}$ is an active low synchronous input requiring setup and hold times relative to the system clock be met for correct operation. $\overline{\text{READY}}$ is ignored during bus hold acknowledge.
HOLD HLDA	64 65	I O	**BUS HOLD REQUEST AND HOLD ACKNOWLEDGE** control ownership of the SAB 80286 local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the SAB 80286 will float its bus drivers to tristate off and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the SAB 80286 deactivating HLDA and regaining control of the local bus. This terminates the bus hold acknowledge condition, HOLD may be asynchronous to the system clock. These signals are active high.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
COD/$\overline{\text{INTA}}$	66	O	**CODE/INTERRUPT ACKNOWLEDGE** distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/$\overline{\text{INTA}}$ floats to tristate off during bus hold acknowledge.
M/$\overline{\text{IO}}$	67	O	**MEMORY / I/O SELECT** distinguishes memory access from I/O access. If high during TS, a memory cycle or a halt/shutdown cycle is in progress. If low, an I/O cycle or an interrupt acknowledge cycle is in progress M/$\overline{\text{IO}}$ floats to tristate off during bus hold acknowledge.
$\overline{\text{LOCK}}$	68	O	**BUS LOCK** indicates that other system bus masters are not to gain control of the system bus following the current bus cycle. The $\overline{\text{LOCK}}$ signal may be activated explicitly by the "LOCK" instruction prefix or automatically by SAB 80286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{\text{LOCK}}$ is active low and floats to tristate off during bus hold acknowledge.
V_{CC}	30, 62	–	**POWER SUPPLY** (+5 V)
GND	9, 35, 60	–	**GROUND** (0 V)
CAP	52	I	**SUBSTRATE FILTER CAPACITOR**: a 0.047 µF ±20% 12 V capacitor must be connected between this pin and ground. This capacitor filters the output of the internal substrate bias generator. A maximum DC leakage current of 1 µA is allowed through the capacitor. For correct operation of the SAB 80286 the substrate bias generator must charge this capacitor to its operating voltage. The capacitor's charging time is 5 milliseconds (max.) after V_{CC} and CLK reach their specified AC and DC parameters. RESET may be applied to prevent spurious activity by the CPU during this time. After this time, the SAB 80286 processor clock can be phase-synchronized to another clock by pulsing RESET low synchronous to the system clock.

Internal Block Diagram



Functional Description

Introduction

The SAB 80286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multitasking systems. Depending on the application, the SAB 80286's performance is up to six times faster than that of the standard 5 MHz SAB 8086, while providing complete upward software compatibility with the Siemens 16-bit CPU family (SAB 8086/88, SAB 80186/88).

The SAB 80286 operates in two modes: real address mode (8086 mode) and protected virtual address mode. Both modes execute a superset of the SAB 8086/88 instruction set. In real address mode programs use real addresses with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the SAB 80286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each task's programs and data. Both modes provide the same basic instruction set, registers, and addressing modes.
The following functional description describes first the basic SAB 80286 architecture common to both modes, second the real address mode, and third the protected mode.

Basic Architecture

The processors of the Intel/Siemens 16-bit CPU family all contain the same basic set of registers, instructions, and addressing modes. Therefore, the SAB 80286 processor is upward-compatible with the SAB 8086, 8088 and 80186 CPUs.

Register Set

The SAB 80286 basic architecture has fifteen registers as shown below. These registers are grouped into the following four categories:

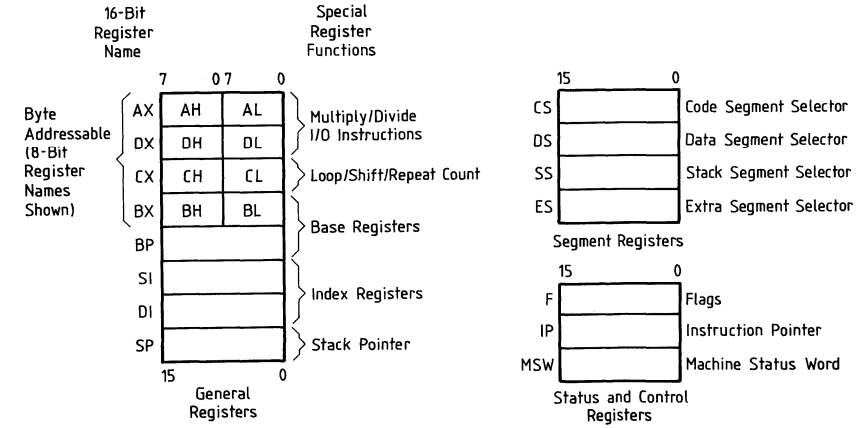
General registers: Eight 16-bit general purpose registers used to contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used either in their entirety as 16-bit words or split into pairs of separate 8-bit registers.

Segment registers: Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data (For usage, refer to Memory Organization).

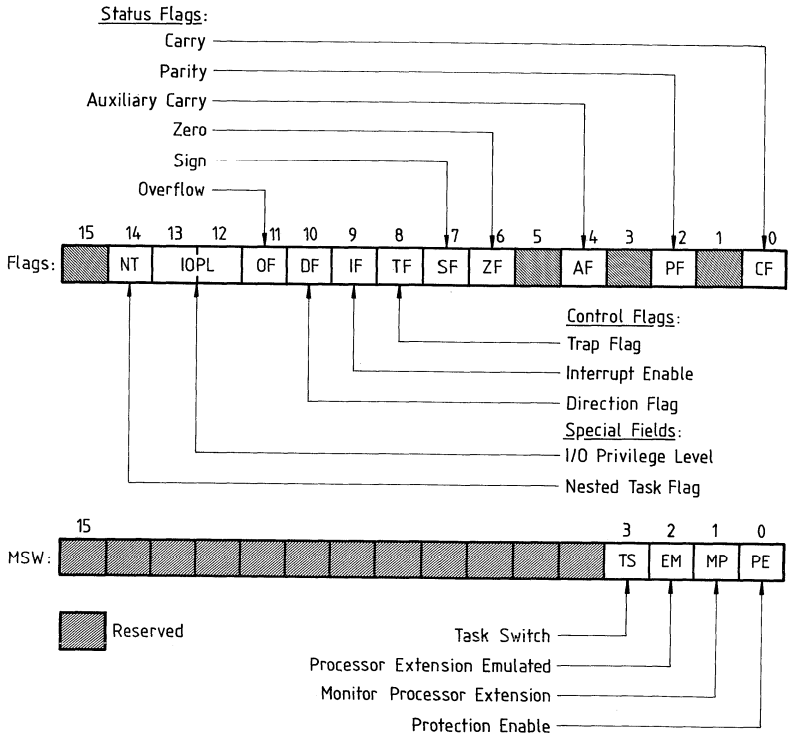
Base and index registers: Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode determines the specific registers used for operand address calculations.

Status and control registers: The three 16-bit special purpose registers in the figure below record or control certain aspects of the SAB 80286 processor state including the instruction pointer which contains the offset address of the next sequential instruction to be executed.

Register Set



Status and Control Register Bit Functions



Flags Word Description

The flags word (flags) records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 7, and 11) and controls the operation of the SAB 80286 within a given operating mode (bits 8 and 9). Flags is a 16-bit register. The function of the flag bits is given in table 1.

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high level instructions, and processor control.

An SAB 80286 instruction can reference zero, one, or two operands; where an operand resides in a register, in the instruction itself, or in memory. Zero-operand instructions (e.g. HLT) are usually one byte long. One-operand instructions (e.g. INC and DEC) are usually two bytes long but some are encoded in only one byte. One-operand instructions may reference a register or memory location.

Two-operand instructions permit the following six types of instruction operations:

- register to register
- memory to register
- immediate data to register
- memory to memory
- register to memory
- immediate data to memory

Two-operand instructions (e.g. MOV and ADD) are usually three to six bytes long. Memory-to-memory operations are provided by a special class of string instructions requiring one to three bytes. For detailed instruction formats and encodings refer to the instruction set summary.

Table 1
Flags Word Bit Functions

Bit position	Name	Functions
0	CF	Carry Flag – Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag – Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low-order 4 bits of AL; cleared otherwise
6	ZF	Zero Flag – Set if result is zero; cleared otherwise
7	SF	Sign Flag – Set equal to high-order bit of result (0 if positive, 1 if negative)
11	OF	Overflow Flag – Set if result is a positive number too large or a negative number too small (excluding sign bit) to fit in destination operand; cleared otherwise
8	TF	Single Step Flag – Once set, a single step interrupt occurs after the next instruction has been executed. TF is cleared by the single step interrupt
9	IF	Interrupt Enable Flag – When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location
10	DF	Direction Flag – Causes string instructions to autodecrement the appropriate index registers when set. Clearing DF causes autoincrement

Memory Organization

Memory is organized as sets of variable length segments. Each segment is a linear contiguous sequence of up to 64 K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit segment selector, and a 16-bit offset. The segment selector indicates the desired segment in memory. The offset component indicates the desired byte address within the segment.

All instructions that address operands in memory must specify the segment and the offset. For speed and compact instruction encoding, segment selectors are usually stored in the high-speed segment registers. An instruction needs to specify only the desired segment register and an offset in order to address a memory operand.

Most instructions need not explicity specify which segment register is used. The correct segment register is automatically chosen according to the rules of table 2.

These rules follow the way programs are written as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs. To access operands not residing in one of the four immediately available segments, a full 32-bit pointer or a new segment selector must be loaded.

I/O Space

The I/O space consists of 64 K 8-bit or 32 K 16-bit ports. I/O instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register, 8-bit port addresses are zero extended such that A15-A8 are low. I/O port addresses 00F8(H) through 00FF(H) are reserved.

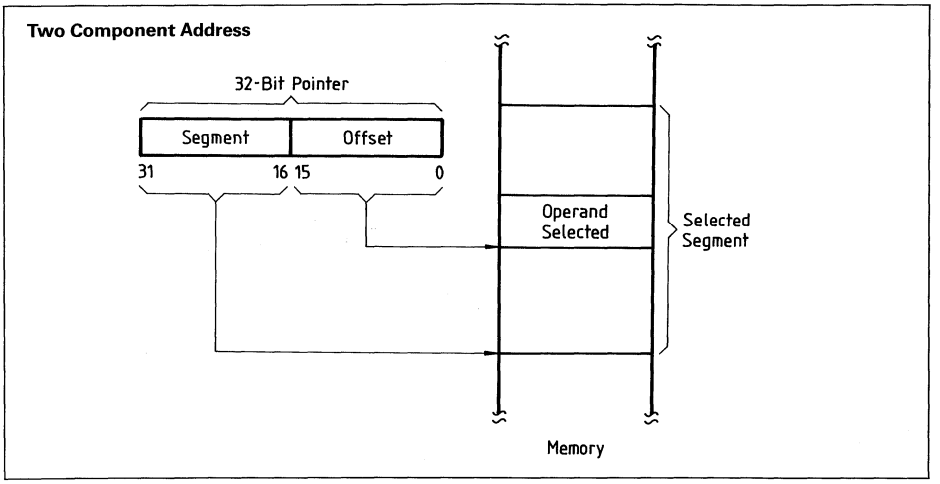


Table 2
Segment Register Selection Rules

Memory reference needed	Segment register used	Implicit segment selection rule
Instructions	Code (CS)	Automatic with instruction prefetch
Stack	Stack (SS)	All stack pushes and pops. Any memory reference which uses BP as a base register
Local data	Data (DS)	All data references except when relative to stack or string destination
External (global) data	Extra (ES)	Alternate data segment and destination of string operation

Addressing Modes

The SAB 80286 provides a total of eight adressing modes for instructions to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

Register operand mode: The operand is located in one of the 8 or 16-bit general registers.

Immediate operand mode: The operand is included in the instruction.

Direct mode: The operand's offset is contained in the instruction as an 8 or 16-bit displacement element.

Register indirect mode: The operand's offset is in one of the registers SI, DI, BX, or BP.

Based mode: The operand's offset is the sum of an 8 or 16-bit displacement and the contents of a base register (BX or BP).

Indexed mode: The operand's offset is the sum of an 8 or 16-bit displacement and the contents of an index register (SI or DI).

Based indexed mode: The operand's offset is the sum of the contents of a base register and an index register.

Based indexed mode with displacement: The operand's offset is the sum of a base register's contents, an index register's contents, and an 8 or 16-bit displacement.

Data Types

The SAB 80286 directly supports the following data types:

Integer:
A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32 and 64-bit integers are supported using the numeric data processor extension.

Ordinal:
An unsigned binary numeric value contained in an 8-bit byte or 16-bit word.

Pointer:
A 32-bit quantity, composed of a segment selector component and an offset component. Each component is a 16-bit word.

String:
A contiguous sequence of bytes or words. A string may contain between 1 byte and 64 Kbytes.

ASCII:
A byte representation of alphanumeric and control characters using the ASCII standard of character representation.

BCD:
A byte (unpacked) representation of the decimal digits 0 to 9.

Packed BCD:
A byte (packed) representation of two decimal digits 0 to 9 storing one digit in each nibble of the byte.

Floating Point:
A signed 32, 64, or 80-bit real number representation (Floating point operands are supported using the extended processor configuration with SAB 80287).

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (flags) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware-initiated interrupts occur in response to an external input and are classifield as non-maskable or maskable. Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. The return address from an exception will always point at the instruction causing the exception and include any leading instruction prefixes.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0 to 31, some of which are used for instruction exceptions, are reserved. For each interrupt, an 8-bit vector must be supplied to the SAB 80286 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

Single Step Interrupt

The SAB 80286 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single step interrupt and is controlled by the single step flag bit (TF) in the flag word. Once this bit is set, an internal single step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single-stepped.

Interrupt Priorities

When simultaneous interrupt requests occur, they are processed in a fixed order as shown in table 4. Interrupt processing involves saving the flags, return address, and setting CS:IP to point at the first instruction of the interrupt handler. If other interrupts remain enabled they are processed before the first instruction of the current interrupt handler is executed. The last interrupt processed is therefore the first one serviced.

Table 3
Interrupt Vector Assignments

Function	Interrupt Number	Related instructions	Return address before instruction causing exception?
Divide error exception	0	DIV, IDIV	Yes
Single step interrupt	1	All	–
NMI interrupt	2	All	–
Breakpoint interrupt	3	INT	–
INT0 detected overflow exception	4	INT0	No
BOUND range exceeded exception	5	BOUND	Yes
Invalid op code exception	6	any undefined op code	Yes
Processor extension not available exception	7	ESC or WAIT	Yes
Reserved	8–15		–
Processor extension error interrupt	16	ESC or WAIT	–
Reserved	17–31		–
User defined	32–255		–

Table 4
Interrupt Processing Order

Order	Interrupt
1	Instruction exception
2	Single step
3	NMI
4	Processor extension segment overrun
5	INTR
6	INT instruction

Initialization and Processor Reset

Processor initialization or start up is accomplished by driving the RESET input pin high. RESET forces the SAB 80286 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as RESET is active. After RESET became inactive and an internal processing interval has elapsed, the SAB 80286 begins execution in real address mode with the instruction at physical location FFFFF0(H). RESET also sets some registers to predefined values as shown in table 5.
A23 to A20 will be high when the SAB 80286 performs memory references relative to the CS register until CS is changed. A23 to A20 will be zero for references to the DS, ES, or SS segments.

Changing CS in real address mode will force A23 to A20 low whenever CS is used again. The initial CS:IP value of F000:FFF0 provides 64 Kbytes of code space for initialization code without changing CS.

Table 5
SAB 80286 Initial Register State after RESET

Flag word	0002(H)
Machine status word	FFF0(H)
Instruction pointer	FFF0(H)
Code segment	F000(H)
Data segment	0000(H)
Extra segment	0000(H)
Stack segment	0000(H)

Machine Status Word Description

The machine status word (MSW) records when a task switch takes place and controls the operating mode of the SAB 80286. It is a 16-bit register of which the lower four bits are used. One bit places the CPU into protected mode, while the other three bits, as shown in table 6, control the processor extension interface. After RESET, this register contains FFF0(H) which place the SAB 80286 in real address mode.

The LMSW and SMSW instructions can load and store the MSW in real address mode. The recommended use of TS, EM, and MP is shown in table 7.

Table 6
MSW Bit Functions

Bit position	Name	Function
0	PE	**P**rotected mode **e**nable places the SAB 80286 into protected mode and cannot be cleared except by RESET
1	MP	**M**onitor **p**rocessor extension allows WAIT instructions to cause a processor extension not present exception (number 7)
2	EM	**Em**ulate processor extension causes a processor extension not present exception (number 7) on ESC instructions to allow emulating a processor extension
3	TS	**T**ask **s**witched indicates that the next instruction using a processor extension will cause exception 7, allowing software to test whether the current processor extension context belongs to the current task

Table 7
Recommended MSW Encodings For Processor Extension Control

TS	MP	EM	Recommended use	Instructions causing exception 7
0	0	0	Initial encoding after RESET. SAB 20286 operation is identical with SAB 8086/88 operation	none
0	0	1	No processor extension is available. Software will emulate its function	ESC
1	0	1	No processor extension is available. Software will emulate its function. The current processor extension context may belong to another task	ESC
0	1	0	A processor extension exists	none
1	1	0	A processor extension exists. The current processor extension context may belong to another task. The exception on WAIT allows software to test for an error pending from a previous processor extension operation	ESC or WAIT

Halt

The HLT instruction stops program execution and prevents the CPU from using the local bus until restarted. Either NMI, INTR with IF = 1, or RESET will force the SAB 80286 out of halt. If interrupted the saved CS:IP will point to the next instruction after the HLT.

Real Address Mode

The SAB 80286 executes a fully upward-compatible superset of the SAB 8086's instruction set in real address mode. In real address mode, the SAB 80286 is object code compatible with SAB 8086 and SAB 8088 software. The real address mode architecture (registers and addressing modes) is exactly as described in the SAB 80286 basic architecture section of this functional description.

Memory Size

Physical memory is a contiguous array of up to 1,048,576 bytes (one megabyte) addressed by pins A0 through A19 and $\overline{BHE}$. A20 through A23 may be ignored.

Memory Addressing

In real address mode the processor generates 20-bit physical addresses directly from a 20-bit-segment base address and a 16-bit offset.

The selector portion of a pointer is interpreted as the upper 16 bits of a 20-bit segment address. The lower four bits of the 20-bit segment addresses are always zero. Segment addresses, therefore, begin on multiples of 16 bytes. See figure on address calculation for a graphic representation of address formation.

All segments in real address mode are 64 Kbytes in size and may be read, written, or executed. An exception or interrupt can occur if data operands or instructions attempt to wrap around the end of a segment (e.g. a word with its low-order byte at offset FFFF(H) and its high-order byte at offset 0000(H). If, in real address mode, the information contained in a segment does not use the full 64 Kbytes, the unused end of the segment may be overlayed by another segment to reduce physical memory requirements.

Real Address Mode, Address Calculation

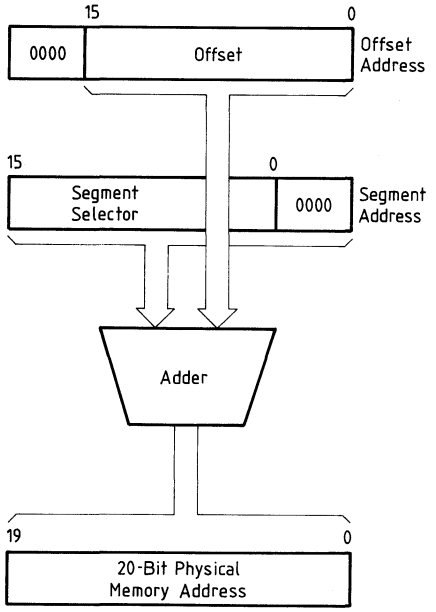


Table 8
Real Address Mode, Addressing Interrupts

Function	Interrupt number	Related instructions	Return address before instruction?
Interrupt table limit too small exception	8	INT vector is not within table limit	Yes
Processor extension segment overrun interrupt	9	ESC with memory operand extending beyond offset FFFF(H)	No
Segment overrun exception	13	Word memory reference with offset = FFFF(H) or an attempt to execute past the end of a segment	Yes

Interrupts

Table 8 shows the interrupt vectors reserved for exceptions and interrupts which indicate an addressing error. The exceptions leave the CPU in the state existing before attempting to execute the failing instruction (except for PUSH, POP, PUSHA, or POPA).

Shutdown

Shutdown occurs when a severe error is detected that prevents further instruction processing by the CPU. Shutdown and halt are externally signalled via a halt bus operation. They can be distinguished by A1 high for halt and A1 low for shutdown. In real address mode, shutdown can occur under two conditions:

- Exceptions 8 or 13 happen and the IDT limit does not include the interrupt vector.
- A CALL, INT or POP instruction attempts to wrap around the stack segment when SP is not even.

An NMI input can bring the CPU out of shutdown if the IDT limit is at least 000F(H) and SP is greater than 0005(H), otherwise shutdown can only be exited via the RESET input.

Protected Virtual Address Mode

The SAB 80286 executes a fully upward-compatible superset of the SAB 8086 instruction set in protected virtual address mode (protected mode). Protected mode also provides memory management and protection mechanisms and associated instructions.

The SAB 80286 enters protected virtual address mode from real address mode by setting the PE (Protection Enable) bit of the machine status word with the Load Machine Status Word (LMSW) instruction. Protected mode offers extended physical and virtual memory address space, memory protection mechanisms, and new operations to support operating system and virtual memory.

All registers, instructions and addressing modes described in the SAB 80286 basic architecture section of the functional description remain the same. Programs for the SAB 8086, SAB 8088, SAB 80186 and real address mode SAB 80286 can be run in protected mode: however, embedded constants for segment selectors are different.

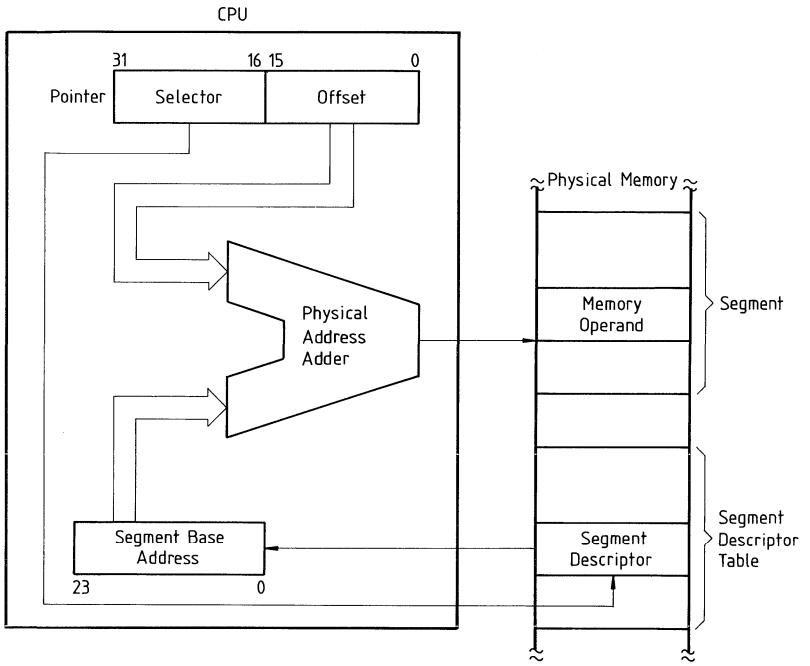
Memory Size

The protected mode SAB 80286 provides a 1 gigabyte virtual address space per task mapped into a 16 megabyte physical address space defined by the address pins A23–A0 and $\overline{BHE}$. The virtual address space may be larger than the physical address space since any use of an address that does not map to a physical memory location will cause a restartable exception.

Memory Addressing

As in real address mode, protected mode uses 32-bit pointers, consisting of 16-bit selector and offset components. The selector, however, specifies an index into a memory resident table rather than the upper 16-bits of a real memory address. The 24-bit base address of the desired segment is obtained from the tables in memory. The 16-bit offset is added to the segment base address to form the physical address as shown in the figure below. The tables are automatically referenced by the CPU whenever a segment register is loaded with a selector. All SAB 80286 instructions which load a segment register will reference the memory-based tables without additional software. The memory-based tables contain 8 byte values called descriptors.

Protected Mode, Memory Addressing



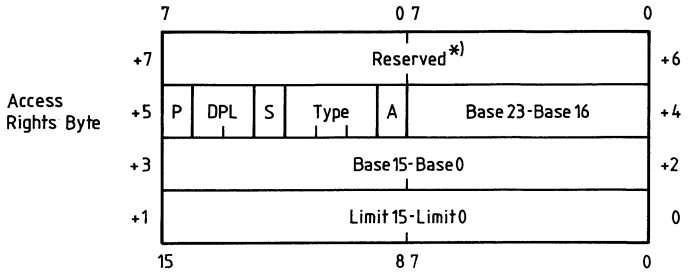
Descriptors

Descriptors define the use of memory. Special types of descriptors also define new functions for transfer of control and task switching. The SAB 80286 has segment descriptors for code, stack and data segments, as well as system control descriptors for special system data segments and control transfer operations. Descriptor accesses are performed as locked bus operations to assure descriptor integrity in multiprocessor systems.

Code and data segment descriptors (S = 1)

Besides segment base addresses, code and data descriptors contain other segment attributes including segment size (1 to 64 Kbytes), access rights (read only, read/write, execute only, and execute/read), and presence in memory (for virtual memory systems; figure and table next page). Any segment usage violating a segment attribute indicated by the segment descriptor will prevent the memory cycle and cause an exception or interrupt.

Code or Data Segment Descriptor



*) Must be set to 0 for compatibility with SAB 80386

Access Rights Byte Definition

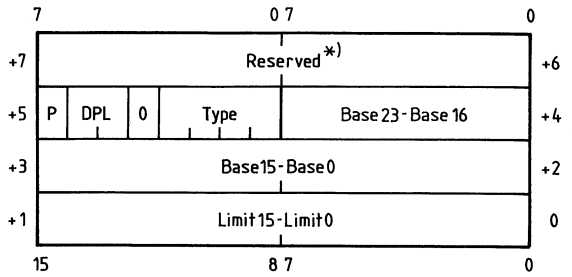
	Bit Position	Name		Function	
	7	Present (P)	P = 1	Segment is mapped into physical memory	
			P = 0	No mapping to physical memory exists, base and limit are not used	
	6-5	Descriptor privilege level (DPL)		Segment privilege attribute used in privilege tests	
	4	Segment descriptor (S)	S = 1	Code or data (includes stacks) segment descriptor	
			S = 0	System segment descriptor or gate descriptor	
Type field definition	3	Executable (E)	E = 0	Data segment descriptor type is:	If data segment (S = 1, E = 0)
	2	Expansion direction (ED)	ED = 0	Expand up segment, offsets must be ≤ limit	
			ED = 1	Expand down segment, offsets must be > limit	
	1	Writeable (W)	W = 0	Data segment may not be written into	
			W = 1	Data segment may be written into	
	3	Executable (E)	E = 1	Code segment descriptor type is:	If code segment (S = 1, E = 1)
	2	Conforming (C)	C = 1	Code segment may only be executed when CPL ≥ DPL and CPL remains unchanged	
	1	Readable (R)	R = 0	Code segment may not be read	
			R = 1	Code segment may be read	
	0	Accessed (A)	A = 0	Segment has not be accessed	
			A = 1	Segment selector has been loaded into segment register or used by selector test instructions	

Code and data (including stack data) are stored in two types of segments: code segments and data segments. Both types are identified and defined by segment descriptors (S = 1). Code segments are identified by the executable (E) bit set to 1 in the descriptor access rights byte, whereas the data segments have the E bit set to 0.

System segment descriptors (S = 0, type = 1-3)

In addition to code and data segment descriptors, the protected mode SAB 80286 defines system segment descriptors. These descriptors define special system data segments which contain a table of descriptors (local descriptor table descriptor) or segments which contain the execution state of a task (task state segment descriptor).
The figure and table on next page show the formats for the special system data segment descriptors.

System Segment Descriptor



*) Must be set to 0 for compatibility with SAB 80386

System Segment Descriptor Fields

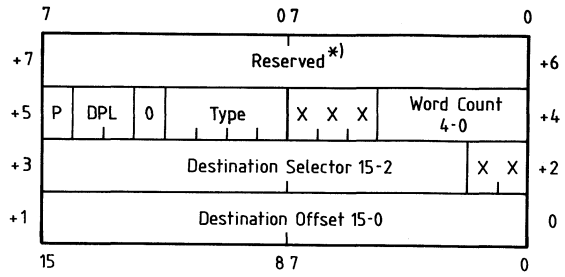
Name	Value	Description
TYPE	1 2 3	Available task state segment Local descriptor table descriptor Busy task state segment
P	0 1	Descriptor contents are not valid Descriptor contents are valid
DPL	0–3	Descriptor privilege level
BASE	24-bit number	Base address of special system data segment in real memory
LIMIT	16-bit number	Offset of last byte in segment

Gate descriptors (S = 0, Type = 4-7)

Gates are used to control access to entry points within the target code segment. The gate descriptors are **call** gates, **task** gates, **interrupt** gates and **trap** gates. Gates provide a level of indirection between the source and destination of the control transfer. This indirection allows the CPU to automatically perform protection checks and control entry point of the destination. Call gates are used to change privilege levels (see privilege), task gates are used to perform a task switch, and interrupt and trap gates are used to specify interrupt service routines. The interrupt gate disables interrupts (resets IF) while the trap gate does not.

The figure and table on the next page show the format of the gate descriptors. The descriptor contains a destination pointer that points to the descriptor of the target segment and the entry point offset. The destination selector in an interrupt gate, trap gate, and call gate must refer to a code segment descriptor. Exception 13 is generated when the gate is used if a destination selector does not refer to the correct descriptor type.

Gate Descriptor



*) Must be set to 0 for compatibility with SAB 80386 (X is don't care)

Gate Descriptor Fields

Name	Value	Description
TYPE	4 5 6 7	– Call gate – Task gate – Interrupt gate – Trap gate
P	0 1	– Descriptor contents are not valid – Descriptor contents are valid
DPL	0–3	Descriptor privilege level
WORD COUNT	0–31	Number of words to copy from callers stack to called procedures stack. Only used with call gate
DESTINATION SELECTOR	16-bit selector	Selector to the target code segment (call, interrupt or trap gate)
DESTINATION OFFSET	16-bit offset	Entry point within the target code segment

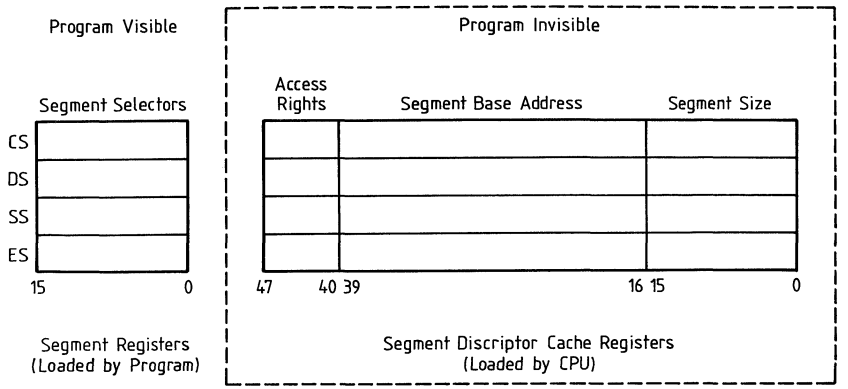
Segment descriptor cache registers

A segment descriptor cache register is assigned to each of the four segment registers (CS, SS, DS, ES). Segment descriptors are automatically loaded (cached) into a segment descriptor cache register (see figure) whenever the associated segment register is loaded with a selector. Only segment descriptors may be loaded into segment descriptor cache registers. Once loaded, all references to that segment of memory use the cached descriptor information instead of reaccessing memory. The descriptor cache registers are not visible to programs. No instructions exist to store their contents. They only change when a segment register is loaded.

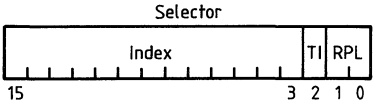
Selector fields

A protected mode selector has three fields: descriptor entry index, local or global descriptor table indicator (TI), and selector privilege (RPL) as shown in the figure on selector fields. These fields select one of two memory-based tables of descriptors, select the appropriate table entry and allow highspeed testing of the selector's privilege attribute (refer to privilege discussion below).

Descriptor Cache Registers



Selector Fields

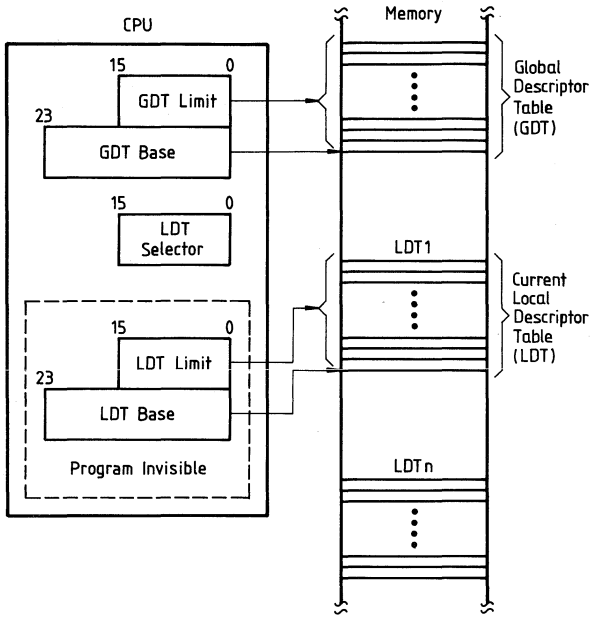


Bits	Name	Function
1-0	Requested Privilege Level (RPL)	Indicates Selector Privilege Level Desired
2	Table Indicator (TI)	TI = 0 Use Global Descriptor Table (GDT) TI = 1 Use Local Descriptor Table (LDT)
15-3	Index	Select Descriptor Entry in Table

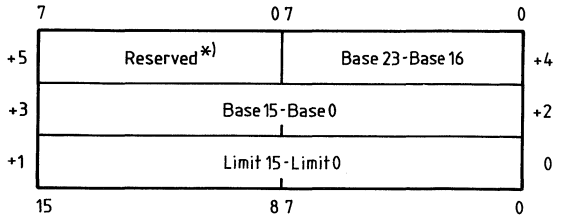
Local and global descriptor tables (LDT, GDT)

Two tables of descriptors, called descriptor tables, contain all descriptors accessible by a task at any given time. A descriptor table is a linear array of up to 8192 descriptors. The upper 13 bits of the selector value are an index into a descriptor table. Each table has a 24-bit base register to locate the descriptor table in physical memory and a 16-bit limit register that confine descriptor access to the defined limits of the table as shown in the figure below. A restartable exception (13) will occur if an attempt is made to reference a descriptor outside the table limits.

Local and Global Descriptor Table Definition



Global Descriptor Table and Interrupt Descriptor Table Data Type

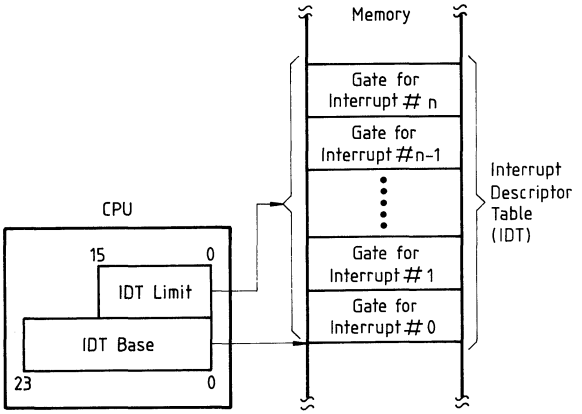


*) Must be set to 0 for compatibility with SAB 80386

Interrupt descriptor table

The protected mode SAB 80286 has a third descriptor table, called the interrupt descriptor table (DT) (see top figure on next page), used to define up to 256 interrupts. It may contain only task gates, interrupt gates and trap gates. The IDT (interrupt descriptor table) has a 24-bit base and 16-bit limit register in the CPU. References to IDT entries are made via INT instructions, external interrupt vectors, or exceptions. The IDT must be at least 256 bytes in size to allocate space for all reserved interrupts.

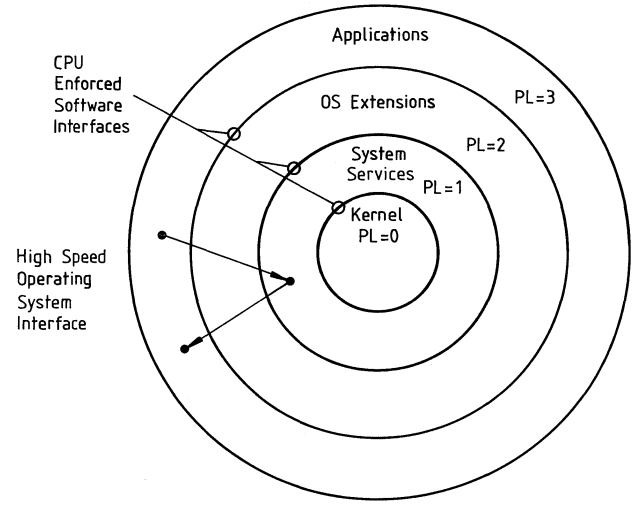
Interrupt Descriptor Table Definition



Privilege

The SAB 80286 has a four-level hierarchical privilege system which controls the use of privileged instructions and access to descriptors (and their associated segments) within a task (figure below). The privilege levels are numbered 0 through 3. Level 0 is the most privileged level.

Hierarchical Privilege Levels



Protection

The SAB 80286 includes mechanisms to protect critical instructions that affect the CPU execution state (e.g. HLT) and code or data segments from improper usage. These mechanisms are grouped under the term "protection" and have three forms:

Restricted usage of segments (e.g. no write allowed to read-only data segments). The only segments available for use are defined by descriptors in the local descriptor table (LDT) and global descriptor table (GDT).

Restricted access to segments via the rules of privilege and descriptor usage.

Privileged instructions or operations that may only be executed at certain privilege levels as determined by the CPL and I/O privilege level (IOPL). The IOPL is defined by bits 14 and 13 of the flag word.

These checks are performed for all instructions and can be split into three categories: segment load checks (table 9), operand reference checks (table 10), and privileged instruction checks (table 11). Any violation of the rules shown will result in an exception. A not-present exception related to the stack segment causes exception 12.

The IRET and POPF instructions do not perform some of their defined functions if CPL is not of sufficient privilege (numerically small enough). No exceptions or other indication are given when these conditions occur.

The IF bit is not changed if CPL > IOPL.
The IOPL field of the flag word is not changed if CPL > 0.

Table 9
Segment Register Load Checks

Error description	Exception number
Descriptor table limit exceeded	13
Segment descriptor not present	11 or 12
Privilege rules violated	13
Invalid descriptor/segment type segment register load: – read only data segment load to SS – special control descriptor load to DS, ES, SS – execute only segment load to DS, ES, SS – data segment load to CS – read/execute code segment load to SS	13

Table 10
Operand Reference Checks

Error description	Exception number
Write into code segment	13
Read from execute-only code segment	13
Write to read-only data segment	13
Segment limit exceeded [1]	12 or 13

[1] Carry out in offset calculations is ignored.

Table 11
Privileged Instruction Checks

Error description	Exception number
CPL > 0 when executing the following instructions LIDT, LLDT, LGDT, LTR, LMSW, CTS, HLT	13
CPL > IOPL when executing the following instructions INS, IN, OUTS, OUT, STI, CLI, LOCK	13

Exceptions

The SAB 80286 detects several types of exceptions and interrupts in protected mode (see table 12). Most of them are restartable after the exceptional condition is removed. Interrupt handlers for most exceptions receive an error code, pushed on the stack after the return address, that identifies the selector involved (0 if none). The return address normally points to the failing instruction, including all leading prefixes. For a processor extension segment overrun exception, the return address will not point at the ESC instruction that caused the exception; however, the processor extension registers may contain the address of the failing instruction.

Table 12
Protected Mode Exceptions

Interrupt vector	Function	Return address at failing instruction?	Always restart-able?	Error code on stack?
8	Double exception detected	yes	no	yes
9	Processor extension segment overrun	no	no	no
10	Invalid task state segment	yes	yes	yes
11	Segment not present	yes	yes	yes
12	Stack segment overrun or segment not present	yes	yes[1)]	yes
13	General protection	yes	no	yes

[1)] When a PUSHA instruction attempts to wrap around the stack segment, the machine state after the exception will not be restartable. This condition is identified by the value of the saved SP being either 0000(H), 0001(H), FFFE(H), or FFFF(H).

Special Operations

Task switch operation

The SAB 80286 provides a built-in task switch operation which saves the entire SAB 80286 execution state (registers, address space, and a link to the previous task), loads a new execution state, and commences execution in the new task. Like gates, the task switch operation is invoked by executing an inter-segment JMP or CALL instruction which refers to a task state segment (TSS) or task gate descriptor in the GDT or LDT. An INT instruction, exception, or external interrupt may also invoke the task switch operation by selecting a task gate descriptor in the associated IDT descriptor entry.

The TSS descriptor points at a segment (see figure on next page) containing the entire SAB 80286 execution state while a task gate descriptor contains a TSS selector. The limit field must be $> 002B(H)$.

The task state segment is marked busy by changing the descriptor type field from type 1 to type 3. Use of a selector that references a busy task state segment causes exception 13.

Processor extension context switching

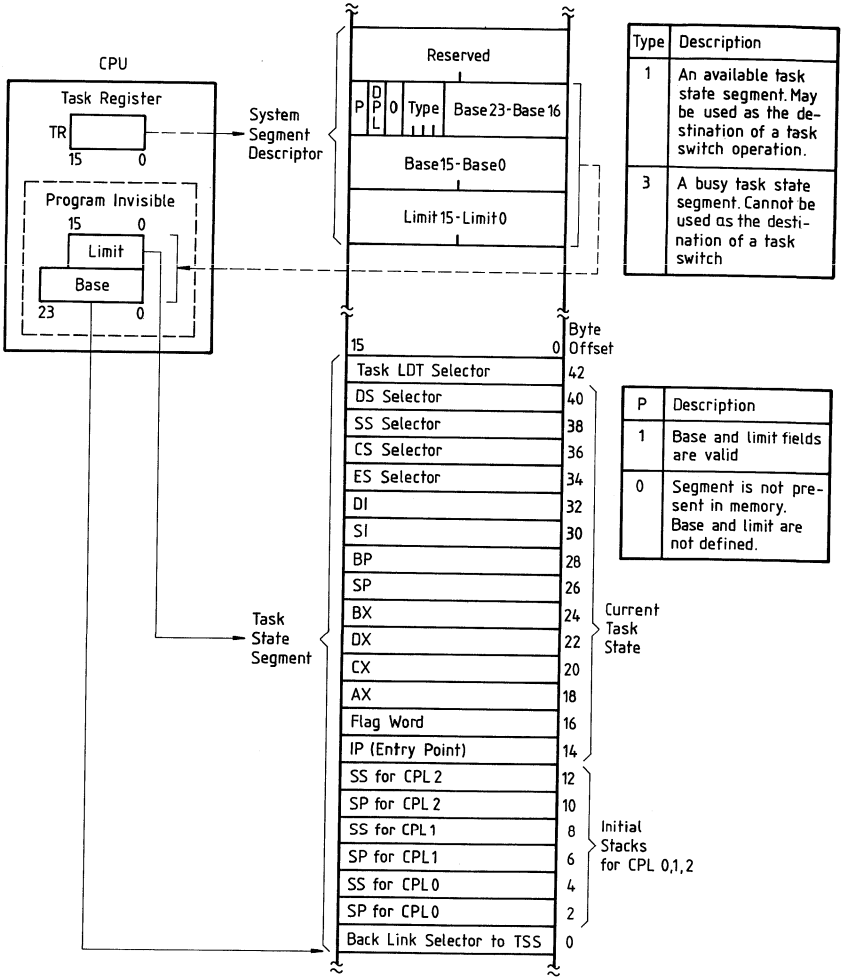
The context of a processor extension (such as the SAB 80287 numerics processor) is not changed by the task switch operation. A processor extension context need only be changed when a different task attempts to use the processor extension (which still contains the context of a previous task).

Whenever the SAB 80286 switches tasks, it sets the task switched (TS) bit of the MSW. TS indicates that a processor extension context may belong to a different task than the current one. The processor extension not present exception (7) will occur when attempting to execute an ESC or WAIT instruction if TS = 1 and a processor extension is present (MP = 1 in MSW).

Double fault and shutdown

If two seperate exceptions are detected during a single instruction execution, the SAB 80286 performs the double fault exception (8). If an exception occurs during processing of the double fault exception, the SAB 80286 will enter shutdown. During shutdown no further instructions or exceptions are processed. Either NMI (CPU remains in protected mode) or RESET (CPU exits protected mode) can force the SAB 80286 out of shutdown. Shutdown is externally signalled via a HALT bus operation with A1 low.

Task State Segment and TSS Registers



System Interface

The SAB 80286 system interface appears in two forms: a local bus and a system bus. The local bus consists of address, data, status, and control signals at the pins of the CPU. A system bus is any buffered version of the local bus. A system bus may also differ from the local bus in terms of coding of status and control lines and/or timing and loading of signals. The SAB 80286 family includes several devices to generate standard system buses such as the IEEE 796 standard Multibus® and the IEEE 796 AMS-M Bus.

Bus Interface Signals and Timing

The SAB 80286 local bus interfaces the SAB 80286 to local memory and I/O components. The interface has 24 address lines, 16 data lines, and 8 status and control signals.

The SAB 80286 CPU, SAB 82284 clock generator, SAB 82288 bus controller, SAB 82289 bus arbiter, SAB 8286A/8287A transceivers, and SAB 8282A/8283A latches provide a buffered and decoded system bus interface. The SAB 82284 generates the system clock and synchronizes $\overline{\text{READY}}$ and RESET. The SAB 82288 converts bus operation status encoded by the SAB 80286 into command and bus control signals.

The SAB 82289 bus arbiter generates Multibus bus arbitration signals. These components can provide the timing and electrical power drive levels required for most system bus interfaces including the Multibus.

Physical Memory and I/O Interface

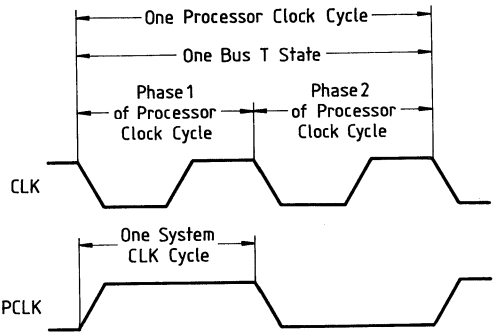
A maximum of 16 megabytes of physical memory can be addressed in protected mode. One megabyte can be addressed in real address mode. Memory is accessible as bytes or words. Words consist of any two consecutive bytes addressed with the least significant byte stored in the lowest address.

The I/O address space contains 64 K addresses in both modes. The I/O space is accessible as either bytes or words, as is memory. Byte-wide peripheral devices may be attached to either the upper or lower byte of the data bus. An interrupt controller such as the SAB 8259A must be connected to the lower byte of the data bus (D7-D0) for proper return of the interrupt vector.

Bus Operation

The SAB 80286 uses a double frequency system clock (CLK input) to control bus timing. All signals on the local bus are measured relative to the system CLK input. The CPU divides the system clock by 2 to produce the internal processor clock, which determines bus state. Each processor clock is composed of two system clock cycles named phase 1 and phase 2. The SAB 82284 clock generator output (PCLK) identifies the next phase of the processor clock (see figure on system and processor clock relationship).

System and Processor Clock Relationships



Six types of bus operations are supported: memory read, memory write, I/O read, I/O write, interrupt acknowledge, and halt/shutdown. Data can be transferred at a maximum rate of one word per two processor clock cycles.

The SAB 80286 bus has three basic states: idle (TI), send status (TS), and perform command (TC). The SAB 80286 CPU also has a fourth local bus state called hold (TH). TH indicates that the SAB 80286 has surrendered control of the local bus to another bus master in response to a HOLD request.

Each bus state is one processor clock long. The figure below shows the four SAB 80286 local bus states and allowed transitions.

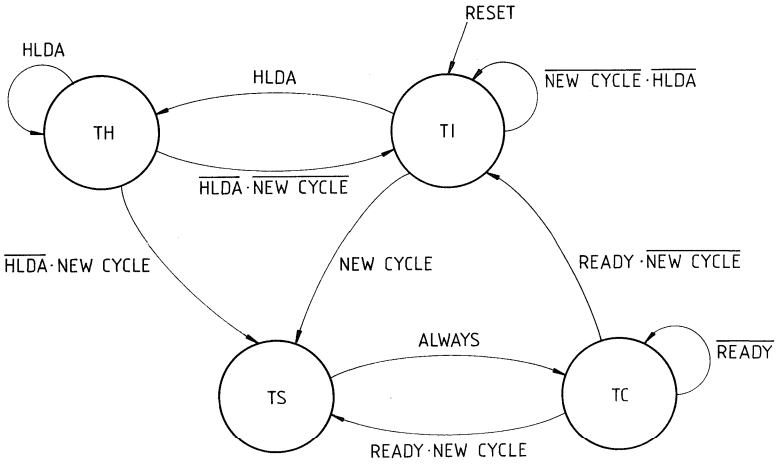
Pipelined Addressing

The SAB 80286 uses a local bus interface with pipelined timing to allow as much time as possible for data access. Pipelined timing allows bus operations to be performed in two processor cycles, while allowing each individual bus operation to last for three processor cycles.

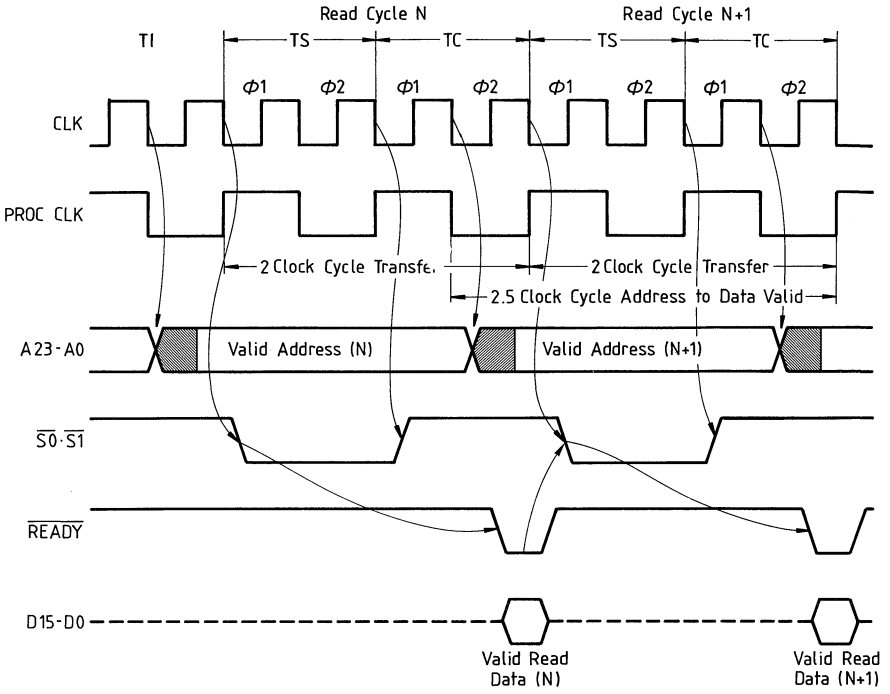
The timing of the address outputs is pipelined such that the address of the next bus operation becomes available during the current bus operation. Or in other words, the first clock of the next bus operation is overlapped with the last clock of the current bus operation. Therefore, address decoder and routing logic can operate in advance of the next bus operation. External address latches may hold the address stable for the entire bus operation, and provide additional ac and dc buffering.

The SAB 80286 does not maintain the address of the current bus operation during all TC states. Instead, the address for the next bus operation may be emitted during phase 2 of any TC. The address remains valid during phase 1 of the first TC to guarantee hold time, relative to ALE, for the address latch inputs.

SAB 80286 Bus States



Basic Bus Cycle



Bus Cycle Termination

At maximum transfer rates, the SAB 80286 bus alternates between the status and command states. The bus status signals become inactive after TS so that they may correctly signal the start of the next bus operation after the completion of the current cycle. No external indication of TC exists on the SAB 80286 local bus. The bus master and bus controller enter TC directly after TS, and continue executing TC cycles until terminated by $\overline{\text{READY}}$.

$\overline{\text{READY}}$ Operation

The current bus master and SAB 82288 bus controller terminate each bus operation simultaneously to achieve maximum bus bandwidth. Both are informed in advance by $\overline{\text{READY}}$ active which identifies the last TC cycle of the current bus operation. The bus master and bus controller must see the same sense of the $\overline{\text{READY}}$ signal, there by requiring $\overline{\text{READY}}$ be synchronous to the system clock.

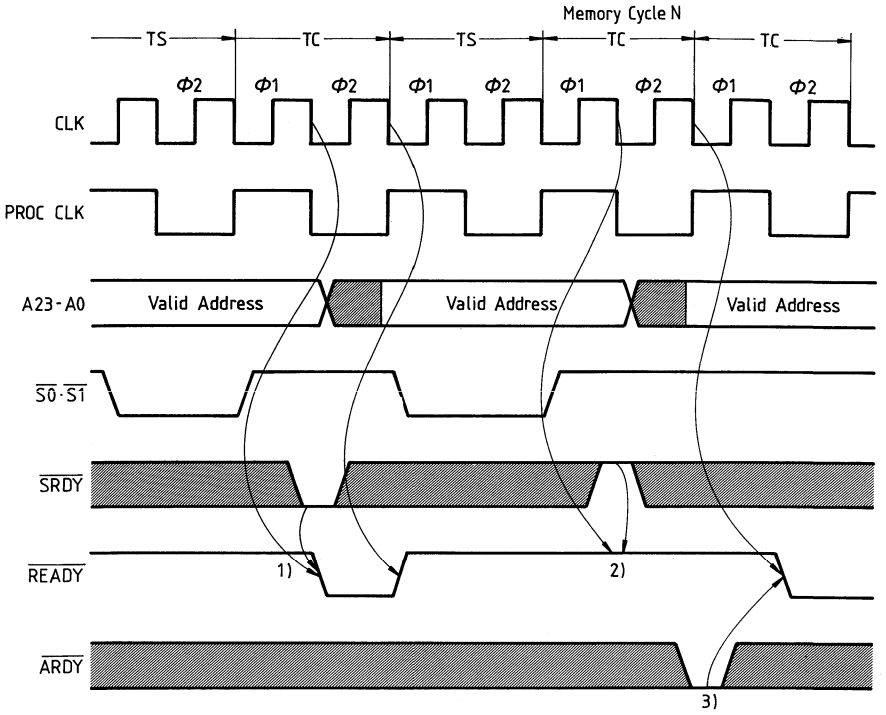
Synchronous Ready

The SAB 82284 clock generator provides $\overline{\text{READY}}$ synchronization from both synchronous and asynchronous sources (see figure on next page). The synchronous ready input ($\overline{\text{SRDY}}$) of the clock generator is sampled with the falling edge of CLK at the end of phase 1 of each TC. The state of $\overline{\text{SRDY}}$ is then transferred to the bus master and bus controller via the $\overline{\text{READY}}$ output line.

Asynchronous Ready

Many systems have devices of subsystems that are asynchronous to the system clock. As a result, their ready outputs cannot be guaranteed to meet the SAB 82284 $\overline{\text{SRDY}}$ setup and hold time requirements. But the SAB 82284 asynchronous ready input ($\overline{\text{ARDY}}$) is designed to accept such signals. The $\overline{\text{ARDY}}$ input is sampled at the beginning of each TC cycle by SAB 82284 synchronization logic. This provides one system CLK cycle time to resolve its value before transferring it to the bus master and bus controller.

Synchronous and Asynchronous Ready



1) $\overline{\text{SRDYEN}}$ is active low
2) If $\overline{\text{SRDYEN}}$ is high, the state of $\overline{\text{SRDY}}$ will not effect $\overline{\text{READY}}$
3) $\overline{\text{ARDYEN}}$ is active low

$\overline{\text{ARDY}}$ or $\overline{\text{ARDYEN}}$ must be high at the end of TS. $\overline{\text{ARDY}}$ cannot be used to terminate a bus cycle with no wait states.

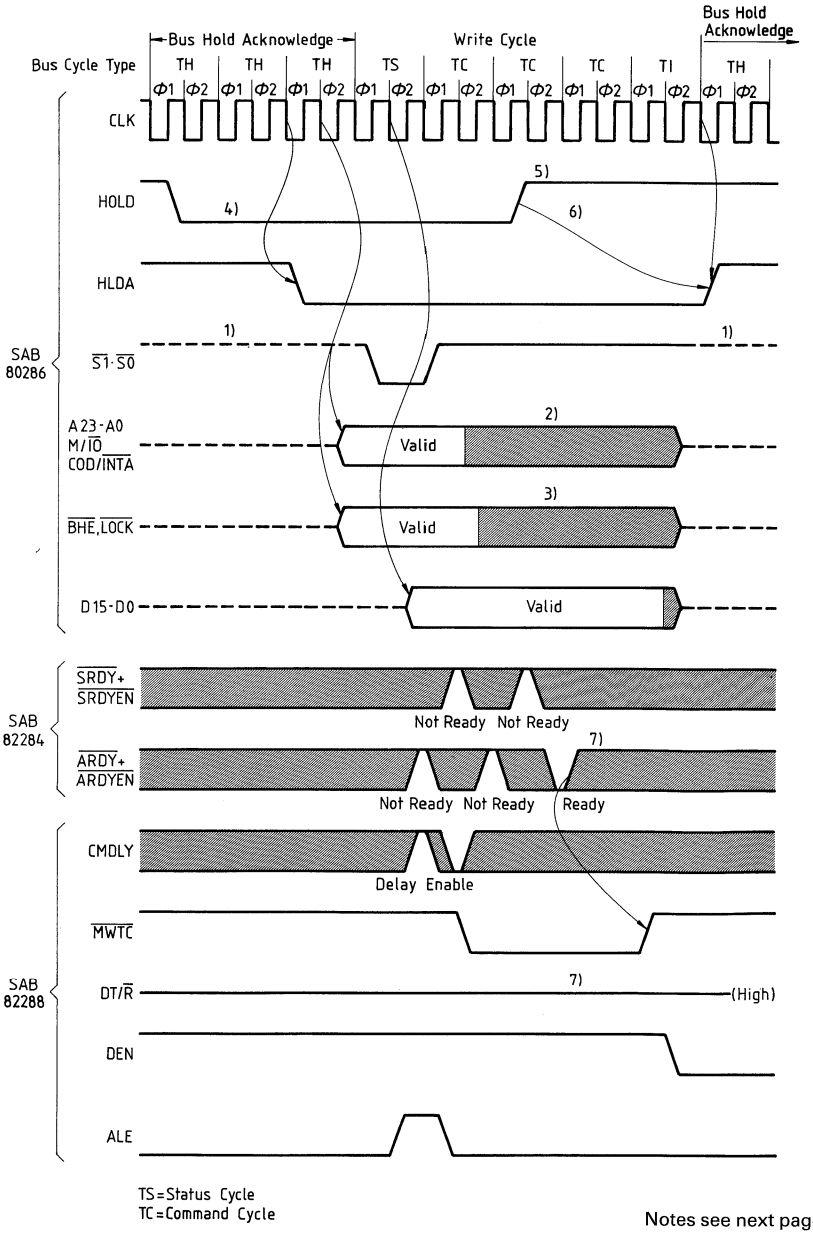
Each ready input of the SAB 82284 has an enable pin ($\overline{\text{SRDYEN}}$ and $\overline{\text{ARDYEN}}$) to select whether the current bus operation will be terminated by the synchronous or asynchronous ready. Either of the ready inputs may terminate a bus operation. These enable inputs are active low and have the same timing as their respective ready inputs. An address decode logic usually selects whether the current bus operation should be terminated by $\overline{\text{ARDY}}$ or $\overline{\text{SRDY}}$.

HOLD and HLDA

HOLD and HLDA allow another bus master to gain control of the local bus by placing the SAB 80286 bus into the TH state. The sequence of events required to pass control between the SAB 80286 and another local bus master is shown in the next figure.

HOLD must not be active during the time from the leading edge of RESET until 34 CLKs following the trailing edge of RESET unless the SAB 80286 is in the Halt condition. To insure that the SAB 80286 remains in the Halt condition until the processor Reset operation is complete, no interrupts should occur after the execution of HLT until 34 CLKs after the trailing edge of the RESET pulse.

Multibus Write Terminated by Asynchronous Ready with Bus Hold



Notes see next page.

Notes:

1) Status lines are not driven by SAB 80286 yet remain high due to pullup resistors in SAB 80288 and SAB 82289 during HOLD state.
2) Address, M/$\overline{IO}$ and COD/$\overline{INTA}$ may start floating during any TC depending on when internal SAB 80286 bus arbiter decides to release bus to external HOLD. The float starts in ϕ 2 of TC.
3) $\overline{BHE}$ and $\overline{LOCK}$ may start floating after the end of any TC depending on when internal SAB 80286 bus arbiter decides to release bus to external HOLD. The float starts in ϕ 1 of TC.
4) The minimum HOLD to HLDA time is shown. Maximum is one TH longer.
5) The earliest HOLD time is shown. It will always allow a subsequent memory cycle if pending as shown.
6) The minimum HOLD in HLDA time is shown. Maximum is a function of the instruction, type of bus cycle and other machine status (i.e., interrupts, waits, lock, etc.)
7) Asynchronous ready allows termination of the cycle. Synchronous ready does not signal ready in this example. Synchronous ready state in ignored after ready is signalled via the asynchronous input.

Processor Extension Transfers

The processor extension interface uses I/O port addresses 00F8(H), 00FA(H), and 00FC(H) which are part of the I/O port address range reserved. An ESC instruction with EM = 0 and TS = 0 will perform I/O bus operations to one or more of these I/O port addresses independent of the value of IOPL and CPL.

ESC instructions with memory references enable the CPU to accept PEREQ inputs for processor extension operand transfers. The CPU will determine the operand starting address and read/write status of the instruction. For each operand transfer, two or three bus operations are performed, one word transfer with I/O port address 00FA(H) and one or two bus operations with memory. Three bus operations are required for each word operand aligned on an odd byte address.

Interrupt Acknowledge Sequence

The figure Interrupt Acknowledge Sequence illustrates a sequence performed by the SAB 80286 in response to an INTR input. An interrupt acknowledge sequence consists of two INTA bus operations. The first allows a master SAB 8259A programmable interrupt controller (PIC) to determine which if any of its slaves should return the interrupt vector. An eight-bit vector is read by the SAB 80286 during the second INTA bus operation to select an interrupt handler routine from the interrupt table.

The master cascade enable (MCE) signal of the SAB 82288 is used to enable the cascade address drivers, during INTA bus operations (see interrupt acknowledge sequence figure), onto the local address bus for distribution to slave interrupt controllers via the system address bus. The SAB 80286 emits the $\overline{LOCK}$ signal (active low) during TS of both INTA bus operations. A local bus "hold" request will not be honored until the end of the second INTA bus operation.

Three idle processor clocks are provided by the SAB 80286 between INTA bus operations to allow for the minimum INTA to INTA time and CAS (cascade address) out delay of the SAB 8259A. The second INTA bus operation must always have at least one extra TC state added via logic controlling $\overline{READY}$. A23–A0 are in tristate off until the first TC state of the second INTA bus operation. This prevents bus contention between the cascade address drivers and CPU address drivers. The extra TC state provides time for the SAB 80286 to resume driving the address lines for subsequent bus operations.

Local Bus Usage Priorities

The SAB 80286 local bus is shared among several internal units and external HOLD requests. In case of simultaneous requests, their relative priorities are:

(Highest)
Any transfers which assert $\overline{LOCK}$ either explicitly (via the LOCK instruction prefix) or implicitly (i.e. segment descriptor access, interrupt acknowledge sequence, or an XCHG with memory).

The second of the two byte bus operations required for an odd-aligned word operand.

The second or third cycle of a processor extension data transfer.

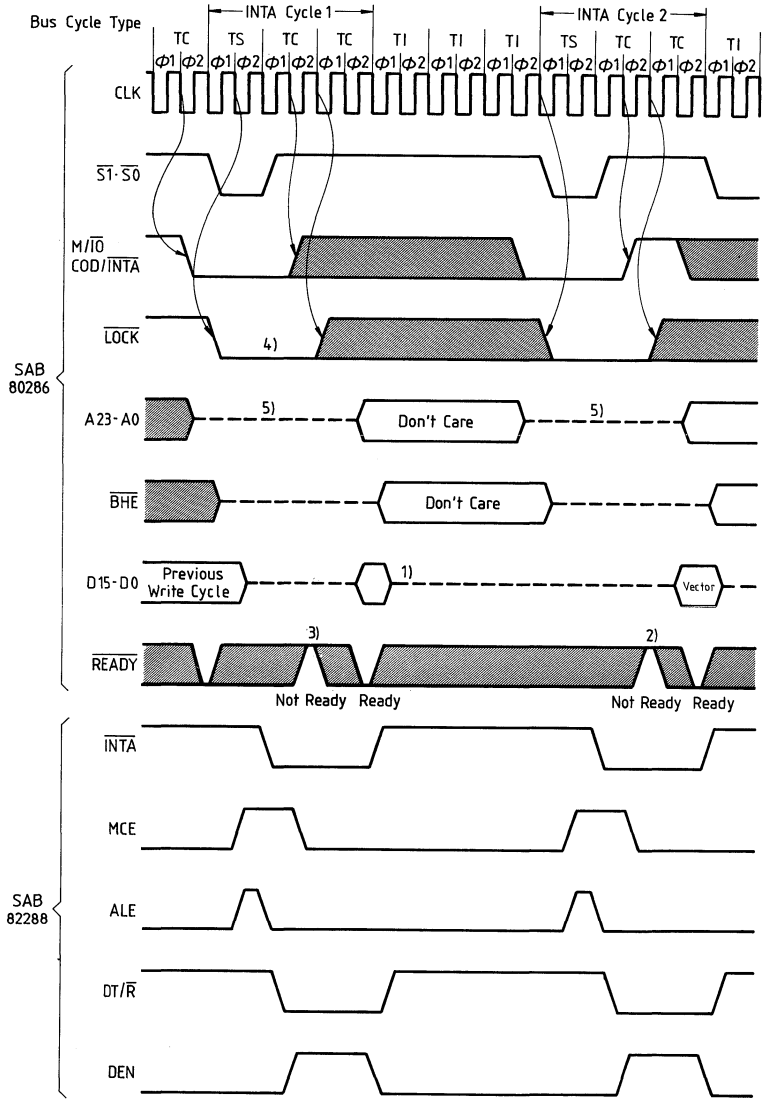
Local bus request via HOLD input.

Processor extension data operand transfer via PEREQ input.

Data transfer performed by EU as part of an instruction.

(Lowest)
An instruction prefetch request from BU. The EU wil inhibit prefetching two processor clocks in advance of any data transfer to minimize waiting by EU for a prefetch to finish.

Interrupt Acknowledge Sequence



Halt or Shutdown Cycles

The SAB 80286 externally indicates halt or shutdown conditions as a bus operation. These conditions occur due to an HLT instruction or multiple protection exceptions while attempting to execute one instruction. A halt or shutdown bus operation is signalled when $\overline{S1}$, $\overline{S0}$ and COD/$\overline{INTA}$ are low and M/$\overline{IO}$ is high. A1 high indicates halt, and A1 low indicates shutdown. The SAB 82288 bus controller does not issue ALE, nor is $\overline{READY}$ required to terminate a halt or shutdown bus operation.

During halt or shutdown, the SAB 80286 may service PEREQ or HOLD requests. A processor extension segment overrun exception during shutdown will inhibit further service of PEREQ. Either NMI or RESET will force the SAB 80286 out of halt or shutdown. An INTR, if interrupts are enabled, or a processor extension segment overrun exception will also force the SAB 80286 out of halt.

1) Data is ignored.
2) First INTA cycles should have at least one wait state inserted to meet SAB 8259A minimum INTA pulse width.
3) Second INTA cycle must have at least one wait state inserted since the CPU will not drive A23–A0. $\overline{BHE}$, and $\overline{LOCK}$ until after the first TC state.
   The CPU-imposed one clock delay prevents bus contention between cascade address buffer being disabled by MCE↓ and address outputs. Without the wait state, the SAB 80286 address will not be valid for a memory cycle started immediately after the second INTA cycle.
   The SAB 8259A also requires one wait state for minimum INTA pulse width.
4) $\overline{LOCK}$ is activated during the INTA cycles to prevent the SAB 82289 from releasing the bus between INTA cycles in a multimaster system.
5) A23–A0 exit Tri-state OFF during ∅2 of the second TC in the INTA cycle.

System Configuration

The versatile bus structure of the SAB 80286 microsystem, with a full complement of support chips, allows flexible configuration of a wide range of systems. The basic configuration shown below is similar to an SAB 8086 maximum mode system. It includes the CPU plus an SAB 8259A interrupt controller, SAB 82284 clock generator and the SAB 82288 bus controller. The latches (SAB 8282A and SAB 8283A) and transceivers (SAB 8286A and SAB 8287A) used in an SAB 8086 system may be used in a SAB 80286 microsystem.

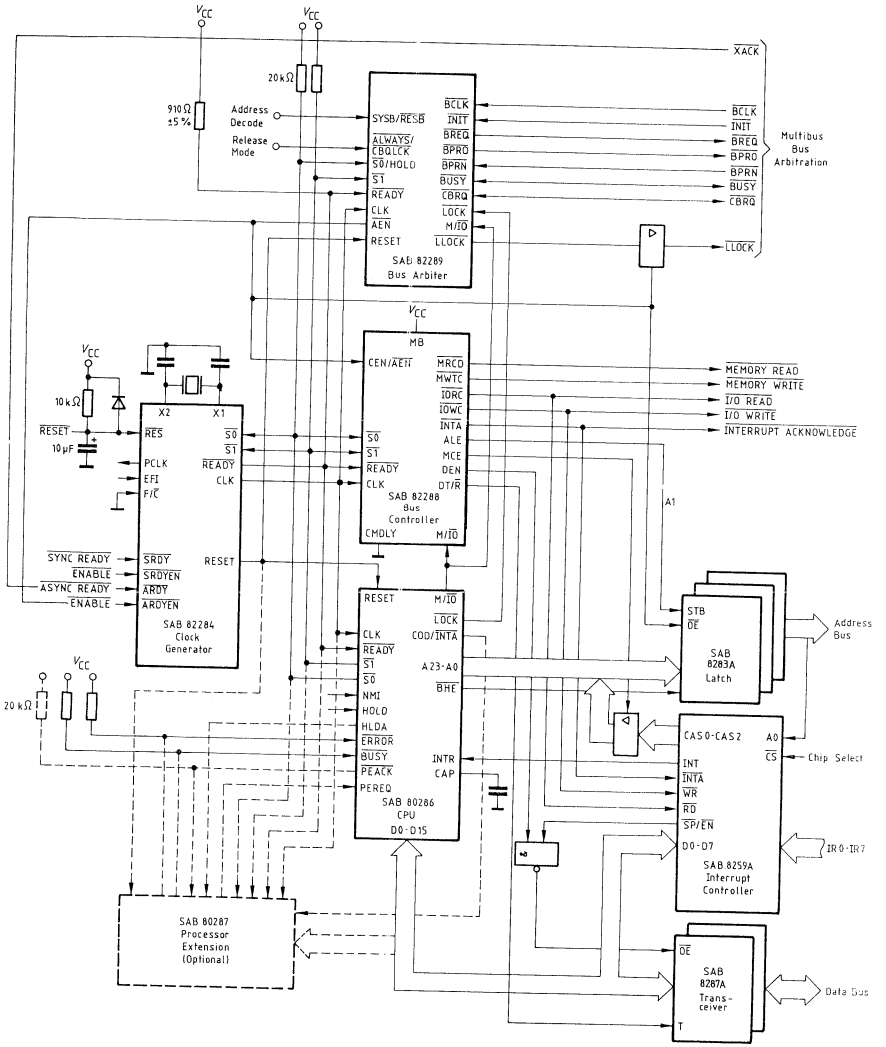
As indicated by the dashed lines in the figure above, the ability to add processor extensions is an integral feature of SAB 80286 microsystems. The processor extension interface allows external hardware to perform special functions and transfer data concurrently with CPU execution of other instructions. Full system integrity is maintained because the SAB 80826 supervises all data transfers and instruction execution for the processor extension.

The SAB 80287 numeric processor extension (NPX), for example, uses this interface. The SAB 80287 has all the instructions and data types of an SAB 8087. The SAB 80287 NPX can perform numeric calculations and data transfers concurrently with CPU program execution. Numerics code and data have the same integrity as all other information protected by the SAB 80286 protection mechanism.

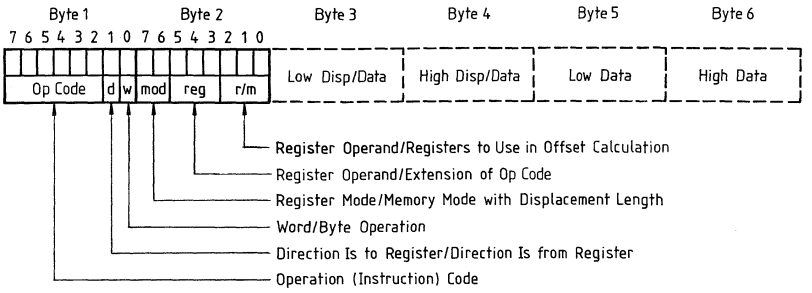
The SAB 80286 can overlap chip select decoding and address propagation during the data transfer for the previous bus operation. This information is latched into the SAB 8282A/8283A's by ALE in the middle of a TS cycle. The latched chip select and address information remains stable during the bus operation while the next cycles address is being decoded and propagated into the system. Decode logic can be implemented with a high-speed bipolar PROM.

The optional decode logic shown in the figure on basic system configuration takes advantage of the overlap between address and data of the SAB 80286 bus cycle to generate advance memory and IO-select signals. This minimizes system performance degradation caused by address propagation and decode delays. In addition to selection of memory and I/O, the advance selects may be used with configurations supporting local and system buses to enable the appropriate bus interface for each bus cycle. The COD/$\overline{INTA}$ and M/$\overline{IO}$ signals are applied to the decode logic to distinguish between interrupt, I/O, code, and data bus cycles. By adding the SAB 82289 bus arbiter chip, the SAB 80286 provides a Multibus system bus interface. A second SAB 82288 bus controller and additional latches and transceivers could be added to the local bus. This configuration allows the SAB 80286 to support an on-board bus for local memory and peripherals, and the Multibus for system bus interfacing.

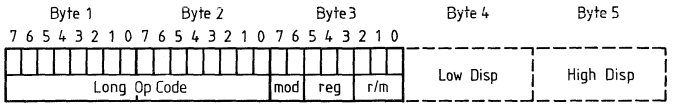
Basic SAB 80286 System Configuration



Instruction Format Examples



A. Short Op Code Format Example



B. Long Op Code Format Example

SAB 80286 Instruction Set Summary

Instruction Timing Notes

The instruction clock counts listed below establish the maximum execution rate of the SAB 80286. With no delays in bus cycles, the actual clock count of an SAB 80286 program will average 5% more than the calculated clock count, due to instruction sequences which execute faster than they can be fetched from memory.

To calculate elapsed times for instruction sequences multiply the sum of all instruction clock counts, as listed in the table below, by the processor clock period. An 8 MHz processor clock has a clock period of 125 nanoseconds and requires an SAB 80286 system clock (CLK input) of 16 MHz.

Instruction Clock Count Assumptions

1. The instruction has been prefetched, decoded, and is ready for execution. Control transfer instruction clock counts include all time required to fetch, decode, and prepare the next instruction for execution.
2. Bus cycles do not require wait states.
3. There are no processor extension data transfer or local bus HOLD requests.
4. No exceptions occur during instruction execution.

Instruction Set Summary Notes

Addressing displacements selected by the MOD field are not shown. If necessary they appear after the instruction fields shown.

Above/below refers to unsigned value

Greater refers to positive signed value

Less refers to less positive (more negative) signed values

if d = 1 then to register; if d = 0 then from register

if w = 1 then word instruction; if w = 0 then byte instruction

if s = 0 then 16-bit immediate data form the operand

if s = 1 then an immediate data byte is sign-extended to form the 16-bit operand

x don't care

Z used for string primitives for comparison with ZF FLAG

If two clock counts are given, the smaller refers to a register operand and the larger refers to a memory operand

* = add one clock if offset calculation requires summing 3 elements

n = number of times repeated

m = number of bytes of code in next instruction

Level(L) – Lexical nesting level of the procedure

The following comments describe possible exceptions, side effects, and allowed usage for instructions in both operating modes of the SAB 80286.

Real address mode only

1. This is a protected mode instruction. Attempted execution in real address mode will result in an undefined opcode exception (6).
2. A segment overrun exception (13) will occur if a word operand reference at offset FFFF(H) is attempted.
3. This instruction may be executed in real address mode to initialize the CPU for protected mode.
4. The IOPL and NT fields will remain 0.
5. Processor extension segment overrun interrupt (9) will occur if the operand exceeds the segment limit.

Either mode

6. An exception may occur, depending on the value of the operand.
7. $\overline{\text{LOCK}}$ is automatically asserted regardless of the presence or absence of the LOCK instruction prefix.
8. $\overline{\text{LOCK}}$ does not remain active between all operand transfers.

Protected virtual address mode only

9. A general protection exception (13) will occur if the memory operand can not be used due to either a segment limit or access rights violation. If a stack segment limit is violated, a stack segment overrun exception (12) occurs.
10. For segment load operations, the CPL, RPL and DPL must agree with privilege rules to avoid an exception. The segment must be present to avoid a not-present exception (11). If the SS register is the destination and a segment not-present violation occurs, a stack exception (12) occurs.
11. All segment descriptor accesses in the GDT or LDT made by this instruction will automatically assert $\overline{\text{LOCK}}$ to maintain descriptor integrity in multiprocessor systems.
12. JMP, CALL, INT, RET, IRET instructions referring to another code segment will cause a general protection exception (13) if any privilege rule is violated.
13. A general protection exception (13) occurs if CPL $\neq 0$.
14. A general protection exception (13) occurs if CPL>IOPL.
15. The IF field of the flag word is not updated if CPL>IOPL. The IOPL field is updated only if CPL = 0.
16. Any violation of privilege rules as applied to the selector operand does not cause a protection exception; rather, the instruction does not return a result and the zero flag is cleared.
17. If the starting address of the memory operand violates a segment limit, or an invalid access is attempted, a general protection exception (13) will occur before the ESC instruction is executed. A stack segment overrun exception (12) will occur if the stack limit is violated by the operand's starting address. If a segment limit is violated during an attempted data transfer then a processor extension segment overrun exception (9) occurs.
18. The destination of an INT, JMP, CALL, RET or IRET instruction must be in the defined limit of a code segment or a general protection exception (13) will occur.

Instruction Set Summary

Function	Format	Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Data Transfer					
MOV = Move:					
Register to register/memory	1000100w mod reg r/m	2, 3 *	2, 3 *	2	9
Register/memory to register	1000101w mod reg r/m	2, 5 *	2, 5 *	2	9
Immediate to register/memory	1100011w mod 000 r/m data data if w = 1	2, 3 *	2, 3 *	2	9
Immediate to register	1011w reg data data if w = 1	2	2		
Memory to accumulator	1010000w addr-low addr-high	5	5	2	9
Accumulator to memory	1010001w addr-low addr-high	3	3	2	9
Register/memory to segment register	10001110 mod 0 reg r/m	2, 5 *	17, 19 *	2	9, 10, 11
Segment register to register/memory	10001100 mod 0 reg r/m	2, 3 *	2, 3 *	2	9
PUSH = Push:					
Memory	11111111 mod 110 r/m	5 *	5 *	2	9
Register	01010 reg	3	3	2	9
Segment register	000 reg 110	3	3	2	9
Immediate	011010s0 data data if s = 0	3	3	2	9
PUSHA = Push All	01100000	17	17	2	9
POP = Pop:					
Memory	10001111 mod 000 r/m	5 *	5 *	2	9
Register	01011 reg	5	5	2	9
Segment register	000 reg 111 (reg ≠ 01)	5	20	2	9, 10, 11

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format			Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Data Transfer (cont'd):							
POPA = Pop All	01100001			19	19	2	9
XCHG = **Exchange:**							
Register/memory with register	1000011w	mod reg r/m		3, 5 *	3, 5 *	2, 7	7, 9
Register with accumulator	10010 reg			3	3		
IN = **Input from:**							
Fixed port	1110010w	port		5	5		14
Variable port	1110110w			5	5		14
OUT = **Output to:**							
Fixed port	1110011w	port		3	3		14
Variable port	1110111w			3	3		14
XLAT = Translate byte to AL	11010111			5	5		9
LEA =Load EA to register	10001101	mod reg r/m		3 *	3 *		
LDS = Load pointer to DS	11000101	mod reg r/m	(mod ≠ 11)	7 *	21 *	2	9, 10, 11
LES = Load pointer to ES	11000100	mod reg r/m	(mod ≠ 11)	7 *	21 *	2	9, 10, 11
LAHF = Load AH with flags	10011111			2	2		
SAHF = Store AH into flags	10011110			2	2		
PUSHF = Push flags	10011100			3	3	2	9
POPF = Pop flags	10011101			5	5	2, 4	2, 4

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Arithmetic					
ADD = Add:					
Reg/memory with register to either	0 0 0 0 0 d w | mod reg. r/m	2, 7 *	2, 7*	2	9
Immediate to register memory	1 0 0 0 0 0 s w | mod 0 0 0 r/m | data | data if s w = 01	3, 7 *	3, 7 *	2	9
Immediate to accumulator	0 0 0 0 0 1 0 w | data | data if w = 1	3	3		
ADC = Add with carry:					
Reg memory with register to either	0 0 0 1 0 0 d w | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate to register/memory	1 0 0 0 0 0 s w | mod 0 1 0 r/m | data | data if s w = 01	3, 7 *	3, 7 *	2	9
Immediate to accumulator	0 0 0 1 0 1 0 w | data | data if w = 1	3	3		
INC = Increment					
Register memory	1 1 1 1 1 1 1 w | mod 0 0 0 r/m	2, 7 *	2, 7 *	2	9
Register	0 1 0 0 0 reg	2	2		
SUB = Subtract					
Reg memory and register to either	0 0 1 0 1 0 d w | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate from register memory	1 0 0 0 0 0 s w | mod 1 0 1 r/m | data | data if s w = 01	3, 7 *	3, 7 *	2	9
Immediate from accumulator	0 0 1 0 1 1 0 w | data | data if w = 1	3	3		
SSB = Subtract with borrow:					
Reg/memory and register to either	0 0 0 1 1 0 d w | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate from register/memory	1 0 0 0 0 0 s w | mod 0 1 1 r/m | data | data if s w = 01	3, 7 *	3, 7 *	2	9
Immediate from accumulator	0 0 0 1 1 1 0 w | data | data if w = 1	3	3		

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Arithmetic (cont'd):					
DEC = **Decrement:**					
Register memory	1 1 1 1 1 1 1 w | mod 0 0 1 r/m	2, 7 *	2, 7 *	2	9
Register	0 1 0 0 1 reg	2	2		
CMP = **Compare:**					
Register memory with register	0 0 1 1 1 0 1 w | mod reg r/m	2, 6 *	2, 6 *	2	9
Register with register/memory	0 0 1 1 1 0 0 w | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate with register memory	1 0 0 0 0 0 s w | mod 1 1 1 r/m | data | data if s w=01	3, 6 *	3, 6 *	2	9
Immediate with accumulator	0 0 1 1 1 1 w | data | data if w = 1	3	3		
NEG = Change sign	1 1 1 1 0 1 1 w | mod 0 1 1 r/m	2	7 *	2	7
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1	3	3		
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1	3	3		
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1	3	3		
DAS = Decimal adjust for substract	0 0 1 0 1 1 1 1	3	3		
MUL = Multiply (unsigned):	1 1 1 1 0 1 1 w | mod 1 0 0 r/m				
register-byte		13	13		
register-word		21	21		
memory-byte		16 *	16 *	2	9
menory-word		24 *	24 *	2	9
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w | mod 1 0 1 r/m				
register-byte		13	13		
register-word		21	21		
memory-byte		16 *	16 *	2	9
memory-word		24 *	24 *	2	9

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Arithmetic (cont'd):					
IMUL = Integer immediate multiply (signed)	0 1 1 0 1 0 s 1 | mod reg r/m | data | data if s = 0	21, 24 *	21, 24 *	2	9
DIV = Divide unsigned):	1 1 1 1 0 1 1 w | mod 1 1 0 r/m				
register-byte		14	14	6	6
register-word		22	22	6	6
memory-byte		17 *	17 *	2, 6	6, 9
memory-word		25 *	25 *	2, 6	6, 9
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w | mod 1 1 1 r/m				
register-byte		17	17	6	6
register-word		25	25	6	6
memory-byte		20 *	20 *	2, 6	6, 9
memory-word		28 *	28 *	2, 6	6, 9
AMM = ASCII adjust for multiply	1 1 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0	16	16		
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1 | 0 0 0 0 1 0 1 0	14	14		
CBW = Convert byte to word	1 0 0 1 1 0 0 0	2	2		
CWD = Convert word to double word	1 0 0 1 1 0 0 1	2	2		
Logic					
Shift/rotate instructions:					
Register/memory by 1	1 1 0 1 0 0 0 w | mod TTT r/m	2, 7 *	2, 7 *	2	9
Register/memory by CL	1 1 0 1 0 0 1 w | mod TTT r/m	5+n, 8+n*	5+n, 8+n*	2	9
Register/memory by count	1 1 0 0 0 0 0 w | mod TTT r/m | count	5+n, 8+n*	5+n, 8+n*	2	9

TTT	Instruction
0 0 0	ROL
0 0 1	ROR
0 1 0	RCL
0 1 1	RCR
1 0 0	SHL/SAL
1 0 1	SHR
1 1 1	SAR

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Logic (cont'd):					
AND = **And:**					
Reg/memory and register to either	0 0 1 0 0 0 d w | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 1 0 0 r/m | data | data if w = 1	3, 7 *	3, 7 *	2	9
Immediate to accumulator	0 0 1 0 0 1 0 w | data | data f w = 1	3	3		
TEST = **And function to flags, no result:**					
Register/memory and register	1 0 0 0 0 1 0 w | mod reg r/m	2, 6 *	2, 6 *	2	9
Immediate data and register/memory	1 1 1 1 0 1 1 w | mod 0 0 0 r/m | data | data if w = 1	3, 6 *	3, 6 *	2	9
Immediate data and accumulator	1 0 1 0 1 0 0 w | data | data if w = 1	3	3		
OR = **Or:**					
Reg/memory and register to either	0 0 0 0 1 0 d w | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 0 0 1 r/m | data | data if w = 1	3, 7 *	3, 7 *	2	9
Immediate to accumulator	0 0 0 0 1 1 0 w | data | data if w = 1	3	3		
XOR = **Exclusive or:**					
Reg/memory and register to either	0 0 1 1 0 0 d w | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 1 1 0 r/m | data | data if w = 1	3, 7 *	3, 7 *	2	9
Immediate to accumulator	0 0 1 1 0 1 0 w | data | data if w = 1	3	3		
NOT = Invert register/memory	1 1 1 1 0 1 1 w | mod 0 1 0 r/m	2, 7 *	2, 7 *	2	9

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
String Manipulation:					
MOVS = Move byte word	1010010w	5	5	2	9
CMPS = Compare byte/word	1010011w	8	8	2	9
SCAS = Scan byte/word	1010111w	7	7	2	9
LODS = Load byte/wd to AL/AX	1010110w	5	5	2	9
STOS = Store byte/wd from AL/A	1010101w	3	3	2	9
INS = Input byte/wd from DX port	0110110w	5	5	2	9, 14
OUTS = Output byte/wd to DX port	0110111w	5	5	2	9, 14
Repeated by count in CX					
MOVS = Move string	11110010 1010010w	5 + 4n	5 + 4n	2	9
CMPS = Compare string	1111001z 1010011w	5 + 9n	5 + 9n	2, 8	8, 9
SCAS = Scan string	1111001z 1010111w	5 + 8n	5 + 8n	2, 8	8, 9
LODS = Load string	11110010 1010110w	5 + 4n	5 + 4n	2, 8	8, 9
STOS = Store string	11110010 1010101w	4 + 3n	4 + 3n	2, 8	8, 9
INS = Input string	11110010 0110110w	5 + 4n	5 + 4n	2	9, 14
OUTS = Output string	11110010 0110111w	5 + 4n	5 + 4n	2	9, 14

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Control Transfer:					
CALL = Call:					
Direct within segment	11101000 | disp-low | disp-high	7 + m	7 + m	2	18
Register/memory indirect within segment	11111111 | mod 010 r/m	7+m,11+m*	7+m,11+m*	2, 8	8, 9, 18
Direct intersegment	10011010 | segment offset | segment selector	13 + m	26 + m	2	11,12,18
Protected mode only (direct intersegment):					
Via call gate to same privilege level			41 + m		8,11,12,18
Via call gate to different privilege level, no parameters			82+m		8,11,12,18
Via call gate to different privilege level, x parameters			86+4x+m		8,11,12,18
Via TSS			177+m		8,11,12,18
Via task gate			182+m		8,11,12,18
Indirect intersegment	11111111 | mod 011 r/m (mod ≠ 11)	16+n	29+n*	2	8,9,11,12,18
Protected mode only (indirect intersegment):					
Via call gate to same privileg level			44+m*		8,9,11,12,18
Via call gate different privilege level, no parameters			83+m*		8,9,11,12,13
Via call gate to different privilege level, x parameters			90+4x+m*		8,9,11,12,18
Via TSS			180+m*		8,9,11,12,18
Via task gate			185+m*		8,9,11,12,18

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Control Transfer (cont'd):					
JMP = Unconditional jump:					
Short/long	11101011 | disp-low	7+m	7+m		18
Direct within segment	11101001 | disp-low | disp-high	7+m	7+m		18
Register/memory indirect within segment	11101010 | mod 010 r/m	7+m,11+m*	7+m,11+m*	2	9, 18
Direct intersegment	11101010 | segment offset	11+m	23+m		11,12,18
	segment selector				
Protected mode only (direct intersegment):					
Via call gate to same privilege level			38+m		8,11,12,18
Via TSS			175+m		8,11,12,18
Via task gate			180+m		8,11,12,18
Indirect intersegment	11111111 | mod 101 r/m (mod ≠ 11)	15+m*	26+m*	2	8,9,11,12,18
Protected mode only (indirect intersegment):					
Via call gate to same privilege level			41+m*		8,9,11,12,18
Via TSS			178+m*		8,9,11,12,18
Via task gate			183+m*		8,9,11,12,18
RET = Return from CALL:					
Within segment	11000011	11+m	11+m	2	8,9,18
Within seg adding immediate to SP	11000010 | data-low | data-high	11+m	11+m	2	8,9,18
Intersegment	11001011	15+m	25+m	2	8,9,11,12,18
Intersegment adding immediate to SP	11001010 | data-low | data-high	15+m		2	8,9,11,12,18
Protected mode only (RET):					
To different privilege level			55+m		9,11,12,18

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format		Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Control Transfer (cont'd):						
JE/JZ = Jump on equal/zero	01110100	disp	7+m or 3	7+m or 3		18
JL/JNGE = Jump on less/not greater equal	01111100	disp	7+m or 3	7+m or 3		18
JLE/JNG = Jump on less or equal/not greater	01111110	disp	7+m or 3	7+m or 3		18
JB/JNAE = Jump on below/not above or equal	01110010	disp	7+m or 3	7+m or 3		18
JBE/JNA = Jump on below or equal/not above	01110110	disp	7+m or 3	7+m or 3		18
JP/JPE = Jump on parity/parity even	01111010	disp	7+m or 3	7+m or 3		18
JO = Jump on overflow	01110000	disp	7+m or 3	7+m or 3		18
JS = Jump on sign	01111000	disp	7+m or 3	7+m or 3		18
JNE/JNZ = Jump on not equal/not zero	01110101	disp	7+m or 3	7+m or 3		18
JNL/JGE = Jump on not less/greater or equal	01111101	disp	7+m or 3	7+m or 3		18
JNLE/JG = Jump on not less or equal/greater	01111111	disp	7+m or 3	7+m or 3		18
JNB/JAE = Jump on not below/above or equal	01110011	disp	7+m or 3	7+m or 3		18
JNBE/JA = Jump on not below or equal/above	01110111	disp	7+m or 3	7+m or 3		18
JNP/JPO = Jump on not par/par odd	01111011	disp	7+m or 3	7+m or 3		18
JNO = Jump on not overflow	01110001	disp	7+m or 3	7+m or 3		18
JNS = Jump on not sign	01111001	disp	7+m or 3	7+m or 3		18
LOOP = Loop CX times	11100010	disp	8+m or 4	8+m or 4		18
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp	8+m or 4	8+m or 4		18
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp	8+m or 4	8+m or 4		18
JCXZ = Jump on CX zero	11100011	disp	8+m or 4	8+m or 4		18

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Control Transfer (cont'd):					
ENTER = Enter procedure	11001000 | data-low | data-high | L			2, 8	8, 9
L = 0		11	11	2, 8	8, 9
L = 1		15	15	2, 8	8, 9
L > 1		16+4(L-1)	16+4(L-1)	2, 8	8, 9
LEAVE = Leave procedure	11001001	5	5	2, 8	8, 9
INT = **Interrupt:**					
Type specified	11001101 | type	23+m		2, 7, 8	
Type 3	11001100	23+m		2, 7, 8	
INTO = Interrupt on overflow	11001110	24+m or 3 (3 if no interrupt)	(3 if no interrupt)	2, 6, 8	
Protected mode only:					
Via interrupt or trap gate to same privilege level			40+m		7,8,11,12,18
Via interrupt or trap gate to fit different privilege level			78+m		7,8,11,12,18
Via Task Gate			167+m		7,8,11,12,18
IRET = Interrupt return	11001111	17+m	31+m	2, 4	8,9,11,12,15,18
Protected mode only:					
To different privilege level			55+m		8,9,11,12,15,18
To different task (NT = 1)			169+m		8,9,11,12,18
BOUND = Detect value out of range	01100010 | mod reg r/m	13 *	13 * (Use INT clock count if exception 5)	2, 6	6,8,9,11,12,18

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Processor Control					
CLC = Clear carry	11111000	2	2		
CMC = Complement carry	11110101	2	2		
STC = Set carry	11111001	2	2		
CLD = Clear direction	11111100	2	2		
STD = Set direction	11111101	2	2		
CLI = Clear interrupt	11111010	3	3		14
STI = Set interrupt	11111011	2	2		14
HLT = Halt	11110100	2	2		13
WAIT = Wait	10011011	3	3		
LOCK = Bus lock prefix	11110000	0	0		14
CTS = Clear task switched flag	00001111 | 00000110	2	2	3	13
ESC = Processor extension escape	11011TTT | mod LLL r/m (TTT LLL are opcode to processor extension)	9-20 *	9-20 *	5, 8	8, 17
SEG = Segment override prefix	001 reg 110	0	0		

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock count: Real address mode	Clock count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Protection Control					
LGDT = Load global descriptor table register	00001111 | 00000001 | mod 010 r/m	11 *	11 *	2, 3	9, 13
SGDT = Store global descriptor table register	00001111 | 00000001 | mod 000 r/m	11 *	11 *	2, 3	9
LIDT = Load interrupt descriptor table register	00001111 | 00000001 | mod 011 r/m	12 *	12 *	2, 3	9, 13
SIDT = Store interrupt descriptor table register	00001111 | 00000001 | mod 001 r/m	12 *	12*	2, 3	9
LLDT = Load local descriptor table register from register memory	00001111 | 00000000 | mod 010 r/m		17, 19 *	1	9, 11, 13
SLDT = Store local descriptor table register to register/memory	00001111 | 00000000 | mod 000 r/m		2, 3 *	1	9
LTR = Load task register from register/memory	00001111 | 00000000 | mod 011 r/m		17, 19 *	1	9, 11, 13
STR = Store task register to register memory	00001111 | 00000000 | mod 001 r/m		2, 3*	1	9
LMSW = Load machine status word from register/memory	00001111 | 00000001 | mod 110 r/m	3, 6 *	3, 6 *	2,3	9, 13
SMSW = Store machine status word	00001111 | 00000001 | mod 100 r/m	2, 3 *	2, 3 *	2, 3	9
LAR = Load access rights from register/memory	00001111 | 00000010 | mod reg r/m		14, 16 *	1	9, 11, 16
LSL = Load segment limit from register/memory	00001111 | 00000011 | mod reg r/m		14, 16 *	1	9, 11, 16
ARPL = Adjust requested privilege level: from register/memory	01100011 | mod reg r/m		10*, 11*	2	8, 9
VERR = Verify read access: register/memory	00001111 | 00000000 | mod 100 r/m		14, 16 *	1	9, 11, 16
VERW = Verify write access:	00001111 | 00000000 | mod 101 r/m		14, 16*	1	9, 11, 16

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Notes:

The effective address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

* except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

REG is assigned according to the following table:

16-bit (w = 1)	8-bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 DI

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

segment override prefix

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment register
00	ES
01	CS
10	SS
11	DS

Table 13
SAB 80286 Systems, Recommended Pullup Resistor Values

SAB 80286 Pin and name	Pullup value	Purpose
4-$\overline{S1}$	20 kΩ ± 10%	Pull $\overline{S0}$, $\overline{S1}$, and $\overline{PEACK}$ inactive during SAB 80286 hold periods
5-$\overline{S0}$		
6-$\overline{PEACK}$		
53-$\overline{ERROR}$	20 kΩ ± 10%	Pull $\overline{ERROR}$ and $\overline{BUSY}$ inactive when SAB 80287 not present (or temporarily removed from socket)
54-$\overline{BUSY}$		
63-$\overline{READY}$	910 Ω ± 5%	Pull $\overline{READY}$ inactive within required minimum time (CL = 150 pF)

Absolute Maximum Ratings

Temperature under bias	T_C = 0 to 100°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to +7 V
Power dissipation	3.3 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_C = 0 to 85°C
V_{CC} = +5 V ±5%

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input low voltage	V_{IL}	−0.5	+0.8	V	–
Input high voltage	V_{IH}	2.0	V_{CC}+0.5	V	–
Clock input low voltage	V_{CL}	−0.5	+0.6	V	–
Clock input high voltage	V_{CH}	3.8	V_{CC}+0.5	V	–
Output low voltage	V_{OL}	–	0.45	V	I_{OL} = 2.0 mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = −400 µA
Power supply current	I_{CC}	–	600	mA	T_C = 0°C (turn on) [1]
Input leakage current	I_{LI}	–	±10	µA	0 V ≤ V_{IN} ≤ V_{CC}
CLK input leakage current	I_{LCR}	–	±10	µA	0.45 V ≤ V_{IN} ≤ V_{CC}
CLK input leakage current	I_{LCR}	–	±1	mA	0 V ≤ V_{IN} < 0.45 V
Input sustaining current on $\overline{\text{BUSY}}$ and $\overline{\text{ERROR}}$	I_{IL}	30	500	µA	V_{IN} = 0 V
Output leakage current	I_{LO}	–	±10	µA	0.45 V ≤ V_{OUT} ≤ V_{CC}
Output leakage current	I_{LO}	–	±1	mA	0 V ≤ V_{OUT} < 0.45 V
Capacitance of inputs (all input exept CLK)	C_{IN}	–	10	pF	f_C = 1 MHz [2]
Capacitance of I/O or outputs	C_{IO}	–	20	pF	f_C = 1 MHz [2]
Capacitance of CLK, $\overline{\text{READY}}$, $\overline{\text{BUSY}}$, $\overline{\text{ERROR}}$, and RESET inputs	C_{CLK}	–	20	pF	f_C = 1 MHz [2]

[1] Low temperature is worst case.

[2] Not 100% tested, guaranteed by design characterization.

AC Characteristics SAB 80286

T_C = 0 to 85°C
V_{CC} = +5 V ±5%

AC timings are referenced to 0.8 V and 2.0 V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
System clock (CLK) period	t_1	62	250	ns	–
System clock (CLK) low time	t_2	15	225	ns	at 1.0 V
System clock (CLK) high time	t_3	25	235	ns	at 3.6 V
System clock (CLK) rise time	t_{17}	–	10	ns	1.0 V to 3.6 V
System clock (CLK) fall time	t_{18}	–	10	ns	3.6 V to 1.0 V
Async inputs, setup time	t_4	20	–	ns	1)
Async inputs, hold time	t_5	20	–	ns	1)
RESET setup time	t_6	28	–	ns	–
RESET hold time	t_7	5	–	ns	–
Read data setup time	t_8	10	–	ns	–
Read data hold time	t_9	8	–	ns	–
$\overline{\text{READY}}$ setup time	t_{10}	38	–	ns	–
$\overline{\text{READY}}$ hold time	t_{11}	25	–	ns	–
Status/$\overline{\text{PEACK}}$ active delay	t_{12a}	1	40	ns	2) 3)
Status/$\overline{\text{PEACK}}$ inactive delay	t_{12b}	1	40	ns	2) 3)
Address valid delay	t_{13}	1	60	ns	2) 3)
Write data valid delay	t_{14}	0	50	ns	2) 3)
Address/status/data float delay	t_{15}	0	50	ns	2) 4)
HLDA valid delay	t_{16}	0	50	ns	2) 3)
Address valid to status valid setup time	t_{19}	38	–	ns	3) 5) 6)

1) Asynchronous inputs are INTR, NMI, HOLD, PEREQ, $\overline{\text{ERROR}}$, and $\overline{\text{BUSY}}$. The specification is given only for testing purposes, to assure recognition at a specific CLK edge.

2) Delay from 1.0 V on the CLK to 0.8 V or 2.0 V or float on the output as appropriate for valid or floating condition.

3) Output load C_L = 100 pF

4) Float condition occurs when output current is less than I_{LO} in magnitude.

5) Delay measured from address either reaching 0.8 V or 2.0 V (valid) to status going active reaching 2.0 V or status going inactive reaching 0.8 V.

6) For a load capacitance of 10 pF on status/$\overline{\text{PEACK}}$ lines, subtract typically 7 ns.

SAB 82284 Timing Requirements

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
$\overline{\text{SRDY}}/\overline{\text{SRDYEN}}$ setup time	t_{11}	15	–	ns	–
$\overline{\text{SRDY}}/\overline{\text{SRDYEN}}$ hold time	t_{12}	0	–	ns	–
$\overline{\text{ARDY}}/\overline{\text{ARDYEN}}$ setup time	t_{13}	0	–	ns	[1]
$\overline{\text{ARDY}}/\overline{\text{ARDYEN}}$ hold time	t_{14}	30	–	ns	[1]
PCLK delay	t_{19}	0	45	ns	C_L = 75 pF I_{OL} = 5 mA I_{OH} = −1 mA

SAB 82288 Timing Requirements

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
CMDLY setup time	t_{12}	20	–	ns	–
CMDLY hold time	t_{13}	0	–	ns	–
Command inactive delay	t_{30}	3	25	ns	[2]
Command active delay	t_{29}	3	25	ns	[2]
ALE active delay	t_{16}	3	20	ns	[3]
ALE inactive delay	t_{17}	–	20	ns	[3]
DT/$\overline{\text{R}}$ read active delay	t_{19}	–	25	ns	[3]
DT/$\overline{\text{R}}$ read inactive delay	t_{22}	5	35	ns	[3]
DEN read active delay	t_{20}	5	35	ns	[3]
DEN read inactive delay	t_{21}	3	35	ns	[3]
DEN write active delay	t_{23}	–	30	ns	[3]
DEN write inactive delay	t_{24}	3	30	ns	[3]

[1] These times are given for testing purposes to assure a predetermined action.

[2] C_L = 300 pF max.
I_{OL} = 32 mA max.
I_{OH} = −5 mA max.

[3] C_L = 150 pF
I_{OL} = 16 mA max.
I_{OH} = −1 mA max.

AC Characteristics SAB 80286-1

T_C = 0 to 85°C
V_{CC} = +5 V ± 5%

AC timings are referenced to 0.8 V and 2.0 V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
System clock (CLK) period	t_1	50	250	ns	–
System clock (CLK) low time	t_2	12	234	ns	at 1.0 V
System clock (CLK) high time	t_3	16	238	ns	at 3.6 V
System clock (CLK) rise time	t_{17}	–	8	ns	1.0 V to 3.6 V
System clock (CLK) fall time	t_{18}	–	8	ns	3.6 V to 1.0 V
Async inputs, setup time	t_4	20	–	ns	1)
Async inputs, hold time	t_5	20	–	ns	1)
RESET setup time	t_6	23	–	ns	–
RESET hold time	t_7	5	–	ns	–
Read data setup time	t_8	8	–	ns	–
Read data hold time	t_9	8	–	ns	–
$\overline{\text{READY}}$ setup time	t_{10}	26	–	ns	–
$\overline{\text{READY}}$ hold time	t_{11}	25	–	ns	–
Status/$\overline{\text{PEACK}}$ active delay	t_{12a}	1	28	ns	2) 3)
Status/$\overline{\text{PEACK}}$ inactive delay	t_{12b}	1	30	ns	2) 3)
Address valid delay	t_{13}	1	47	ns	2) 3)
Write data valid delay	t_{14}	0	40	ns	2) 3)
Address/status/data fload delay	t_{15}	0	47	ns	2) 4)
HLDA valid delay	t_{16}	0	47	ns	2) 3)
Address valid to status valid setup time	t_{19}	27	–	ns	3) 5) 6)

1) Asynchronous inputs are INTR, NMI, HOLD, PEREQ, $\overline{\text{ERROR}}$, and $\overline{\text{BUSY}}$. The specification is given only for testing purposes, to assure recognition at a specific CLK edge.

2) Delay from 1.0 V on the CLK to 0.8 V or 2.0 V or float on the output as appropriate for valid or floating condition.

3) Output load C_L = 100 pF

4) Float condition occurs when output current is less than I_{LO} in magnitude.

5) Delay measured from address either reaching 0.8 V or 2.0 V (valid) to status going active reaching 2.0 V or status going inactive reaching 0.8 V.

6) For a load capacitance of 10 pF on status/$\overline{\text{PEACK}}$ lines, subtract maximum 7 ns.

SAB 82284-1 Timing Requirements

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
$\overline{\text{SRDY}}/\overline{\text{SRDYEN}}$ setup time	t_{11}	15	–	ns	–
$\overline{\text{SRDY}}/\overline{\text{SRDYEN}}$ hold time	t_{12}	0	–	ns	–
$\overline{\text{ARDY}}/\overline{\text{ARDYEN}}$ setup time	t_{13}	0	–	ns	[1]
$\overline{\text{ARDY}}/\overline{\text{ARDYEN}}$ hold time	t_{14}	30	–	ns	[1]
PCLK delay	t_{19}	0	35	ns	$C_L = 75$ pF $I_{OL} = 5$ mA $I_{OH} = -1$ mA

SAB 82288-1 Timing Requirements

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
CMDLY setup time	t_{12}	15	–	ns	–
CMDLY hold time	t_{13}	0	–	ns	–
Command inactive delay	t_{30}	5	20	ns	[2]
Command active delay	t_{29}	3	21	ns	[2]
ALE active delay	t_{16}	3	16	ns	[3]
ALE inactive delay	t_{17}	–	19	ns	[3]
DT/$\overline{\text{R}}$ read active delay	t_{19}	–	23	ns	[3]
DT/$\overline{\text{R}}$ read inactive delay	t_{22}	5	20	ns	[3]
DEN read active delay	t_{20}	5	21	ns	[3]
DEN read inactive delay	t_{21}	3	21	ns	[3]
DEN write active delay	t_{23}	–	23	ns	[3]
DEN write inactive delay	t_{24}	3	19	ns	[3]

[1] These times are given for testing purpose to assure a predetermined action

[2] $C_L = 300$ pF max.
$I_{OL} = 32$ mA max.
$I_{OH} = -5$ mA max.

[3] $C_L = 150$ pF
$I_{OL} = 16$ mA max.
$I_{OH} = -1$ mA max.

AC Characteristics SAB 80286-12

T_C = 0 to 85°C
V_{CC} = +5 V ±5%

AC timings are referenced to 0.8 V and 2.0 V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
System clock (CLK) period	t_1	40	250	ns	–
System clock (CLK) low time	t_2	11	237	ns	at 1.0 V
System clock (CLK) high time	t_3	13	239	ns	at 3.6 V
System clock (CLK) rise time	t_{17}	–	8	ns	1.0 V to 3.6 V
System clock (CLK) fall time	t_{18}	–	8	ns	3.6 V to 1.0 V
Async inputs, setup time	t_4	15	–	ns	1)
Async inputs, hold time	t_5	15	–	ns	1)
RESET setup time	t_6	18	–	ns	–
RESET hold time	t_7	5	–	ns	–
Read data setup time	t_8	5	–	ns	–
Read data hold time	t_9	6	–	ns	–
$\overline{\text{READY}}$ setup time	t_{10}	22	–	ns	–
$\overline{\text{READY}}$ hold time	t_{11}	20	–	ns	–
Status/$\overline{\text{PEACK}}$ active delay	t_{12a}	3	18	ns	2) 3)
Status/$\overline{\text{PEACK}}$ inactive delay	t_{12b}	3	20	ns	2) 3)
Address valid delay	t_{13}	1	32	ns	2) 3)
Write data valid delay	t_{14}	0	30	ns	2) 3)
Address/status/data float delay	t_{15}	0	32	ns	2) 4)
HLDA valid delay	t_{16}	0	25	ns	2) 3)
Address valid to status valid setup time	t_{19}	22	–	ns	3) 5)

1) Asynchronous inputs are INTR, NMI, HOLD, PEREQ, $\overline{\text{ERROR}}$, and $\overline{\text{BUSY}}$. The specification is given only for testing purposes, to assure recognition at a specific CLK edge.

2) Delay from 1.0 V on the CLK to 0.8 V or 2.0 V or float on the output as appropriate for valid or floating condition.

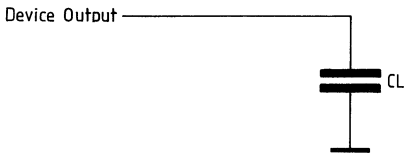
3) Output load C_L = 100 pF

4) Float condition occurs when output current is less than I_{LO} in magnitude.

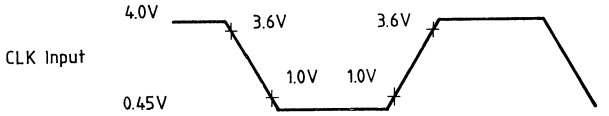
5) Delay measured from address either reaching 0.8 V or 2.0 V (valid) to status going active reaching 2.0 V or status going inactive reaching 0.8 V.

AC Testing Waveforms

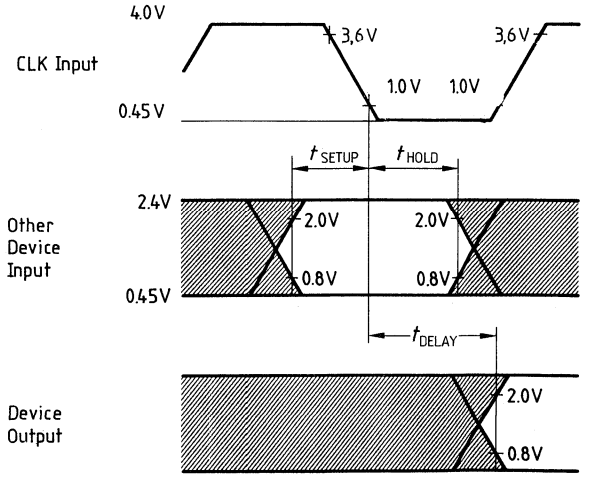
Test Loading on Outputs



Drive and Measurement Points – CLK Input

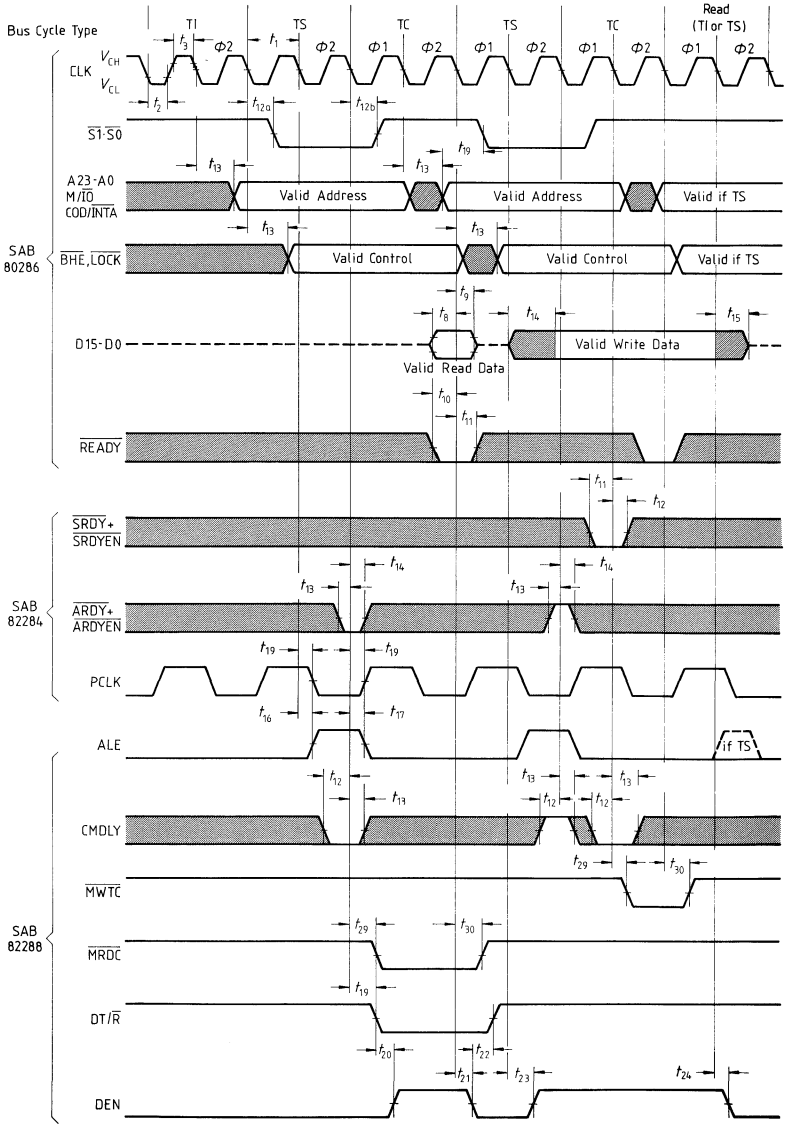


Setup, Hold and Delay Time Measurement – General

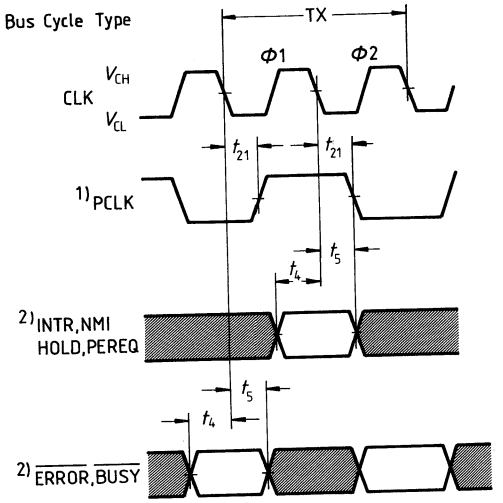


Waveforms

Major Cycle Timing



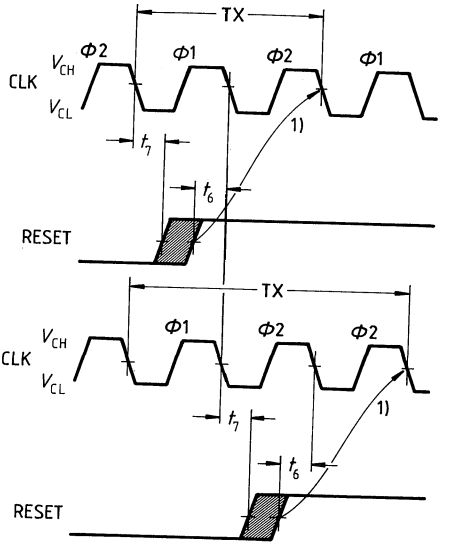
Asynchronous Input Signal Timing



1) PCLK indicates which processor cycle phase will occur on the next CLK, PCLK may not indicate the correct phase until the first bus cycle is performed.

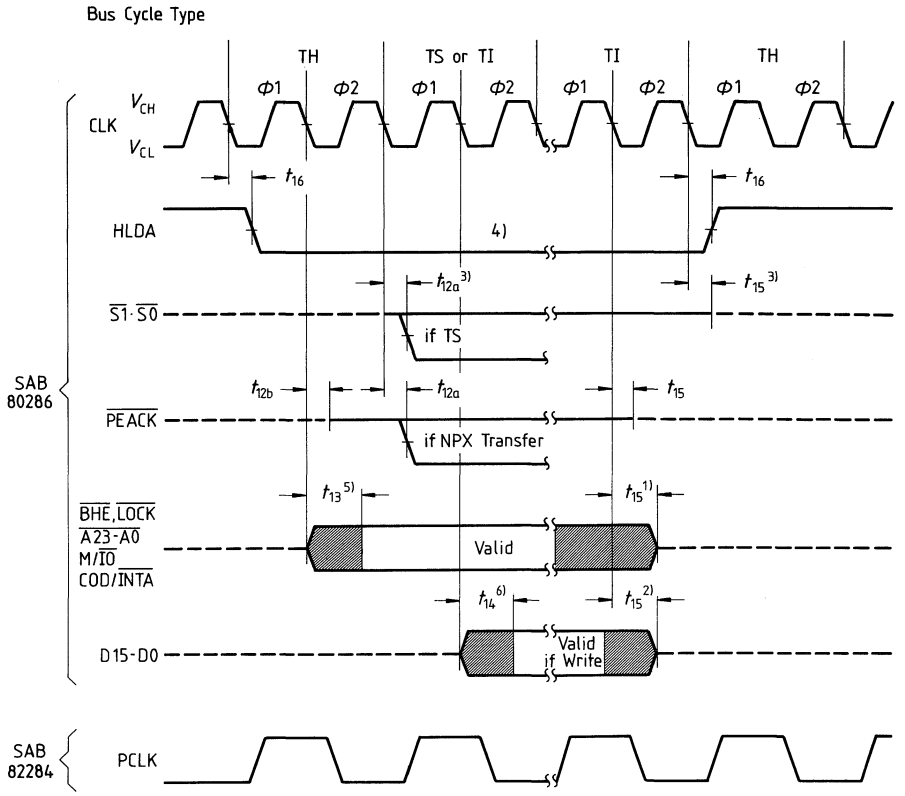
2) These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

Reset Input Timing and Subsequent Processor Cycle Phase



1) When RESET meets the setup time shown, the next CLK will start or repeat Φ 2 of a processor cycle.

Exciting and Entering HOLD



1) These signals may not be driven by the SAB 80286 during the time shown. The worst case in terms of latest float time is shown.

2) The data bus will be driven as shown if the last cycle before TI in the diagram was a write TC.

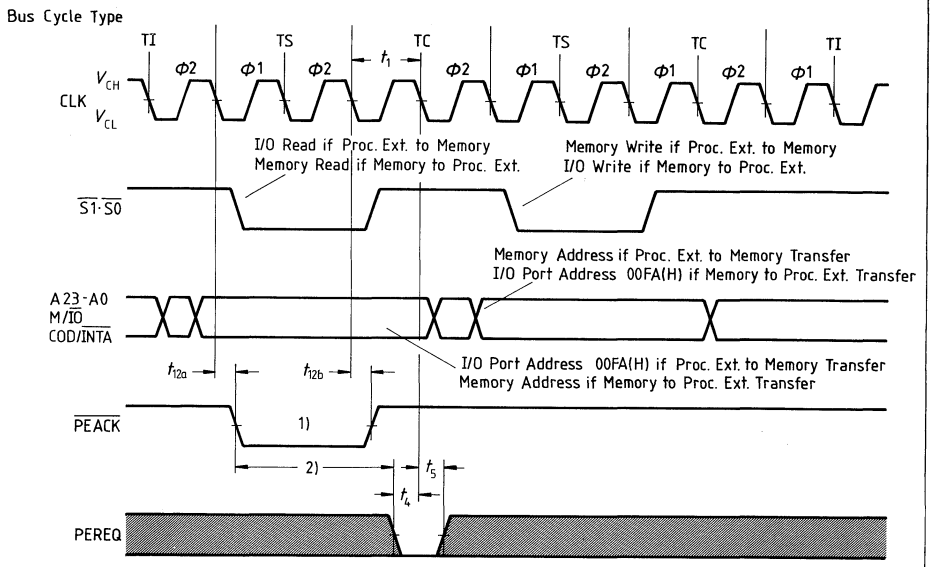
3) The SAB 80286 floats its status pins during TH. Pullup resistors in SAB 80288 keep these signals high.

4) For HOLD request set up to HLDA (refer to figure on Multibus write terminated by async ready).

5) $\overline{BHE}$ and $\overline{LOCK}$ are driven at this time but will not become valid until TS.

6) The data bus will remain in tristate off if a read cycle is performed.

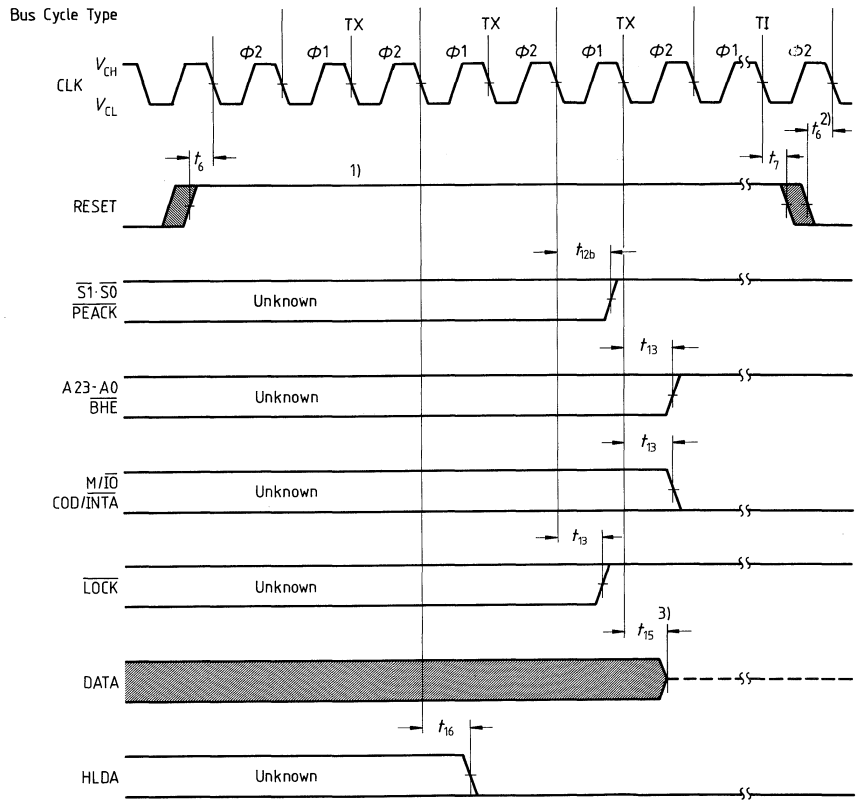
PEREQ/PEACK Timing for One Transfer Only



1) PEACK always goes active during the first bus operation of a processor extension data operand transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address 00FA(H).

2) To prevent a second processor extension data operand transfer, the worst case maximum time (shown above) is: $3\times t_1 - t_{12a\,max} - t_{4\,min}$. The actual, configuration-dependent, maximum time is: $3\times t_1 - t_{12a\,max} - t_{4\,min} + A\times 2\times t_1$.
A is the number of extra TC states added to either the first or second bus operation of the processor extension data operand transfer sequence.

Initial SAB 80286 Pin State during RESET



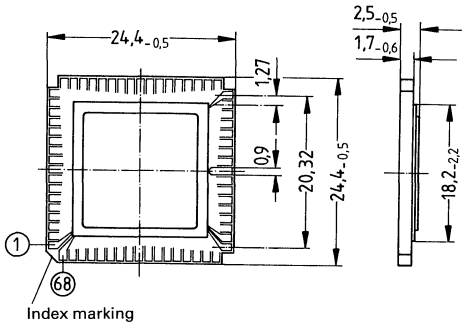
1) Setup time for RESET↑ may be violated with the consideration that Φ 1 of the processor clock may begin one system CLK period later.

2) Setup and hold times for RESET↓ must be met for proper operation.

3) The data bus is only guaranteed to be in tristate off at the time shown.

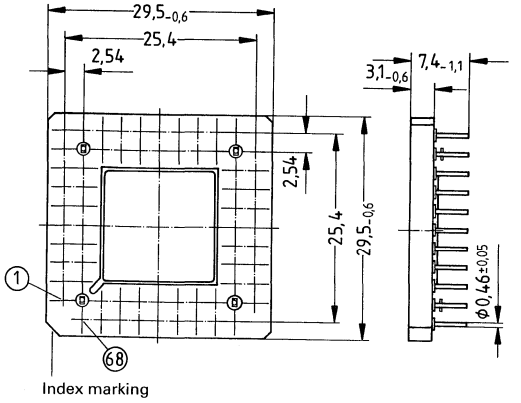
Package Outlines

Ceramic Package, C-CC, 68 Pins (SMD)



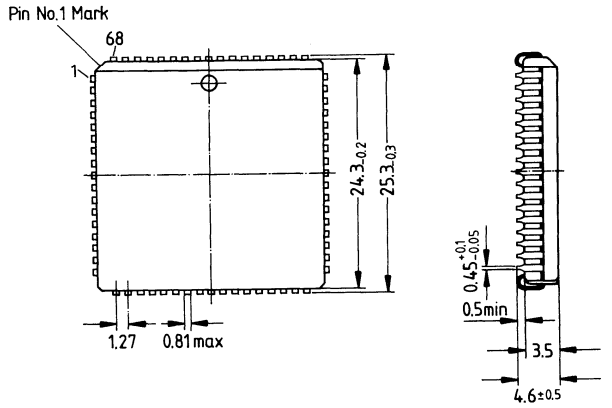
Dimensions in mm

Pin Grid Array, C-PGA, 68 Pins



Dimensions in mm

Plastic Package, PL-CC-68, 68 Pins (SMD)



Dimensions in mm

Ordering Information

Type	Ordering code	Description
SAB 80286-R	Q67120-C151	16-bit microprocessor, 8 MHz (C-CC)
SAB 80286-1-R	Q67120-C268	16-bit microprocessor, 10 MHz (C-CC)
SAB 80286-A	Q67120-C204	16-bit microprocessor, 8 MHz (PGA)
SAB 80286-1-A	Q67120-C270	16-bit microprocessor, 10 MHz (PGA)
SAB 80286-N	Q67120-C330	16-bit microprocessor, 8 MHz (PL-CC)
SAB 80286-1-N	Q67120-C269	16-bit microprocessor, 10 MHz (PL-CC)
SAB 80286-12-N	Q67120-C381	16-bit microprocessor, 12.5 MHz (PL-CC)
SAB 80286-12-A	Q67120-C380	16-bit microprocessor, 12.5 MHz (PGA)
SAB 80286-12-R	Q67120-C382	16-bit microprocessor, 12.5 MHz (C-CC)

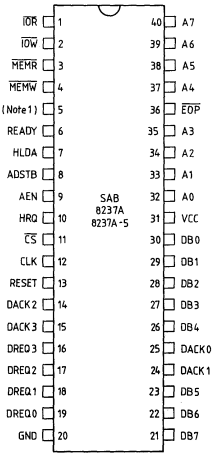
System and Support Components

Preliminary

SAB 8237A, SAB 8237A-5 High Performance Programmable DMA Controller

- Four Independent DMA Channels
- Enable/Disable Control of Individual DMA Requests
- Memory-to-Memory Transfers
- Memory Block Initialization
- Address Increment or Decrement
- Independent Autoinitialization of all Channels
- High performance: Transfers up to 1.6 MBytes/Second with 5 MHz SAB 8237A-5
- Directly Expandable to any Number of Channels
- End of Process Input for Terminating Transfers
- Software DMA Requests
- Independent Polarity Control for DREQ and DACK Signals
- Single +5 V Power Supply
- 40 Pin Dual-In-Line Package
- Fully compatible with the Industry Standard 9517A/8237A

Pin Configuration



1) Pin always tied high

Pin Names

DB7-DBØ	Data Bus (bidirectional)
IOR, IOW	I/O Read and Write Input/Output
MEMR, MEMW	Memory Read and Write Output
AØ-A3	Address Input/Output
A4-A7	Adress Output
CS	Chip Select Input
CLK	Clock Input
READY	Ready Input
HRQ	Hold Request Output
HLDA	Hold Acknowledge Input
RESET	Reset Input
DREQØ-DREQ3	DMA Request Input
DACKØ-DACK3	DMA Acknowledge Output
AEN	Address Enable Output
ADSTB	Address Strobe Output
EOP	End of Process Input/Output

The SAB 8237A Multimode Direct Memory Access (DMA) Controller is designed to improve system performance by allowing external devices to directly transfer information to or from system memory. Memory-to-memory transfer capability is also provided.

The SAB 8237A contains four independent channels, each with a separate register set, and may be expanded to any number of channels by cascading additional controller chips. The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original state following an End of Process (EOP). Each channel has a full 64K address and word count capability.

The SAB 8237A is fabricated in +5 V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 40-pin DIP. The SAB 8237A-5 is the 5 MHz version of the standard 3 MHz SAB 8237A respectively.

3.85

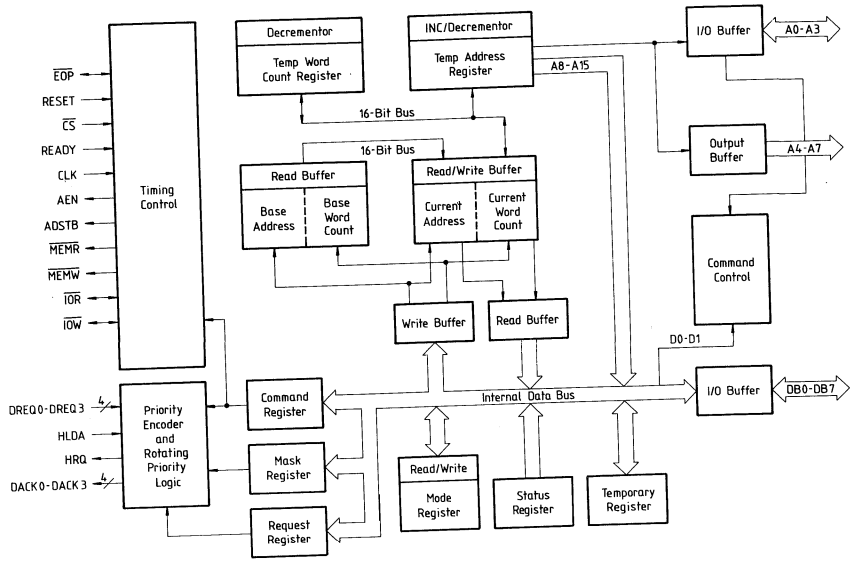
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
$\overline{IOR}$	1	I/O	I/O READ I/O Read is a bidirectional active low three-state line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the SAB 8237A to access data from a peripheral device during a DMA Write transfer.
$\overline{IOW}$	2	I/O	I/O WRITE I/O Write is a bidirectional active low three-state line. In the idle cycle it is an input control signal used by the CPU to load information into the SAB 8237A. In the Active cycle it is an output control signal used by the SAB 8237A to load data to a peripheral device during a DMA Read transfer. Write operations by the CPU to the SAB 8237A require a rising $\overline{IOW}$ edge following each data byte transfer. It is not sufficient to hold the $\overline{IOW}$ pin low and toggle $\overline{CS}$.
$\overline{MEMR}$	3	O	MEMORY READ The Memory Read signal is an active low three-state output used to access data from the selected memory location during a memory-to-peripheral or a memory-to-memory transfer.
$\overline{MEMW}$	4	O	MEMORY WRITE The Memory Write signal is an active low three-state output used to write data to the selected memory location during a peripheral-to-memory or a memory-to-memory transfer.
–	5	I	Pin 5 must be tied high.
READY	6	I	READY Ready is an input used to extend the memory read and write pulses from the SAB 8237A to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.
HLDA	7	I	HOLD ACKNOWLEDGE The active high Hold Acknowledge from the CPU indicates that control of the system busses has been relinquished.
ADSTB	8	O	ADDRESS STROBE The active high Address Strobe is used to strobe the upper address byte from DBØ-DB7 into an external latch.
AEN	9	O	ADDRESS ENABLE Address Enable is an active high signal used to disable the system bus during DMA cycles and to enable the output of the external latch which holds the upper byte of the address. Note that during DMA transfers HLDA and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed as programmed I/O during the DMA operation. The SAB 8237A automatically deselects itself by disabling the $\overline{CS}$ input during DMA transfers.

Symbol	Number	Input (I) Output (O)	Function
HRQ	10	O	HOLD REQUEST The Hold Request to the CPU is used by the DMA to request control of the system bus. Software requests or unmasked DREQs cause the SAB 8237A to issue HRQ.
$\overline{CS}$	11	I	CHIP SELECT Chip Select is an active low input used to select the SAB 8237A as an I/O device during an I/O Read or I/O Write by the host CPU. This allows CPU communication on the data bus. During multiple transfers to or from the SAB 8237A by the host CPU $\overline{CS}$ may be held low providing $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer.
CLK	12	I	CLOCK This input controls the internal operations of the SAB 8237A and its rate of data transfers. The input may be driven at up to 3 MHZ for the standard SAB8237A and up to 5 MHz for the SAB 8237A-5.
RESET	13	I	RESET Reset is an asynchronous active high input which clears the Command, Status, Request and Temporary register. It also clears the First/Last Flip/Flop and sets the Mask register. Following a Reset the device is in the idle cycle.
DACKØ DACK1 DACK2 DACK3	25 24 14 15	O O O O	DMA ACKNOWLEDGE The DMA Acknowledge lines indicate that a channel is active. In many systems they will be used to select a peripheral. Only one DACK will be active at a time and none will be active unless the DMA is in control of the bus. The polarity of these lines is programmable. Reset initializes them to active-low.
DREQØ DREQ1 DREQ2 DREQ3	19 18 17 16	I I I I	DMA REQUEST The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service in Fixed Priority, DREQØ has the highest priority and and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. The Polarity of DREQ is programmable. Reset initializes these lines to active high.
DBØ-DB7	30-26, 23-21	I/O	DATA BUS The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled during the I/O Read by the host CPU, permitting the CPU to examine the contents of an Address register, the Status register, the Temporary register or a Word Count register. The Data Bus is enabled to input data during a host CPU I/O write, allowing the CPU to program the SAB 8237A control registers. During DMA cycles the most significant eight bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the source memory location comes into the SAB 8237A's Temporary register on the read-from-memory half of the operation. On the write-to-memory half of the operation, the data bus outputs the Temporary register data into the destination memory location.

Symbol	Number	Input (I) Output (O)	Function
A∅–A3	32–35	I/O	ADDRESS ∅–3 The four least significant address lines are bidirectional 3-state signals. During DMA idle cycles they are inputs and allow the host CPU to load or read control registers. When the DMA is active, they are outputs and provide the lower 4-bits of the output address.
A4–A7	37–40	O	ADDRESS 4–7 The four most significant address lines are three-state outputs and provide four bits of address. These lines are enabled only during DMA service.
$\overline{EOP}$	36	I/O	END OF PROCESS $\overline{EOP}$ is an active low bidirectional open-drain signal providing information concerning the completion of DMA service. When a channel's Word Count goes to zero, the SAB 8237A pulses $\overline{EOP}$ low to provide the peripheral with a completion signal. $\overline{EOP}$ may also be pulled low by the peripheral to cause premature completion. The reception of $\overline{EOP}$, either internal or external, causes the currently active channel to terminate the service, to set its TC bit in the Status register and to reset its request bit. If Autoinitialization is selected for the channel, the current registers will be updated from the base registers. Otherwise the channel's mask bit will be set and the register contents will remain unaltered. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ always applies to the channel with an active DACK; external $\overline{EOP}$s are disregarded when DACK∅-DACK3 are all inactive if the DMA is in state SI. In situations where two or more SAB 8237A DMAs are cascaded, the $\overline{EOP}$ pins should be logically OR'ed (not wire-OR'ed). Because $\overline{EOP}$ is an open-drain signal, an external pullup resistor is required. Values of 3.3 kΩ or 4.7 kΩ are recommanded; the $\overline{EOP}$ pin cannot sink the current passed by a 1 kΩ pullup.
VCC	31	–	POWER SUPPLY (+5V)
GND	20	–	GROUND (0V)

Block Diagram



Register Description

Current Address Register
Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer.

Current Word Count Register
Each channel has a 16-bit Current Word Count register. This register should be programmed with, and will return on a CPU read, a value one less than the number of words to be transferred. The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes to zero, a TC will be generated.

Base Address and Base Word Count Registers
Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original values of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes during DMA programming by the microprocessor.

Command Register
This 8-bit register controls the operation of the SAB 8237A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset.

Mode Registers
Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits Ø and 1 determine which channel Mode register is to be written.

Request Register
The SAB 8237A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a Reset.

Mask Register
Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset.

Status Register
The Status registers may be read out of the SAB 8237A by the microprocessor. It indicates which channels have reached a terminal count and which channels have pending DMA requests.

Temporary Register
The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition.

Functional Description

DMA Operation
The SAB 8237A is designed to operate in two major cycles. These are called Idle and Activa cycles. Each device cycle is made up of a number of states. State I (SI)is the inactive state. It is entered when the SAB 8237A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State Ø (SØ) is the first state of a DMA service. The SAB 8237A has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the CPU will signal that transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted before S4 by the use of the Ready line on the SAB 8237A.
Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for each complete transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23 and S24) for the write-to-memory half of the transfer.

Idle Cycle
When no channel is requesting service, the SAB 8237A will enter the Idle cycle and perform "SI" states. In this cycle the SAB 8237A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the SAB 8237A.

Active Cycle
When the SAB 8237A is in the Idle cycle and a channel requests a DMA service, the device will output a HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode
In Single Transfer mode, the SAB 8237A will make a one-byte transfer during each HRQ/HLDA handshake. When DREQ goes active, HRQ will go active. After the CPU responds by driving HRQ active, a one-byte transfer will take place. Following the transfer, HRQ will go inactive, the word count will be decremented and the address will be either incremented or decremented.

Block Transfer Mode
In Block Transfer mode, the SAB 8237A will continue making transfers until a TC (caused by the word count going to zero) or an external End of Process ($\overline{EOP}$) is encountered.

Demand Transfer Mode
In Demand Transfer mode the device will continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus, the device requesting service may discontinue transfers by bringing DREQ inactive. Service may be resumed by asserting an active DREQ once again.

Cascade Mode
This mode is used to cascade more than one SAB 8237A together for simple system expansion. The HRQ and HLDA signals from the additional SAB 8237A are connected to the DREQ and DACK signals of a channel of the initial SAB 8237A.

TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{IOR}$ and $\overline{MEMW}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers; the SAB8237A operates as in Read or Write transfers generating addresses, responding to $\overline{EOP}$, etc., however, the memory and I/O control lines remain inactive.

Memory-to-Memory

The SAB8237A includes a block move capability that allows blocks of data to be moved from one memory adress space to another. Channel Ø forms the source address and channel 1 forms the destination address. The channel 1 word count is used. A memory-to-memory transfer is initiated by setting a software DMA request for channel Ø.

Autoinitialize

By programming a bit in the Mode register a channel may be set up for an Autoinitialize operation. During Autoinitialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word Count registers of that channel following $\overline{EOP}$.

Extended Write

For Flyby Transactions late write is normally used, as this allows sufficient time for the $\overline{IOR}$ signal to get data from the peripheral onto the bus before $\overline{MEMW}$ is activated. In some systems, performance can be improved by starting the write cycle earlier.

Address Generation

In order to reduce pin count, the SAB 8237A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through the 3-state enable control signal of the latch. The lower order address bits are output by the SAB 8237A directly. To save time and speed transfers, the SAB 8237A executes S1 states only when updating of A8–A15 in the latch is necessary.

Compressed Timing

In order to achieve even greater throughput where system characteristics permit, the SAB 8237A can compress the transfer time to two clock cycles. By removing state S3 the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write.

Priority

The SAB 8237A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel Ø. The second schema is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.

Software Commands

There are two special software commands which can be executed in the Program Condition.
Clear First/Last Flip/Flop: This command may be issued prior to writing or reading SAB 8237A address or word count information. This initializes the Flip/Flop to a known state so that subsequent accesses to register contents by the microprocessor will address lower and upper bytes in the correct sequence.
Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary and Internal First/Last Flip/Flop registers are cleared and the Mask register is set.

Absolute Maximum Ratings [1]

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to + 150°C
Voltage on Any Pin with Respect to Ground (VSS)	−0.5 to + 7 V
Power Dissipation	2 W

D.C. Characteristics

TA = 0 to 70°C; VCC = 5 V ± 5%; VSS = 0 V

Symbol	Parameter	Limit Values			Unit	Test Condition	
		Min.	Typ. [2]	Max.			
VOH	Output High Voltage	2.4		–		IOH = −200 µA	
		3.3				IOH = −100 µA (HRQ only)	
VOL	Output Low Voltage	–		0.40	V	IOL = 3.2 mA	
VIH	Input High Voltage	2.0	–	VCC+0.5		–	
VIL	Input Low Voltage	−0.5		0.8			
ILI	Input Load Current	–		±10	µA	0 V ≤ VIN ≤ VCC	
ILO	Output Leakage Current					0.4 V ≤ VOUT < VCC	
ICC	VCC Supply Current		110	130	mA	TA = +25°C	All outputs disconnected
			130	150		TA = 0°C	
CO	Output Capacitance		4	8	pF	fc = 1.0 MHz, Inputs = 0 V	
CI	Input Capacitance		8	15			
CIO	I/O Capacitance		10	18			

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) Typical values are for TA = 25°C, nominal supply voltage and nominal processing parameters.

A.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 5%; V_{SS} = 0 V

DMA (Master) Mode

Symbol	Parameter	Limit Values				Unit
		8237A		8237A-5		
		Min.	Max.	Min.	Max.	
TAEL	AEN High from CLK Low (S1) Delay Time		300		200	
TAET	AEN Low from CLK High (S1) Delay Time		200		130	
TAFAB	ADR Active to Float Delay from CLK High	–	150	–	90	
TAFC	$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Float from CLK High		150		120	
TAFDB	DB Active to Float Delay from CLK High		250		170	
TAHR	ADR from $\overline{\text{READ}}$ High Hold Time	TCY–100		TCY–100		
TAHS	DB from ADSTB Low Hold Time	50	–	40	–	
TAHW	ADR from $\overline{\text{WRITE}}$ High Hold Time	TCY–50		TCY–50		
TAK	DACK Valid from CLK Low Delay Time [1]		250		170	
	$\overline{\text{EOP}}$ High from CLK High Delay Time [2]	–	250	–	170	
	$\overline{\text{EOP}}$ Low to CLK High Delay Time		250		170	
TASM	ADR Stable from CLK High		250		170	
TASS	DB to ADSTB Low Setup Time	100		100	ns	ns
TCH	CLK High Time (transitions ≤ 10 ns)	120	–	80	–	
TCL	CLK Low Time (transitions ≤ 10 ns)	150		68		
TCY	CLK Cycle Time	320		200		
TDCL	CLK High to $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Low Delay [3]		270		190	
TDCTR	$\overline{\text{READ}}$ High from CLK High (S4) Delay Time [3]		270		190	
TDCTW	$\overline{\text{WRITE}}$ High from CLK High (S4) Delay Time [3]	–	200	–	130	
TDQ1	HRQ Valid from CLK High Delay Time [4]		160		120	
TDQ2			250		120	
TEPS	$\overline{\text{EOP}}$ Low from CLK Low Setup Time	60	–	40	–	
TEPW	$\overline{\text{EOP}}$ Pulse Width	300		220		
TFAAB	ADR Float to Active Delay from CLK High		250		170	
TFAC	$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Active from CLK High		200		150	
TFADB	DB Float to Active Delay from CLK High		300		200	

Notes see next page.

Symbol	Parameter	Limit Values				Unit
		8237A		8237A-5		
		Min.	Max.	Min.	Max.	
THS	HLDA Valid to CLK High Setup Time	100		75		
TIDH	Input Data from $\overline{MEMR}$ High Hold Time	0		0		
TIDS	Input Data to $\overline{MEMR}$ High Setup Time	250		170		
TODH	Output Data from $\overline{MEMW}$ High Hold Time	20	–	10	–	ns
TODV	Output Data Valid to $\overline{MEMW}$ High [5]	200		125		
TQS	DREQ to CLK Low (S1, S4) Setup Time [1]	0		0		
TRH	CLK to READY Low Hold Time	20		20		
TRS	READY to CLK Low Setup Time	100		60		
TSTL	ADSTB High from CLK High Delay Time	–	200	–	130	
TSTT	ADSTB Low from CLK High Delay Time		140		90	
TQH	DREQ from DACK Valid Hold Time	0	–	0	–	
TRQHA	HRQ to HLDA Delay Time	1		1		clk

1) DREQ and DACK signals may be active high or low. Timing diagrams assume the active high mode.

2) $\overline{EOP}$ is an open collector output. This parameter assumes the presence of a 2.2 kΩ pullup to *V*CC.

3) The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be TCY -100 ns and for extended write will be 2TCY -100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY -50 ns and for compressed read will be TCY -50 ns.

4) TDQ is specified for two different output high levels. TDQ1 is measured at 2.0 V. TDQ2 is measured a 3.3 V. The value for TDQ2 assumes an external 3.3 kΩ pull-up resistor connected from HRQ to *V*CC.

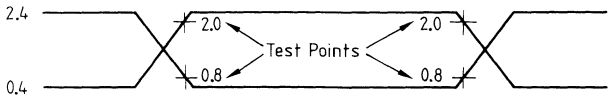
5) If N wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by N (TCY).

Peripheral (Slave) Mode

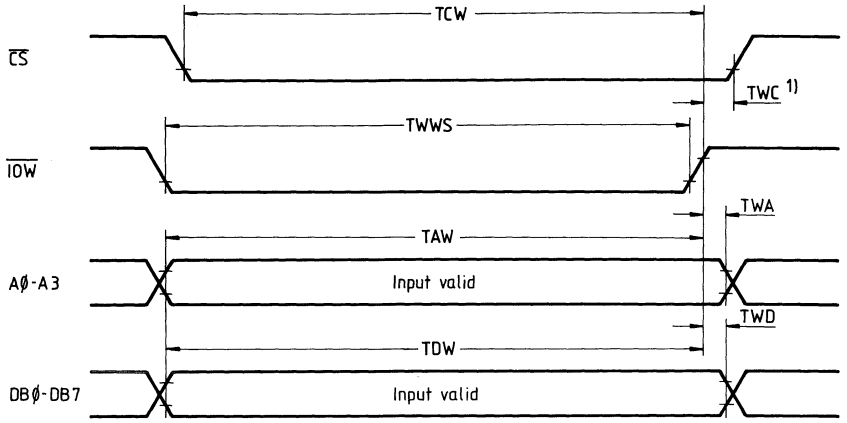
Symbol	Parameter	Limit Values				Unit
		8237A		8237A-5		
		Min.	Max.	Min.	Max.	
TAR	ADR Valid or $\overline{CS}$ Low to $\overline{READ}$ Low	50		50		
TAW	ADR Valid to $\overline{WRITE}$ High Setup Time	200		130		
TCW	$\overline{CS}$ Low to $\overline{WRITE}$ High Setup Time	200	–	130	–	
TDW	Data Valid to $\overline{WRITE}$ High Setup Time	200		130		
TRA	ADR or $\overline{CS}$ Hold from $\overline{READ}$ High	0		0		
TRDE	Data Access from $\overline{READ}$ Low [1]	–	200	–	140	
TRDF	DB Float Delay from $\overline{READ}$ High	20	100	0	70	ns
TRSTD	Power Supply High to RESET Low Setup Time	500		500		
TRSTS	RESET to First $\overline{IOWR}$	2 TCY		2 TCY		
TRSTW	RESET Pulse Width	300		300		
TRW	$\overline{READ}$ Width	300	–	200	–	
TWA	ADR from $\overline{WRITE}$ High Hold Time	20		20		
TWC	$\overline{CS}$ High from $\overline{WRITE}$ High Hold Time	20		20		
TWD	Data from $\overline{WRITE}$ High Hold Time	30		30		
TWWS	$\overline{WRITE}$ Width	200		160		

1) Output loading is 1 TTL gate plus 150 pF capacitance, unless otherwise noted.

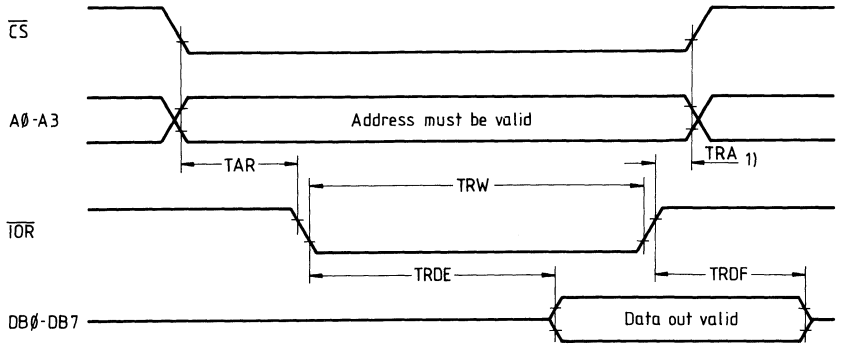
Input Waveforms for AC-Tests



Slave Mode Write Timing

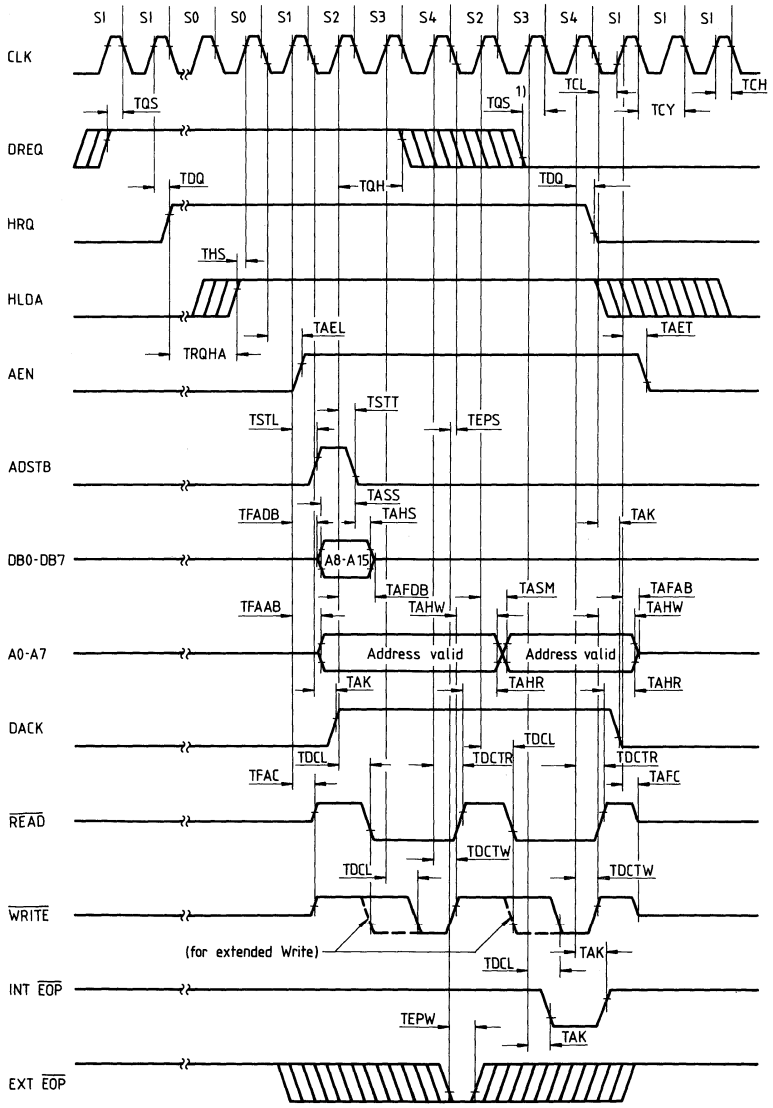


Slave Mode Read Timing



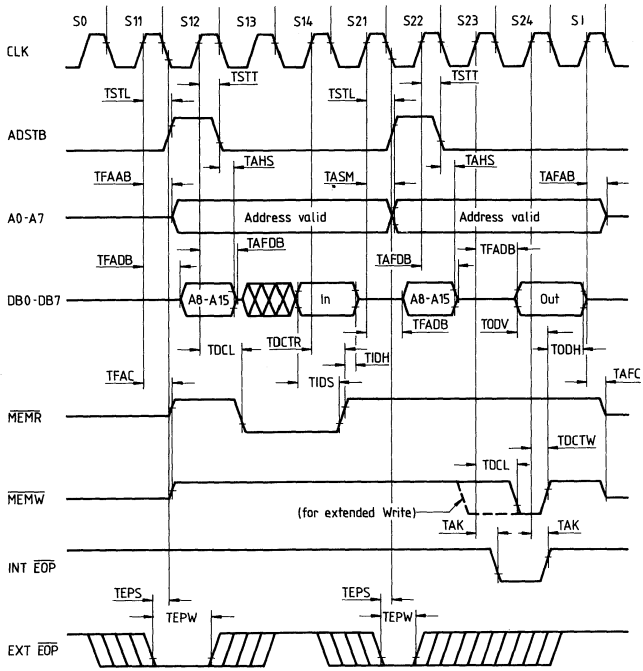
1) Successive read and/or write operation by the CPU to program or examine the controller must be timed to allow at least 600 ns for the SAB 8237A and at least 400 ns for the SAB 8237A-5, as recovery time between active read or write pulses.

DMA Transfer Timing

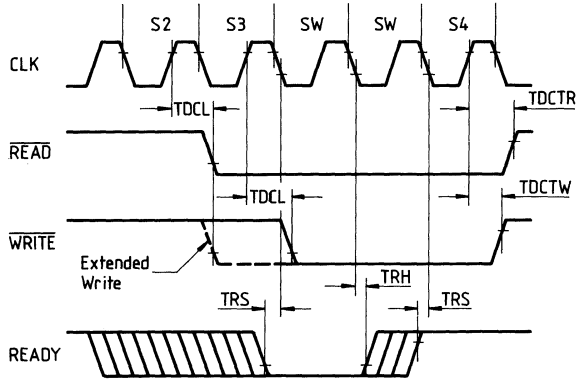


1) DREQ should be held active until DACK is returned.

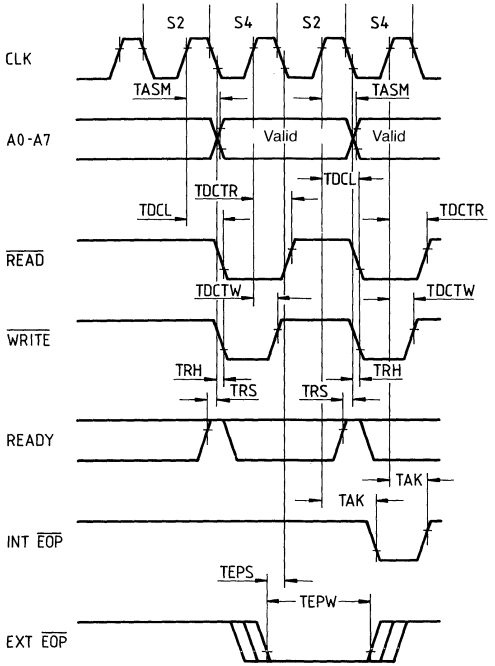
Memory-to-Memory Transfer Timing



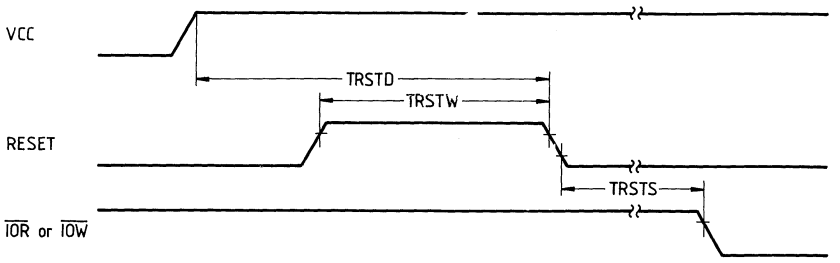
Ready Timing



Compressed Transfer Timing

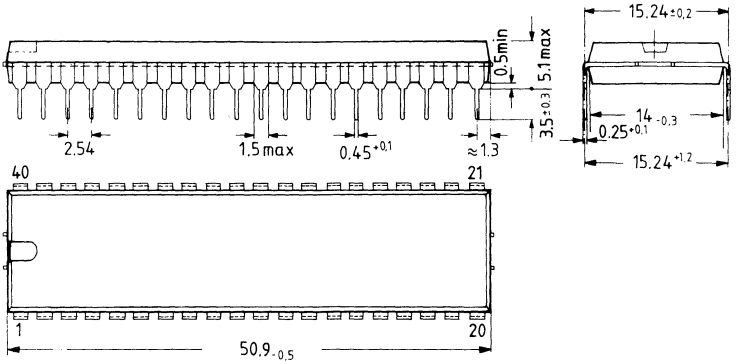


Reset Timing



Package Outline

40 Pin Plastic Package-Type P



Ordering Information

Type	Description	Ordering code
SAB 8237A-P	Programmable DMA Controller 3 MHz (Plastic)	Q 67120–Y49
SAB 8237A-5-P	Programmable DMA Controller 5 MHz (Plastic)	Q 67120–Y72

Preliminary

SAB 82C37A-5/82C37A-8 High-Performance CMOS Programmable DMA Controller

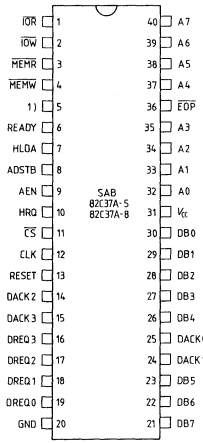
SAB 82C37A-5 5 MHz

- Four independent DMA channels
- Enable/disable control of individual DMA requests
- Memory-to-memory transfers
- Memory block initialization
- Address increment or decrement
- Independent autoinitialization of all channels
- High performance: transfers up to 2.6 Mbytes/s with 8 MHz SAB 82C37A-8

SAB 82C37A-8 8 MHz

- Directly expandable to any number of channels
- End of process input for terminating transfers
- Software DMA requests
- Independent polarity control for DREQ and DACK signals
- Fully static design
- Low standby power dissipation
- Compatible with the industry standard NMOS 9517A/8237A

Pin Configuration



1) Pin always tied high

Pin Names

DB7-DB0	Data Bus (bidirectional)
$\overline{IOR}$, $\overline{IOW}$	I/O Read and Write Input/Output
$\overline{MEMR}$, $\overline{MEMW}$	Memory Read and Write Output
A0-A3	Address Input/Output
A4-A7	Adress Output
$\overline{CS}$	Chip Select Input
CLK	Clock Input
READY	Ready Input
HRQ	Hold Request Output
$\overline{HLDA}$	Hold Acknowledge Input
RESET	Reset Input
DREQ0-DREQ3	DMA Request Input
DACK0-DACK3	DMA Acknowledge Output
AEN	Address Enable Output
ADSTB	Address Strobe Output
$\overline{EOP}$	End of Process Input/Output

The SAB 82C37A Multimode Direct Memory Access (DMA) Controller is designed to improve system performance by allowing external devices to directly transfer information to or from system memory. Memory-to-memory transfer capability is also provided.
The SAB 82C37A contains four independent channels, each with a separate register set, and may be expanded to any number of channels by cascading additional controller chips. The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to autoinitialize to its original state following an end-of-process ($\overline{EOP}$). Each channel has a full 64K address and word count capability.
The SAB 82C37A is fabricated in Siemens ACMOS technology and packaged in a 40-pin DIP. The SAB 82C37A-8 is the 8 MHz version of the 5 MHz SAB 82C37A-5. The SAB 82C37A is compatible with the industry standard 8237A/9517A DMA controllers.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{IOR}$	1	I/O	$\overline{I/O\ READ}$ I/O read is a bidirectional active-low tristate line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the active cycle, it is an output control signal used by the SAB 82C37A to access data from a peripheral device during a DMA write transfer.
$\overline{IOW}$	2	I/O	$\overline{I/O\ WRITE}$ I/O write is a bidirectional active-low tristate line. In the idle cycle it is an input control signal used by the CPU to load information into the SAB 82C37A. In the active cycle it is an output control signal used by the SAB 82C37A to load data to a peripheral device during a DMA read transfer. Write operations by the CPU to the SAB 82C37A require a rising $\overline{IOW}$ edge following each data byte transfer. It is not sufficient to hold the $\overline{IOW}$ pin low and toggle $\overline{CS}$.
$\overline{MEMR}$	3	O	$\overline{MEMORY\ READ}$ The memory read signal is an active-low tristate output used to access data from the selected memory location during a memory-to-peripheral or a memory-to-memory transfer.
$\overline{MEMW}$	4	O	$\overline{MEMORY\ WRITE}$ The memory write signal is an active-low tristate output used to write data to the selected memory location during a peripheral-to-memory or a memory-to-memory transfer.
–	5	I	Pin 5 must be tied high.
READY	6	I	READY READY is an input used to extend the memory read and write pulses from the SAB 82C37A to accommodate slow memories or I/O peripheral devices. READY must not make transitions during its specified setup/hold time.
HLDA	7	I	HOLD ACKNOWLEDGE The active-high hold acknowledge from the CPU indicates that control of the system buses has been relinquished.
ADSTB	8	O	ADDRESS STROBE The active-high address strobe is used to strobe the upper address byte from DB0-DB7 into an external latch.
AEN	9	O	ADDRESS ENABLE Address enable is an active-high signal used to disable the system bus during DMA cycles and to enable the output of the external latch which holds the upper byte of the address. Note that during DMA transfers HLDA and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed as programmed I/O during the DMA operation. The SAB 82C37A automatically deselects itself by disabling the $\overline{CS}$ input during DMA transfers.

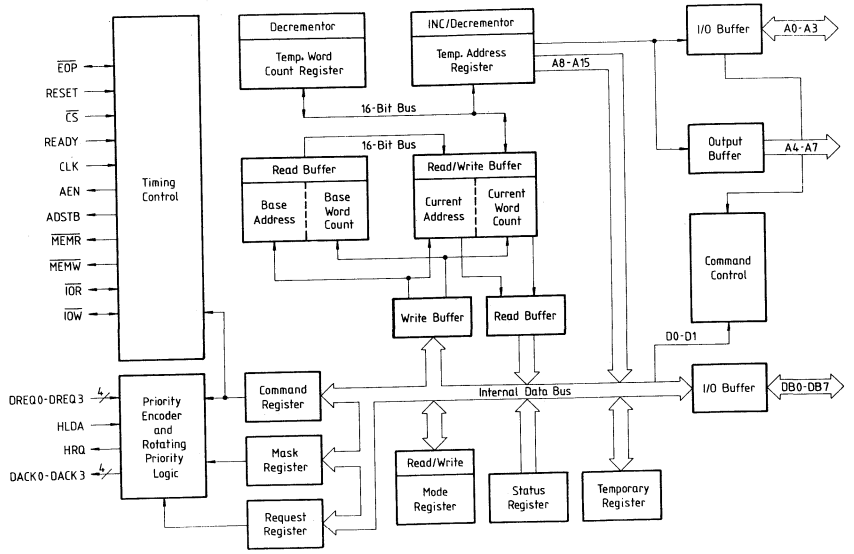
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
HRQ	10	O	HOLD REQUEST The hold request to the CPU is used by the DMA to request control of the system bus. Software requests or unmasked DREQs cause the SAB 82C37A to issue HRQ.
$\overline{CS}$	11	I	$\overline{CHIP\ SELECT}$ Chip select is an active-low input used to select the SAB 82C37A as an I/O device during an I/O read or I/O write by the host CPU. This allows CPU communication on the data bus. During multiple transfers to or from the SAB 82C37A by the host CPU $\overline{CS}$ may be held low providing $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer.
CLK	12	I	CLOCK This input controls the internal operations of the SAB 82C37A and its rate of data transfers. The input may be driven at up to 5 MHZ for the standard SAB 82C37A-5 and up to 8 MHz for the SAB 82C37A-8.
RESET	13	I	RESET Reset is an asynchronous active-high input which clears the command, status, request and temporary register. It also clears the first/last flipflop and sets the mask register. Following a reset, the device is in the idle cycle.
DACK0 DACK1 DACK2 DACK3	25 24 14 15	O O O O	DMA ACKNOWLEDGE The DMA acknowledge lines indicate that a channel is active. In many systems they will be used to select a peripheral. Only one DACK will be active at a time and none will be active unless the DMA is in control of the bus. The polarity of these lines is programmable. Reset initializes them to active-low.
DREQ0 DREQ1 DREQ2 DREQ3	19 18 17 16	I I I I	DMA REQUEST The DMA request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed priority, DREQ0 has the highest priority and and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of a DREQ signal. The polarity of DREQ is programmable. Reset initializes these lines to active high.
DB0-DB7	30-26, 23-21	I/O	DATA BUS The data bus lines are bidirectional tristate signals connected to the system data bus. The outputs are enabled during the I/O read by the host CPU, permitting the CPU to examine the contents of an address register, the status register, the temporary register or a word count register. The data bus is enabled to input data during a host CPU I/O write, allowing the CPU to program the SAB 82C37A control registers. During DMA cycles the most significant eight bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the source memory location comes into the SAB 82C37A's temporary register on the read-from-memory half of the operation. On the write-to-memory half of the operation, the data bus outputs the temporary register data into the destination memory location.

Pin Functions and Definitions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
A0–A3	32–35	I/O	ADDRESS 0–3 The four least significant address lines are bidirectional tristate signals. During DMA idle cycles they are inputs and allow the host CPU to load or read control registers. When the DMA is active, they are outputs and provide the lower 4 bits of the output address.
A4–A7	37–40	O	ADDRESS 4–7 The four most significant address lines are tristate outputs and provide four bits of address. These lines are enabled only during DMA service.
$\overline{EOP}$	36	I/O	$\overline{END\ OF\ PROCESS}$ End of process ($\overline{EOP}$) is an active-low bidirectional open-drain signal providing information concerning the completion of DMA service. When a channel's word count goes to zero, the SAB 82C37A pulses $\overline{EOP}$ low to provide the peripheral with a completion signal. $\overline{EOP}$ may also be pulled low by the peripheral to cause premature completion. The reception of $\overline{EOP}$, either internal or external, causes the currently active channel to terminate the service, to set its TC bit in the status register and to reset its request bit. If autoinitialization is selected for the channel, the current registers will be updated from the base registers. Otherwise the channel's mask bit will be set and the register contents will remain unaltered. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ always applies to the channel with an active DACK; external $\overline{EOP}$s are disregarded when DACK0-DACK3 are all inactive if the DMA is in state SI. In situations where two or more SAB 82C37A DMA controllers are cascaded, the $\overline{EOP}$ pins should be logically ORed (not wire-ORed). Because $\overline{EOP}$ is an open-drain signal, an external pullup resistor is required. Values of 3.3 kΩ or 4.7 kΩ are recommended.
V_{CC}	31	–	POWER SUPPLY (+5 V)
GND	20	–	GROUND (0 V)

Block Diagram



Functional Description

DMA Operation
The SAB 82C37A is designed to operate in two major cycles. These are called idle and active cycles. Each device cycle is made up of a number of states. State I (SI) is the inactive state. It is entered when the SAB 82C37A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the program condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The SAB 82C37A has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the CPU will signal that transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted before S4 by the use of the READY line on the SAB 82C37A.
Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for each complete transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23 and S24) for the write-to-memory half of the transfer.

Idle Cycle
When no channel is requesting service, the SAB 82C37A will enter the idle cycle and perform "SI" states. In this cycle the SAB 82C37A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the SAB 82C37A.

Active Cycle
When the SAB 82C37A is in the idle cycle and a channel requests a DMA service, the device will output a HRQ to the microprocessor and enter the active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode – In single transfer mode, the SAB 82C37A will make a one-byte transfer during each HRQ/HLDA handshake. When DREQ goes active, HRQ will go active. After the CPU responds by driving HRQ active, a one-byte transfer will take place. Following the transfer, HRQ will go inactive, the word count will be decremented and the address will be either incremented or decremented.

Block Transfer Mode – In block transfer mode, the SAB 82C37A will continue making transfers until a TC (caused by the word count going to zero) or an external end-of-process ($\overline{EOP}$) is encountered.

Demand Transfer Mode – In demand transfer mode the device will continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus, the device requesting service may discontinue transfers by bringing DREQ inactive. Service may be resumed by asserting an active DREQ once again.

Cascade Mode – This mode is used to cascade more than one SAB 82C37A together for simple system expansion. The HRQ and HLDA signals from the additional SAB 82C37A are connected to the DREQ and DACK signals of a channel of the initial SAB 82C37A.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are read, write and verify. Write transfers move data from an I/O device to the memory by activating $\overline{IOR}$ and $\overline{MEMW}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers; the SAB82C37A operates as in read or write transfers generating addresses, responding to $\overline{EOP}$, etc., however, the memory and I/O control lines remain inactive.

Memory-to-Memory – The SAB 82C37A includes a block move capability that allows blocks of data to be moved from one memory adress space to another. Channel 0 forms the source address and channel 1 forms the destination address. The channel 1 word count is used. A memory-to-memory transfer is initiated by setting a software DMA request for channel 0.

Autoinitialize – By programming a bit in the mode register a channel may be set up for an autoinitialize operation. During autoinitialization, the original values of the current address and current word count registers are automatically restored from the base address and base word count registers of that channel following $\overline{EOP}$.

Extended Write – For flyby transactions late write is normally used, as this allows sufficient time for the $\overline{IOR}$ signal to get data from the peripheral onto the bus before $\overline{MEMW}$ is activated. In some systems, performance can be improved by starting the write cycle earlier.

Address Generation – In order to reduce pin count, the SAB 82C37A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of address strobe (ADSTB) is used to load these bits from the data lines to the latch. Address enable (AEN) is used to enable the bits onto the address bus through the tristate enable control signal of the latch. The lower order address bits are output by the SAB 82C37A directly. To save time and speed transfers, the SAB 82C37A executes S1 states only when updating of A8–A15 in the latch is necessary.

Compressed Timing – In order to achieve even greater throughput where system characteristics permit, the SAB 82C37A can compress the transfer time to two clock cycles. By removing state S3 the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write.

Priority – The SAB 82C37A has two types of priority encoding available as software selectable options. The first is fixed priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel 0. The second scheme is rotating priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.

Software Commands
There are two special software commands which can be executed in the program condition.
Clear first/last flipflop: This command may be issued prior to writing or reading SAB 82C37A address or word count information. This initializes the flipflop to a known state so that subsequent accesses to register contents by the microprocessor will address lower and upper bytes in the correct sequence.
Master clear: This software instruction has the same effect as the hardware reset. The command, status, request, temporary and internal first/last flipflop registers are cleared and the mask register is set.

Register Description

Current Address Register
Each channel has a 16-bit current address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the current address register during the transfer.

Current Word Count Register
Each channel has a 16-bit current word count register. This register should be programmed with, and will return on a CPU read, a value one less than the number of words to be transferred. The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes to zero, a TC will be generated.

Base Address and Base Word Count Registers
Each channel has a pair of base address and base word count registers. These 16-bit registers store the original values of their associated current registers. During autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in bytes during DMA programming by the microprocessor.

Command Register
This 8-bit register controls the operation of the SAB 82C37A. It is programmed by the microprocessor in the program condition and is cleared by reset.

Mode Registers
Each channel has a 6-bit mode register associated with it. When the register is being written to by the microprocessor in the program condition, bits 0 and 1 determine which channel mode register is to be written to.

Request Register
The SAB 82C37A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit request register. These are nonmaskable and subject to prioritization by the priority encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external $\overline{\text{EOP}}$. The entire register is cleared by a reset.

Mask Register
Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{\text{EOP}}$ if the channel is not programmed for autoinitialize. Each bit of the 4-bit mask register may also be set or cleared separately under software control. The entire register is also set by a reset.

Status Register
The status registers may be read out of the SAB 82C37A by the microprocessor. It indicates which channels have reached a terminal count and which channels have pending DMA requests.

Temporary Register
The temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the program condition.

Absolute Maximum Ratings

Ambient temperature under bias	0° to 70°C
Storage temperature	−65° to + 150°C
Supply voltage	−0.5 to + 7.0 V
Voltage on any pin with respect to ground	−0.5 to V_{CC} + 0.5 V
Power dissipation	1 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} − 0.4	– –	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{IL}	Input leakage current	–	±1	µA	0 V < V_{IN} < V_{CC}
I_{OFL}	Output leakage current	–	±10	µA	0 V < V_{OUT} < V_{CC}
I_{CC}	V_{CC} supply current	–	2	mA/MHz	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open
I_{CCSB}	V_{CC} supply current – standby	–	10	µA	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open CLK = 0 MHz

Capacitance [1)]

T_A = 25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	f_c = 1 MHz
C_{IO}	I/O capacitance	–	20	pF	Unmeasured pins returned to GND
C_{OUT}	Output capacitance	–	15	pF	

[1)] This parameter is periodically sampled and not 100% tested.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; GND = 0 V

DMA (Master) Mode

Symbol	Parameter	Limit values				Unit
		82C37A-5		82C37A-8		
		min.	max.	min.	max.	
t_{AEL}	AEN high from CLK low (S1) delay time	–	200	–	105	ns
t_{AET}	AEN low from CLK high (S1) delay time	–	130	–	80	ns
t_{AFAB}	Address active to float delay from CLK high	–	90	–	55	ns
t_{AFC}	$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ float from CLK high	–	120	–	75	ns
t_{AFDB}	DB active to float delay from CLK high	–	120	–	80	ns
t_{AHR}	Address from $\overline{\text{READ}}$ high hold time	t_{CY}–100	–	t_{CY}–75	–	ns
t_{AHS}	DB from ADSTB low hold time	30	–	25	–	ns
t_{AHW}	Address from $\overline{\text{WRITE}}$ high hold time	t_{CY}–50	–	t_{CY}–50	–	ns
t_{AK}	DACK valid from CLK low delay time [1]	–	170	–	105	ns
	$\overline{\text{EOP}}$ high from CLK high delay time [2]	–	170	–	105	ns
	$\overline{\text{EOP}}$ low to CLK high delay time	–	170	–	60	ns
t_{ASM}	Address stable from CLK high	–	120	–	60	ns
t_{ASS}	DB to ADSTB low setup time	100	–	65	ns	ns
t_{CH}	CLK high time (transitions ≤ 10 ns)	80	–	55	–	ns
t_{CL}	CLK low time (transitions ≤ 10 ns)	68	–	43	–	ns
t_{CY}	CLK cycle time	200	–	125	–	ns
t_{DCL}	CLK high to $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ low delay [3]	–	190	–	120	ns
t_{DCTR}	$\overline{\text{READ}}$ high from CLK high (S4) delay time[3]	–	190	–	115	ns
t_{DCTW}	$\overline{\text{WRITE}}$ high from CLK high (S4) delay time[3]	–	130	–	80	ns
t_{DQ}	HRQ valid from CLK high delay time	–	120	–	75	ns
t_{EPS}	$\overline{\text{EOP}}$ low from CLK low setup time	40	–	25	–	ns
t_{EPW}	$\overline{\text{EOP}}$ pulse width	220	–	135	–	ns
t_{FAAB}	Address float to active delay from CLK high	–	120	–	60	ns
t_{FAC}	$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ active from CLK high	–	150	–	90	ns
t_{FADB}	DB float to active delay from CLK high	–	120	–	60	ns

Notes see next page.

Symbol	Parameter	Limit values				Unit
		82C37A-5		82C37A-8		
		min.	max.	min.	max.	
t_{HS}	HLDA valid to CLK high setup time	75	–	45	–	ns
t_{IDH}	Input data from $\overline{MEMR}$ high hold time	0	–	0	–	ns
t_{IDS}	Input data to $\overline{MEMR}$ high setup time	170	–	90	–	ns
t_{ODH}	Output data from $\overline{MEMW}$ high hold time	10	–	10	–	ns
t_{ODV}	Output data valid to $\overline{MEMW}$ high [4]	125	–	90	–	ns
t_{QS}	DREQ to CLK low (S1, S4) setup time [1]	0	–	0	–	ns
t_{RH}	CLK to READY low hold time	20	–	20	–	ns
t_{RS}	READY to CLK low setup time	60	–	35	–	ns
t_{STL}	ADSTB high from CLK high delay time	–	130	–	70	ns
t_{CLSL}	ADSTB low from CLK low delay time	–	150	–	70	ns
t_{SHSL}	ADSTB high time	70	–	50	–	ns
t_{QH}	DREQ from DACK valid hold time	0	–	0	–	ns
t_{RQHA}	HRQ to HLDA delay time	1	–	1	–	CLK

[1] DREQ and DACK signals may be active high or low. Timing diagrams assume the active high mode.

[2] $\overline{EOP}$ is an open-drain output. This parameter assumes the presence of a 1.6 kΩ pullup to V_{CC}.

[3] The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be t_{CY}–100 ns and for extended write will be $2t_{CY}$–100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be $2t_{CY}$–50 ns and for compressed read will be t_{CY}–50 ns.

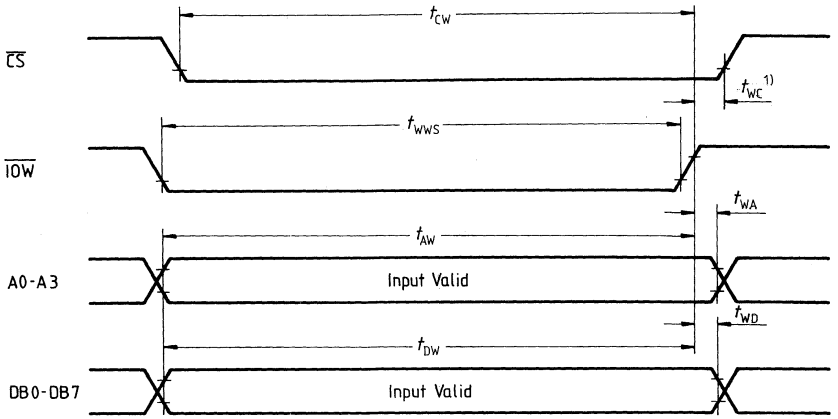
[4] If n wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by n (t_{CY}).

Peripheral (Slave) Mode

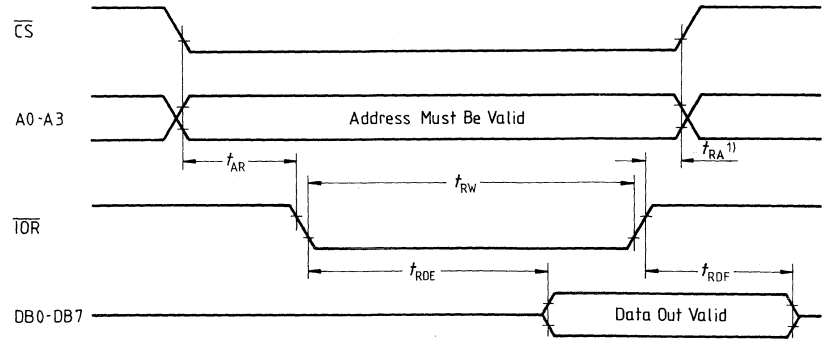
Symbol	Parameter	Limit values				Unit
		82C37A-5		82C37A-8		
		min.	max.	min.	max.	
t_{AR}	Address valid or $\overline{CS}$ low to $\overline{READ}$ low	50	–	10	–	ns
t_{AW}	Address valid to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{CW}	$\overline{CS}$ low to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{DW}	Data valid to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{RA}	Address or $\overline{CS}$ hold from $\overline{READ}$ high	0	–	0	–	ns
t_{RDE}	Data access from $\overline{READ}$ low [1]	–	140	–	120	ns
t_{RDF}	DB float delay from $\overline{READ}$ high	0	70	0	55	ns
t_{RSTD}	Power supply high to RESET low setup time	500	–	500	–	µs
t_{RSTS}	RESET to first $\overline{IOWR}$	2 t_{CY}	–	2 t_{CY}	–	ns
t_{RSTW}	RESET pulse width	300	–	300	–	ns
t_{RW}	$\overline{READ}$ width	200	–	155	–	ns
t_{WA}	Address from $\overline{WRITE}$ high hold time	0	–	0	–	ns
t_{WC}	$\overline{CS}$ high from $\overline{WRITE}$ high hold time	0	–	0	–	ns
t_{WD}	Data from $\overline{WRITE}$ high hold time	30	–	10	–	ns
t_{WWS}	$\overline{WRITE}$ width	160	–	100	–	ns

[1] Output loading is 1 TTL gate plus 150 pF capacitance, unless otherwise noted.

Slave Mode Write Timing

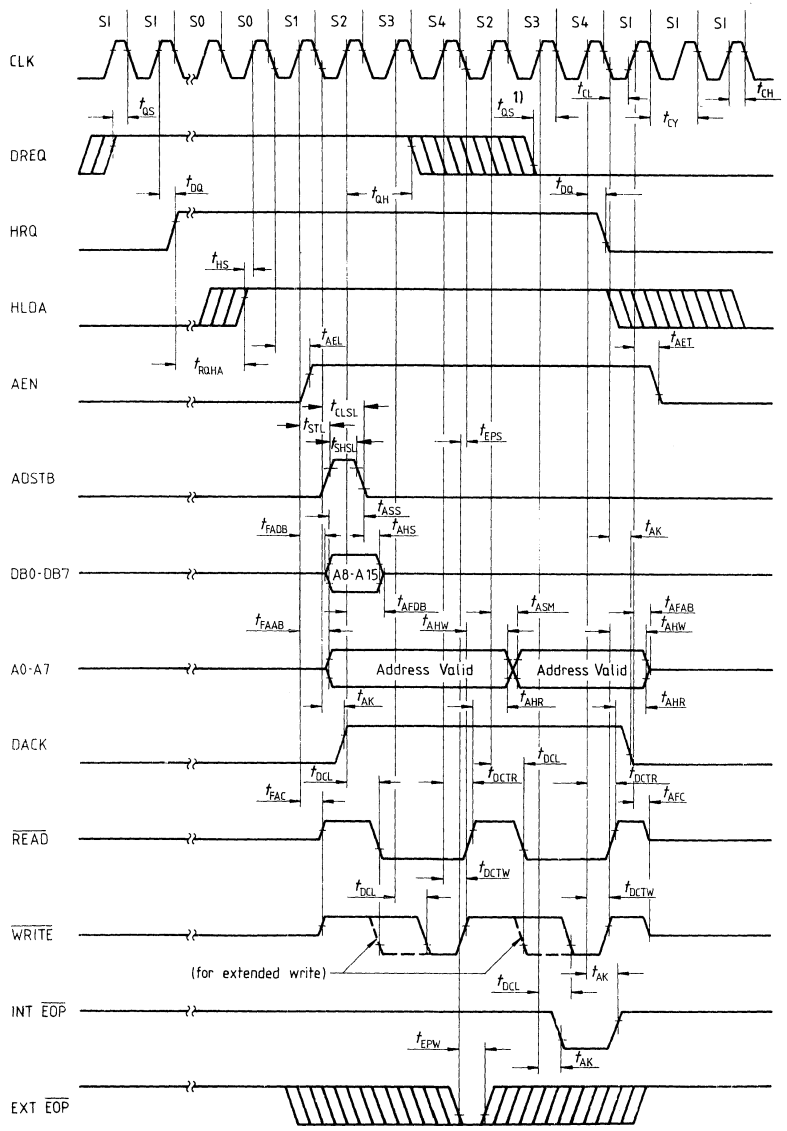


Slave Mode Read Timing



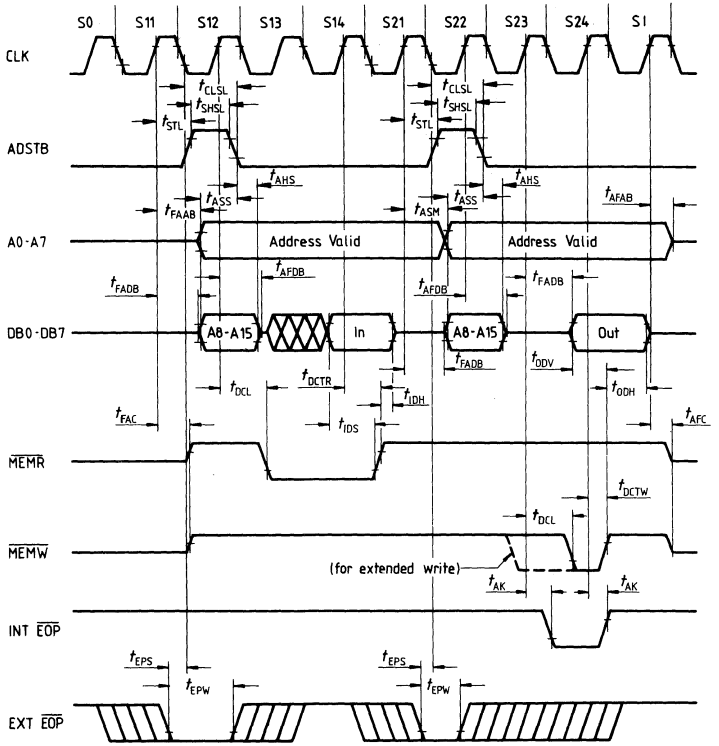
1) Successive read and/or write operation by the CPU to access the SAB 82C37A registers must meet recovery times:
   400 ns at least for the SAB 82C37A-5
   300 ns at least for the SAB 82C37A-8

DMA Transfer Timing

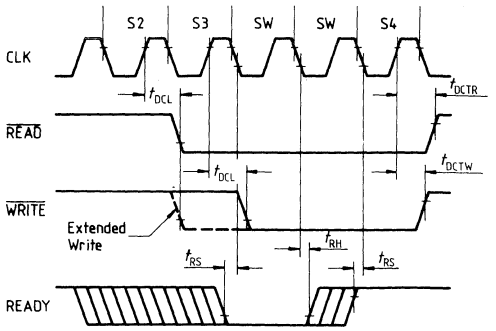


1) DREQ should be held active until DACK is returned.

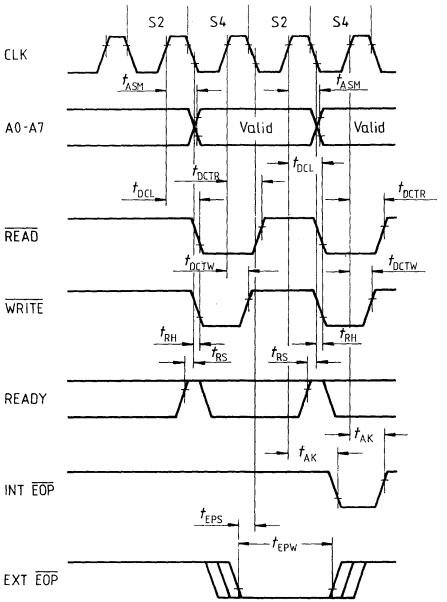
Memory-to-Memory Transfer Timing



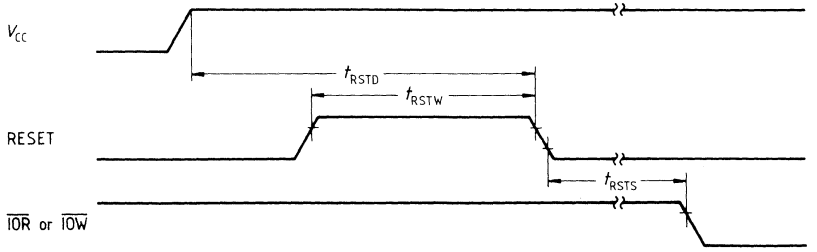
Ready Timing



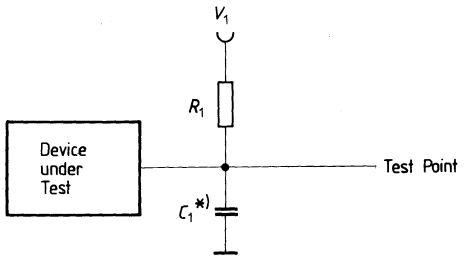
Compressed Transfer Timing



Reset Timing



AC Test Circuits

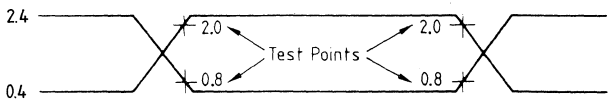


*) Includes stray and jig capacitance

Test Condition Definition

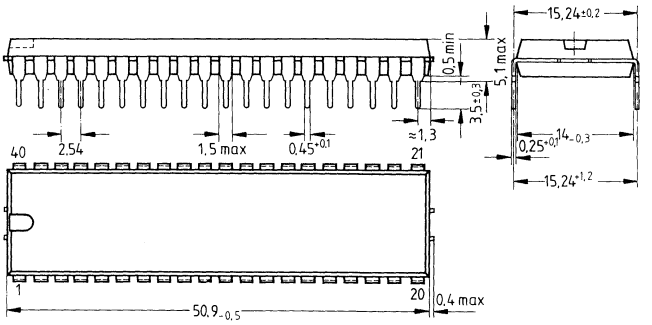
Pins	V_1	R_1	C_1
All Outputs Except $\overline{EOP}$	1.7 V	520 Ω	100 pF
$\overline{EOP}$	V_{CC}	1.6 KΩ	50 pF

Input Waveforms for AC Tests



Package Outlines

Plastic Package, P-DIP-40



Dimensions in mm

Ordering Information

Type	Ordering code	Description
SAB 82C37A-5-P	Q 67120-P215	Programmable DMA controller 5 MHz (P-DIP-40)
SAB 82C37A-8-P	Q 67120-P239	Programmable DMA controller 8 MHz (P-DIP-40)

Preliminary

SAB 82C37B-5/82C37B-8 High-Performance CMOS Programmable DMA Controller

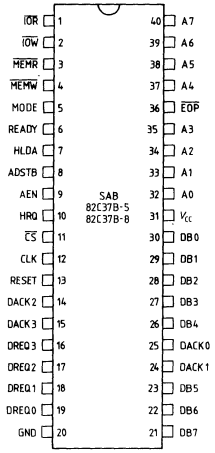
SAB 82C37B-5 5 MHz

- Fully upward-compatible to SAB 82C37A (CMOS) and SAB 8237A (NMOS)
- Two basic operating modes
  Normal mode: 16-bit registers
  Superset mode: 24-bit registers
- Supports 24-bit address and count valves
- Four independent DMA channels
- Address increment or decrement by 1 or 2 (byte or word transfers)

SAB 82C37B-8 8 MHz

- High performance: transfers up to 8 Mbytes/s with 8 MHz SAB 82C37B-8
- Directly expandable to any number of channels
- Independent polarity control for DREQ and DACK signals
- Fully static design
- Low standby power dissipation

Pin Configuration



Pin Names

DB7-DB0	Data Bus (bidirectional)
$\overline{IOR}$, $\overline{IOW}$	I/O Read and Write Input/Output
$\overline{MEMR}$, $\overline{MEMW}$	Memory Read and Write Output
A0-A3	Address Input/Output
A4-A7	Adress Output
$\overline{CS}$	Chip Select Input
CLK	Clock Input
READY	Ready Input
HRQ	Hold Request Output
$\overline{HLDA}$	Hold Acknowledge Input
RESET	Reset Input
DREQ0-DREQ3	DMA Request Inputs
DACK0-DACK3	DMA Acknowledge Outputs
AEN	Address Enable Output
ADSTB	Address Strobe Output
$\overline{EOP}$	End of Process Input/Output
MODE	Mode Select Input

The SAB 82C37B Multimode Direct Memory Access (DMA) Controller improves the system performance by allowing external devices to directly transfer information to or from system memory. A memory-to-memory transfer capability is also provided. The SAB 82C37B may operate in two modes. The normal mode provides direct compatibility to the industry standard 8237A/9517A DMA controllers. In the superset mode, the SAB 82C37B contains 24-bit wide address and count registers for each channel.
The four independent channels with their own register set may be cascaded by additional DMA controller chips.
The SAB 82C37B is fabricated in Siemens ACMOS technology and packaged in a 40-pin DIP. The SAB 82C37B-8 is the 8 MHz version of the 5 MHz SAB 82C37B-5.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{IOR}$	1	I/O	$\overline{I/O\ READ}$ I/O read is a bidirectional active-low tristate line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the active cycle, it is an output control signal used by the SAB 82C37A to access data from a peripheral device during a DMA write transfer.
$\overline{IOW}$	2	I/O	$\overline{I/O\ WRITE}$ I/O write is a bidirectional active-low tristate line. In the idle cycle it is an input control signal used by the CPU to load information into the SAB 82C37B. In the active cycle it is an output control signal used by the SAB 82C37B to load data to a peripheral device during a DMA read transfer. Write operations by the CPU to the SAB 82C37B require a rising $\overline{IOW}$ edge following each data byte transfer. It is not sufficient to hold the $\overline{IOW}$ pin low and toggle $\overline{CS}$.
$\overline{MEMR}$	3	0	$\overline{MEMORY\ READ}$ The memory read signal is an active-low tristate output used to access data from the selected memory location during a memory-to-peripheral or a memory-to-memory transfer.
$\overline{MEMW}$	4	0	$\overline{MEMORY\ WRITE}$ The memory write signal is an active-low tristate output used to write data to the selected memory location during a peripheral-to-memory or a memory-to-memory transfer.
MODE	5	I	MODE MODE selects the SAB 82C37B operating mode. If MODE = high, normal mode with 16-bit address and count registers is selected. MODE = low selects the superset mode with 24-bit address and count registers and word transfer capability. MODE is a strapping pin and must not be changed dynamically during controller operation.
READY	6	I	READY READY is an input used to extend the memory read and write pulses from the SAB 82C37B to accommodate slow memories or I/O peripheral devices. READY must not make transitions during its specified setup/hold time and is ignored in verify transfer mode.
HLDA	7	I	HOLD ACKNOWLEDGE The active-high hold acknowledge from the CPU indicates that control of the system buses has been relinquished.
ADSTB	8	O	ADDRESS STROBE The active-high address strobe is used to strobe the addresses A8-A15 at DB0-DB7 into an external latch. In the superset mode (MODE = low), ADSTB is also used to strobe A16 to A23 at A0-A7 into an external latch. During block operations, ADSTB will only be issued when the upper addresses A8-A23 must be updated, thus speeding operation by eliminating S1 states.

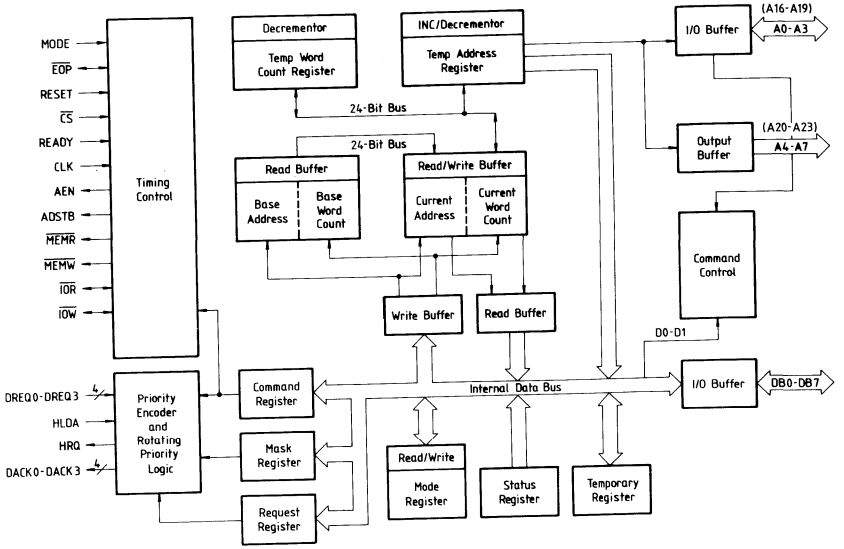
Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
AEN	9	O	ADDRESS ENABLE Address enable is an active-high signal used to disable the system bus during DMA cycles and to enable the output of the external latch which holds the upper byte of the address. Note that during DMA transfers HLDA and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed as programmed I/O during the DMA operation. The SAB 82C37B automatically deselects itself by disabling the $\overline{CS}$ input during DMA transfers.
HRQ	10	O	HOLD REQUEST The hold request to the CPU is used by the DMA to request control of the system bus. Software requests or unmasked DREQs cause the SAB 82C37B to issue HRQ.
$\overline{CS}$	11	I	$\overline{CHIP\ SELECT}$ Chip select is an active-low input used to select the SAB 82C37B as an I/O device during an I/O read or I/O write by the host CPU. This allows CPU communication on the data bus. During multiple transfers to or from the SAB 82C37B by the host CPU $\overline{CS}$ may be held low providing $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer.
CLK	12	I	CLOCK This input controls the internal operations of the SAB 82C37B and its rate of data transfers. The input may be driven from DC up to 5 MHz for the SAB 82C37B-5 and up to 8 MHz for the SAB 82C37B-8. The clock may be stopped any time for standby operation, even in the middle of a bus operation.
RESET	13	I	RESET Reset is an asynchronous active-high input which clears the command, status, request and temporary register. It also clears the first/last flipflop (normal mode) or the byte pointer counter (superset mode) and sets the mask register. Following a reset the device is performing idle cycles.
DACK0 DACK1 DACK2 DACK3	25 24 14 15	O O O O	DMA ACKNOWLEDGE The DMA acknowledge lines indicate that a channel is active. In many systems they will be used to select a peripheral. Only one DACK will be active at a time and none will be active unless the DMA is in control of the bus. The polarity of these lines is programmable. Reset initializes them to active-low.
DREQ0 DREQ1 DREQ2 DREQ3	19 18 17 16	I I I I	DMA REQUEST The DMA request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of a DREQ signal. The polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ will not be recognized while the clock is stopped. Unused DREQ inputs should be pulled high or low (inactive) and the corresponding mask bit should be set.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
DB0-DB7	30-26, 23-21	I/O	DATA BUS The data bus lines are bidirectional tristate signals connected to the system data bus. The outputs are enabled during the I/O read by the host CPU, permitting the CPU to examine the contents of a register. The data bus is enabled to input data during a host CPU I/O write, allowing the CPU to program the SAB 82C37B control registers. During DMA cycles the addresses A8-A15 are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the source memory location comes into the SAB 82C37B's temporary register on the read-from-memory half of the operation. On the write-to-memory half of the operation, the data bus outputs the temporary register data into the destination memory location.
A0–A3	32–35	I/O	ADDRESS 0–3 The four least significant address lines are bidirectional tristate signals. During DMA idle cycles they are inputs and allow the host CPU to load or read control registers. When the DMA is active, they are outputs and provide the A0-A3 output addresses, and in the superset mode A16 to A19.
A4–A7	37–40	O	ADDRESS 4–7 The four most significant address lines are tristate outputs and provide A4-A7 addresses. In the superset mode A20-A23 are available at these lines during S1 states. These lines are enabled only during the DMA service.
$\overline{EOP}$	36	I/O	END OF PROCESS End of process ($\overline{EOP}$) is an active-low bidirectional signal. Information concerning the completion of DMA services. is available at the bidirectional $\overline{EOP}$ pin. The SAB 82C37B allows an external signal to terminate an active DMA service by pulling the $\overline{EOP}$ pin low. A pulse is generated by the SAB 82C37B when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. The $\overline{EOP}$ pin is driven by an open-drain transistor on-chip, and requires an external pullup resistor. When an $\overline{EOP}$ pulse occurs, whether internally or externally generated, the SAB 82C37B will terminate the service, and if autoinitialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for autoinitialize. In that case, the mask bit remains clear.
V_{CC}	31	–	POWER SUPPLY (+5 V)
GND	20	–	GROUND (0 V)

Block Diagram



Functional Description

The SAB 82C37B direct memory access controller is designed to improve the data transfer rate in systems which must transfer data from an I/O device to memory, or move a block memory to an I/O device. It will also perform memory-to-memory block moves, or fill a block of memory with data from a single location. Operating modes are provided to handle single byte transfers as well as discontinuous data streams.
The DMA controller is a state-driven address and control signal generator, which permits data to be transferred directly from an I/O device to memory or vice versa without ever being stored in a temporary register. This can greatly increase the data transfer rate for sequential operations, compared with processor move or repeated string instructions. Memory-to-memory operations require temporary internal storage of the data byte between generation of the source and destination addresses, so memory-to-memory transfers take place at less than half the rate I/O operations, but still much faster than with central processor techniques.

DMA Operation

In a system, the SAB 82C37B address and control outputs and data bus pins are basically connected in parallel with the systems buses. External latches are required for the upper address lines. While inactive, the controller's outputs are in a high-impedance state. When activated by a DMA request and bus control is relinquished by the host, the SAB 82C37B drives the buses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the command, mode, address, and word count registers.

Once initiated, a block DMA transfer will proceed as the controller outputs the data address, simultaneous $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$ pulses, and selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte is transferred, the address is automatically incremented (or decremented) and the word count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the word count register underflows, or an external $\overline{\text{EOP}}$ is applied.

The DMA controller operates in two major cycles, active and idle. After being programmed, the controller is normally idle until a DMA request occurs on an unmasked channel, or a software request is given. The SAB 82C37B will then request control of the system buses and enter the active cycle.

The SAB 82C37B can assume seven separate states, each composed of one full clock period. State I (SI) is the idle state. It is entered when the SAB 82C37B has no valid DMA requests pending, at the end of a transfer sequence, or when a reset or master clear has occurred. While in SI, the DMA controller is inactive but may be in the program condition (being programmed by the processor).

State 0 (S0) is the first state of a DMA service. The SAB 82C37B has requested a hold but the processor has not yet returned an acknowledge. The SAB 82C37B may still be programmed until it has received HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the ready line on the SAB 82C37B.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two-digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14 are used for the read-from-memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

Idle Cycle

When no channel is requesting service, the SAB 82C37B will enter the idle cycle and perform "SI" states. In this cycle, the SAB 82C37B samples the DREQ lines on the falling edge of every clock cycle to determine if any channel is requesting a DMA service.

Note that for standby operation where the clock has been stopped, DMA requests will be ignored. The device will respond to $\overline{\text{CS}}$ (chip select), in case of an attempt by the microprocessor to write or read the internal registers of the SAB 82C37B. When $\overline{\text{CS}}$ is low and HLDA is low, the SAB 82C37B enters the program condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers.

Active Cycle

When the SAB 82C37B is in the idle cycle, and a software request or an unmasked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode – In single transfer mode, the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a terminal count bit in the status register is set, an $\overline{EOP}$ pulse is generated, and the channel will autoinitialize if this option has been selected. If not programmed to autoinitialize, the mask bit will be set, along with the TC bit and $\overline{EOP}$ pulse.

DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed, unless a higher priority channel takes over.

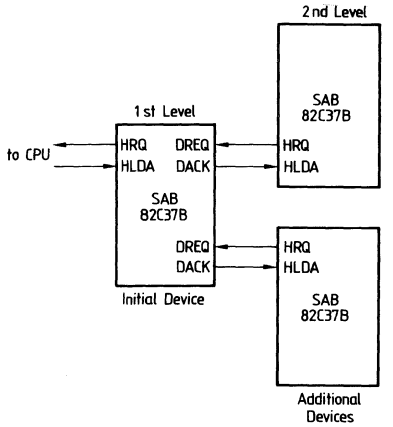
Block Transfer Mode – In block transfer mode, the device is activated by DREQ or software request and continues making transfers during the service until a TC, caused by word count going to FFFFH, or an external end-of-process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again, an autoinitialization will occur at the end of the service if the channel has been programmed for that option.

Demand Transfer Mode – In demand transfer mode the device continues making transfers until a TC or external $\overline{EOP}$ is encountered, or until DREQ goes inactive. Thus, transfers may continue until the I/O device has exhausted its data capacitiy. Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an $\overline{EOP}$ can cause an autoinitialization at the end of the service. $\overline{EOP}$ is generated either by TC or by an external signal.

Cascade Mode – This mode is used to cascade more than one SAB 82C37B for simple system expansion. The HRQ and HLDA signals from the additional SAB 82C37B are connected to the DREQ and DACK signals respectively of a channel for the initial SAB 82C37B. This allows the DMA request of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests.

The following figure shows two additional devices cascaded with an initial device using two of the previous channels.

Cascaded SAB 82C37B Devices



When programming cascaded controllers, start with the first level (closest to the microprocessor). After reset, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. Also, the initial device's mask bits function normally on cascaded channels, so they may be used to inhibit second-level services.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are read, write and verify. Write transfers move data from an I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$.

Verify transfers are pseudo-transfers. The SAB 82C37B operates as in read or write transfers generating addresses and responding to $\overline{EOP}$, etc., however the memory and I/O control lines all remain inactive. Verify mode is not permitted for memory-to-memory operation. Ready is ignored during verify transfers.

Autoinitialize – By programming a bit in the mode register, a channel may be set up as an autoinitialize channel. During autoinitialization, the original values of the current address and current word count registers are automatically restored from the base address and base word count registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in autoinitialize. Following autoinitialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or software request is made.

Memory-to-Memory – To perform block moves of data from one memory address space to another with minimum of program effort and time, the SAB 82C37B includes a memory-to-memory transfer feature. Programming a bit in the command register selects channels 0 and 1 to operate as memory-to-memory transfer channels.

The transfer is initiated by setting the software or hardware DREQ for channel 0. The SAB 82C37B requests a DMA service in the normal manner. After HLDA is true, the device, using four-state transfers in block transfer mode, reads data from the memory. The channel 0 current address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the SAB 82C37B internal temporary register. Another four-state transfer moves the data to memory using the address in channel one's current address register and incrementing or decrementing it in the normal manner. The channel 1 current word count is decremented.

When the word count of channel 1 goes to FFFFH, a TC is generated causing an $\overline{EOP}$ output terminating the service. Channel 0 word count decrementing to FFFFH will not set the channel 0 TC bit in the status register or generate an $\overline{EOP}$ in this mode. It will cause an autoinitialization of channel 0, if that option has been selected.

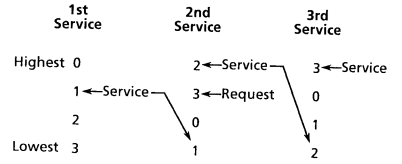
If full autoinitialization for a memory-to-memory operation is desired, the channel 0 and channel 1 word counts must be set equal before the transfer begins.

In memory-to-memory mode, channel 0 may be programmed to retain the same address for all transfers. This allows a single byte to be written to a block of memory. This channel 0 address hold feature is selected by bit 1 in the command register.

Priority – The SAB 82C37B has two types of priority encoding available as software selectable options. The first is fixed priority which fixes the channels in priority order based upon the descending value of their numbers. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interferring with the service until it is completed.

The second scheme is rotating priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. The next lower channel from the channel serviced has highest priority on the following request: Priority rotates every time control of the system buses is returned to the processor.

Rotating Priority



Compressed Timing – In order to achieve even greater throughput where system characteristics permit, the SAB 82C37B can compress the transfer time to two clock cycles. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. $\overline{EOP}$ will be output in S2 if compressed timing is selected. Compressed timing is not allowed for memory-to-memory transfers.

Basic Operating Modes – The SAB 82C37B may work in two basic operating modes: the normal mode and the superset mode. In the normal mode, the SAB 82C37B is compatible with its NMOS SAB 8237A predecessor and provides 16-bit wide address and count registers. In the superset mode address and count registers have a width of 24 bits. In this mode the SAB 82C37B directly supports the full addressing capabilities of the SAB 8086/8088, SAB 80186/80188 and SAB 80286 microprocessor families.

Two additional features ara available in the superset mode. The address increment/decrement of the address registers can be programmed to be one or two. So byte or word transfers may be selected during a DMA operation. Furthermore, the incrementing/decrementing of the address bits A16–A23 may be disabled. In this case, addresses will wrap around within a 64K page and A16–A23 work like a page register.

Thus with the capabilities of the superset mode, external page registers are no longer required for each DMA channel to get a DMA address greater than 16 bits. Instead of external page registers, the SAB 82C37B in superset mode generates the upper address information A16–A23 for DMA cycles needing one external address latch, which may be used by each DMA channel.

The two basic operating modes are selected by the MODE pin. If MODE is tied to V_{CC}, normal mode is selected. The superset mode is selected by connecting the MODE pin to GND. MODE must not be changed dynamically during controller operation.

Address Generation – In order to reduce pin count, the SAB 82C37B multiplexes addresses on data lines and address lines. State S1 is used to output the higher address bits to external address latches. A8–A15 are output at the data bus lines DB0–7. In superset mode additionally A16–A23 appear at the address lines A0–A7. The falling edge of the address strobe (ADSTB) is used to strobe this information into latches. AEN (address enable) is used to enable these latches to drive the address bus. The lower address bits are output by the SAB 82C37B directly (for more details see timing diagrams).

During block and demand transfer mode service, which includes multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the SAB 82C37B executes S1 states only when an updating of A8–A23 in the latch is necessary.

Programming

The SAB 82C37B will accept programming from the host processor anytime that HLDA is inactive, and at least one rising clock edge has occurred after HLDA went low. It is the responsibility of the host processor to assure that programming and HLDA are mutually exclusive.

Note that a problem can occur if a DMA request occurs on an unmasked channel while the SAB 82C37B is being programmed.

Such problems can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming any of its registers. Once the programming is complete, the controller can be enabled/unmasked.

Due to the number and size of the internal registers, an internal flipflop (normal mode) or a modulo-3 register pointer (superset mode) are used to generate internally additional address bits for register addressing. This flipflop or byte counter determines which byte of the 16/24-bit address and word count registers is accessed. Flipflop and byte counter are reset through RESET or by software.

Register Description

Current Address Register

Each channel has a 16/24-bit current address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the values of the address are stored in the current address register during the transfer. This register is written or read by the microprocessor in successive bytes. It may also be reinitialized by an autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{EOP}$.

Current Word Count Register

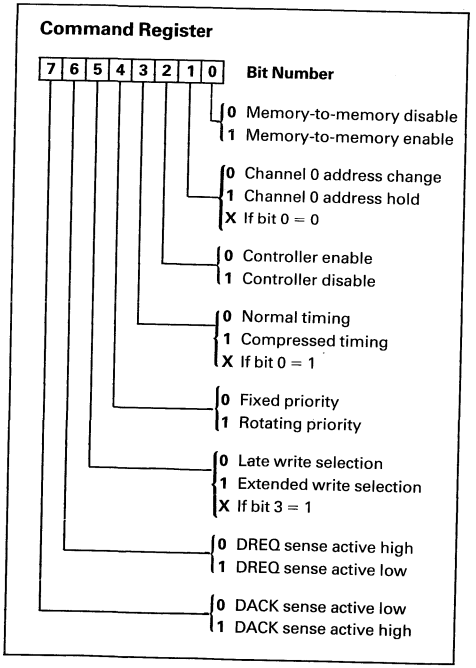
Each channel has a 16/24-bit current word count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the current word count register (i.e. programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. When the value in the register goes from 0 to (FF)FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the program condition. Following the end of a DMA service it may also be reinitialized by an autoinitialization back to its original value. Autoinitialization can occur only when an $\overline{EOP}$ occurs. If it is not autoinitialized, this register will have a count of (FF)FFFFH after TC.

Base Address and Base Word Count Registers

Each channel has a pair of base address and base word count registers. These 16/24-bit registers store the original value of their associated current registers. During autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in bytes in the program condition by the microprocessor. These registers cannot be read by the microprocessor.

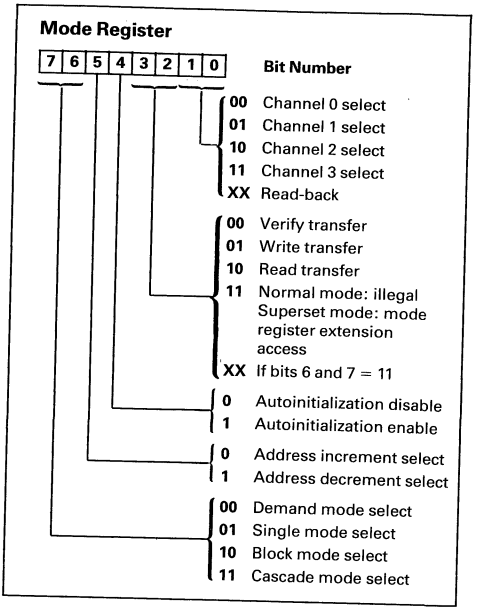
Command Register

This 8-bit register controls the operation of the SAB 82C37B. It is programmed by the microprocessor and is cleared by reset or a master clear instruction.

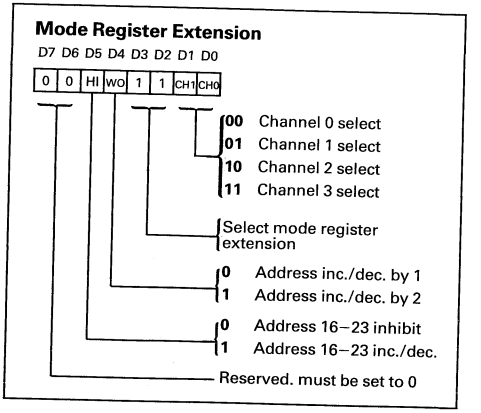


Mode Register

Each channel has a 6-bit mode register associated with it. When the register is being written to by the microprocessor in the program condition, bits 0 and 1 determine which channel mode register is to be written to.



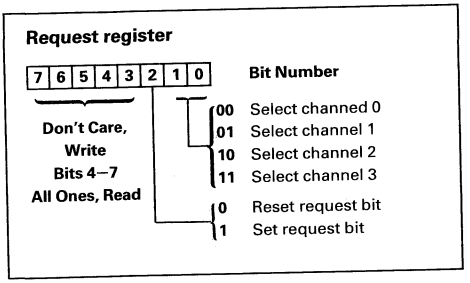
If the bits 2 and 3 of the mode register are set during writing, the mode register extension register will be accessed (only in superset mode!). In normal mode, no mode register extension is available. The mode register extension is used to program the special features of the SAB 82C37B superset mode.



When the processor reads back the mode register, bits 2 to 7 contain the information which was written into the mode register bits 2 to 7. Bit 0 contains the value of W0 of the mode register extension and bit 1 shows the value of HI. In normal mode the value of these two bits is undefined.

Request Register

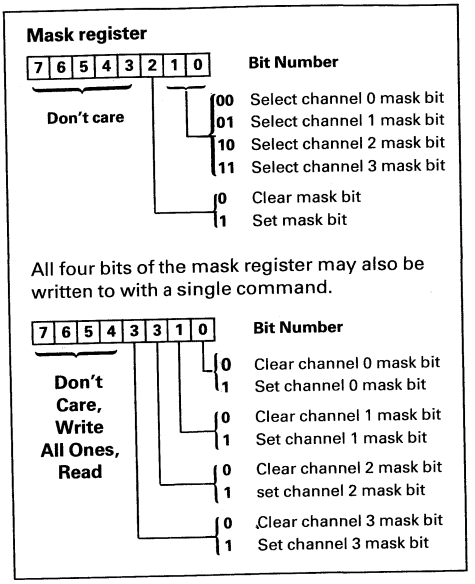
The SAB 82C37B can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit request register. These are non-maskable and subject to prioritization by the priority encoder network. Each register bit is set or reset separately under software control. The entire register is cleared by a reset. A software request for DMA operation can be made in block or single modes. For memory-to-memory transfers, the software request for channel 0 should be set. When reading the request register, bits 4–7 will always read as ones, and bits 0–3 will display the request bits of channels 0–3 respectively.



Mask Register

Each channel has associated with it a mask bit which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed to autoinitialize. Each bit of the 4-bit mask register may also be set or cleared separately or simultaneously under software control. The entire register is also set by a reset or master clear.

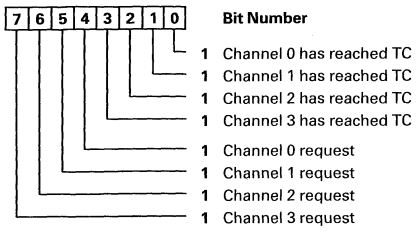
When reading the mask register, bits 4–7 will always read as logical ones, and bits 0–3 will display the mask bits of channel 0–3, respectively. The 4 bits of the mask register may be cleared simultaneously by using the clear mask register command (see software commands section).



Status Register

The status register contains information about the status of the SAB 82C37B. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0–3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. Status bits are cleared upon reset, master clear, and on each status read. Bits 4–7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the status register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user-defined service priority.

Status Register



Temporary Register
The temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor. The temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a reset or master clear.

Software Commands
There are special software commands which can be executed by reading or writing to the SAB 82C37B. These commands do not depend on the specific data pattern on the data bus, but are activated by the I/O operation itself. On read-type commands, the data value is not guaranteed. These commands are:

Clear Register Pointer – This command is executed prior to writing or reading a new address or word count information to the SAB 82C37B. In normal mode, this command initializes a byte pointer flipflop to 0 so that subsequent accesses to register contents start by addressing the low byte first. In the superset mode, the modulo-3 register pointer is reset by this command. Thus the following first byte access to address or count registers starts with the lowest byte. The next byte will be the middle byte followed by the highest byte of the 24-bit registers. After this the lowest byte will be addressed again with the next access.

Set Register Pointer – In normal mode, this command will set the register pointer flipflop to select the high byte first on read or write operations to address and count registers. In the superset mode, this command sets the byte pointer to the medium byte. The byte addressed next will be the highest byte.

Master Clear – This software instruction has the same effect as the hardware reset. The command, status, request, and temporary registers, and internal byte pointer and mode register counter are cleared and the mask register is set. The SAB 82C37B will enter the idle cycle.

Software Command Codes and Register Codes

Operation	A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Mask Bit	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set Byte Pointer Flipflop	1	1	0	0	0	1
Clear Byte Pointer Flipflop	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
Clear Mode Register Counter	1	1	1	0	0	1
Clear Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

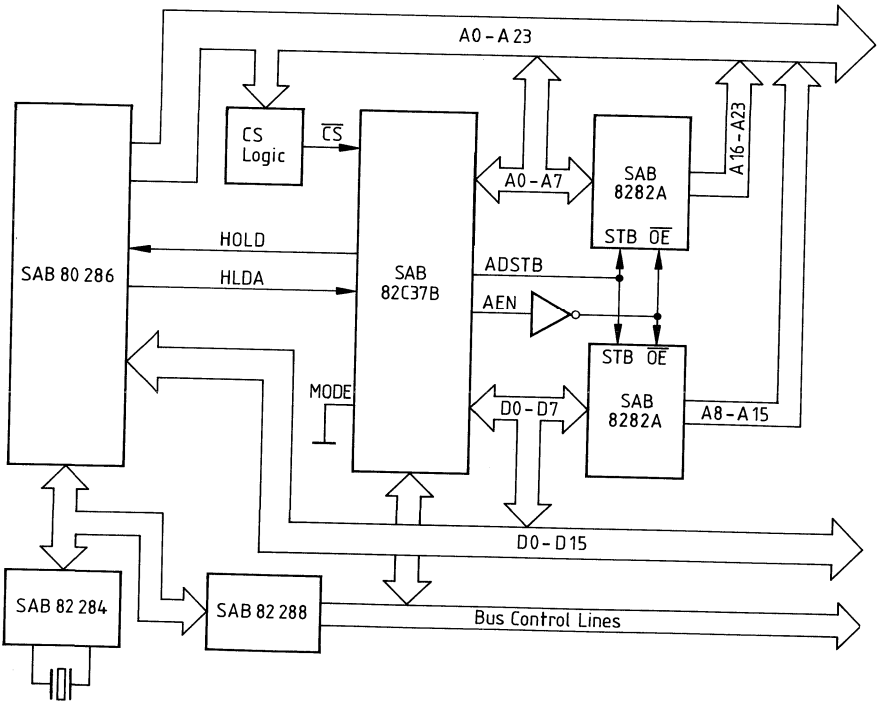
Clear Mask Register – This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Clear Mode Register Counter – Since only one address location is available for reading the mode registers, an internal two-bit counter has been included to select mode registers during read operations. To read the mode registers, first execute the clear mode register counter command, then do consecutive reads until the desired channel is read. Read order is channel 0 first, channel 3 last.

External EOP Operation

The $\overline{EOP}$ pin is a bidirectional, open-drain pin which may be driven by external signals to terminate DMA operation. It is important to note that the SAB 82C37B will not accept external $\overline{EOP}$ signals when it is an SI (idle) state. The controller must be active to latch EXT $\overline{EOP}$. Once latched, the EXT $\overline{EOP}$ will be acted upon during the next S2 state, unless the SAB 82C37B enters an idle state first. In the latter case, the latched $\overline{EOP}$ is cleared. External $\overline{EOP}$ pulses occurring between active DMA transfers in demand mode will not be recognized, since the SAB 82C37B is in an SI state.

Typical SAB 80286/82C37B System Configuration



Absolute Maximum Ratings

Ambient temperature under bias	0° to 70°C
Storage temperature	−65° to + 150°C
Supply voltage	−0.5 to + 7.0 V
Voltage on any pin with respect to ground	−0.5 to V_{CC} + 0.5 V
Power dissipation	1 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} − 0.4	– –	V V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{IL}	Input load current	–	±1	µA	0 V < V_{IN} < V_{CC}
I_{OFL}	Output leakage current	–	±10	µA	0 V < V_{OUT} < V_{CC}
I_{CC}	V_{CC} supply current	–	2	mA/MHz	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open
I_{CCSB}	V_{CC} supply current – standby	–	10	µA	V_{CC} = 5.5 V V_{IN} = V_{CC} or GND Outputs open CLK = 0 MHz

Capacitance [1)]

T_A = 25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	f_c = 1 MHz
C_{IO}	I/O capacitance	–	20	pF	Unmeasured pins returned to GND
C_{OUT}	Output capacitance	–	15	pF	

[1)] This parameter is periodically sampled and not 100% tested.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ± 10%; GND = 0 V

DMA (Master) Mode

Symbol	Parameter	Limit values				Unit
		82C37B-5		82C37B-8		
		min.	max.	min.	max.	
t_{AEL}	AEN high from CLK low (S1) delay time	–	200	–	105	ns
t_{AET}	AEN low from CLK high (S1) delay time	–	130	–	80	ns
t_{AFAB}	Address active to float delay from CLK high	–	90	–	55	ns
t_{AFC}	$\overline{READ}$ or $\overline{WRITE}$ float from CLK high	–	120	–	75	ns
t_{AFDB}	DB/Address active to float delay from CLK high	–	120	–	80	ns
t_{AHR}	Address from $\overline{READ}$ high hold time	t_{CY}–100	–	t_{CY}–75	–	ns
t_{AHS}	DB from ADSTB low hold time	30	–	25	–	ns
t_{AHW}	Address from $\overline{WRITE}$ high hold time	t_{CY}–50	–	t_{CY}–50	–	ns
t_{AK}	DACK valid from CLK low delay time [1]	–	170	–	105	ns
	$\overline{EOP}$ high from CLK high delay time [2]	–	170	–	105	ns
	$\overline{EOP}$ low to CLK high delay time	–	170	–	60	ns
t_{ASM}	Address stable from CLK high	–	120	–	60	ns
t_{ASS}	DB to ADSTB low setup time	100	–	65	–	ns
t_{CH}	CLK high time (transitions ≤ 10 ns)	80	–	55	–	ns
t_{CL}	CLK low time (transitions ≤ 10 ns)	68	–	43	–	ns
t_{CY}	CLK cycle time	200	–	125	–	ns
t_{DCL}	CLK high to $\overline{READ}$ or $\overline{WRITE}$ low delay [3]	–	190	–	120	ns
t_{DCTR}	$\overline{READ}$ high from CLK high (S4) delay time [3]	–	190	–	115	ns
t_{DCTW}	$\overline{WRITE}$ high from CLK high (S4) delay time [3]	–	130	–	80	ns
t_{DQ}	HRQ valid from CLK high delay time	–	120	–	75	ns
t_{EPS}	$\overline{EOP}$ low from CLK low setup time	40	–	25	–	ns
t_{EPW}	$\overline{EOP}$ pulse width	220	–	135	–	ns
t_{FAAB}	Address float to active delay from CLK high	–	120	–	60	ns
t_{FAC}	$\overline{READ}$ or $\overline{WRITE}$ active from CLK high	–	150	–	90	ns
t_{FADB}	DB float to active delay from CLK high	–	120	–	60	ns

Notes see next page.

Symbol	Parameter	Limit values				Unit
		82C37B-5		82C37B-8		
		min.	max.	min.	max.	
t_{HS}	HLDA valid to CLK high setup time	75	–	45	–	ns
t_{IDH}	Input data from $\overline{MEMR}$ high hold time	0	–	0	–	ns
t_{IDS}	Input data to $\overline{MEMR}$ high setup time	170	–	90	–	ns
t_{ODH}	Output data from $\overline{MEMW}$ high hold time	10	–	10	–	ns
t_{ODV}	Output data valid to $\overline{MEMW}$ high [4]	125	–	90	–	ns
t_{QS}	DREQ to CLK low (S1, S4) setup time [1]	0	–	0	–	ns
t_{RH}	CLK to READY low hold time	20	–	20	–	ns
t_{RS}	READY to CLK low setup time	60	–	35	–	ns
t_{STL}	ADSTB high from CLK high delay time	–	130	–	70	ns
t_{CLSL}	ADSTB low from CLK low delay time	–	150	–	70	ns
t_{SHSL}	ADSTB high time	70	–	50	–	ns
t_{QH}	DREQ from DACK valid hold time	0	–	0	–	ns
t_{RQHA}	HRQ to HLDA delay time	1	–	1	–	CLK

[1] DREQ and DACK signals may be active high or low. Timing diagrams assume the active high mode.

[2] $\overline{EOP}$ is an open-collector output. This parameter assumes the presence of a 1.6 kΩ pullup to V_{CC}.

[3] The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be t_{CY}–100 ns and for extended write will be $2t_{CY}$–100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be $2t_{CY}$–50 ns and for compressed read will be t_{CY}–50 ns.

[4] If n wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by n (t_{CY}).

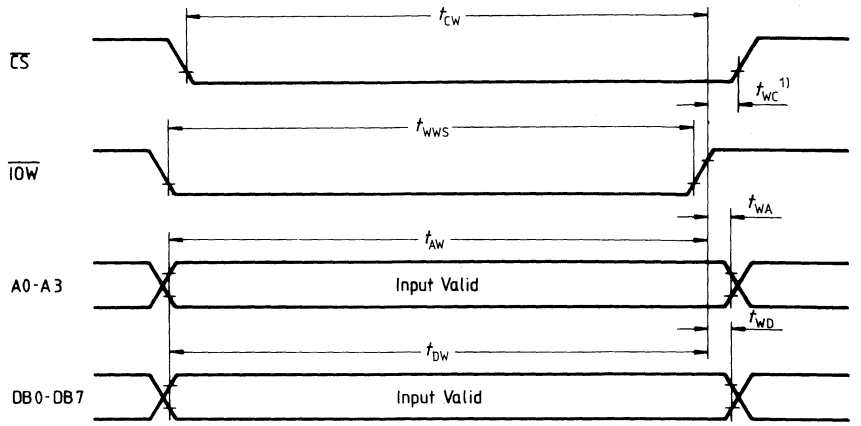
Peripheral (Slave) Mode

Symbol	Parameter	Limit values				Unit
		82C37B-5		82C37B-8		
		min.	max.	min.	max.	
t_{AR}	Address valid or $\overline{CS}$ low to $\overline{READ}$ low	50	–	10	–	ns
t_{AW}	Address valid to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{CW}	$\overline{CS}$ low to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{DW}	Data valid to $\overline{WRITE}$ high setup time	130	–	100	–	ns
t_{RA}	Address or $\overline{CS}$ hold from $\overline{READ}$ high	0	–	0	–	ns
t_{RDE}	Data access from $\overline{READ}$ low [1]	–	140	–	120	ns
t_{RDF}	DB float delay from $\overline{READ}$ high	0	70	0	55	ns
t_{RSTD}	Power supply high to RESET low setup time	500	–	500	–	µs
t_{RSTS}	RESET to first $\overline{IOWR}$	2 t_{CY}	–	2 t_{CY}	–	ns
t_{RSTW}	RESET pulse width	300	–	300	–	ns
t_{RW}	$\overline{READ}$ width	200	–	155	–	ns
t_{WA}	Address from $\overline{WRITE}$ high hold time	0	–	0	–	ns
t_{WC}	$\overline{CS}$ high from $\overline{WRITE}$ high hold time	0	–	0	–	ns
t_{WD}	Data from $\overline{WRITE}$ high hold time	30	–	10	–	ns
t_{WWS}	$\overline{WRITE}$ width	160	–	100	–	ns

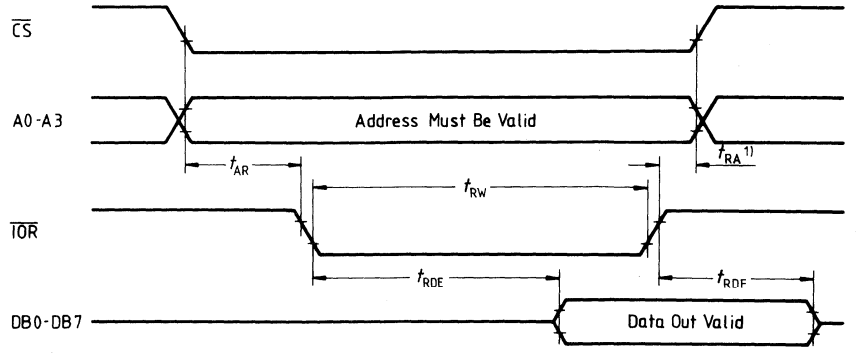
[1] Output loading is 1 TTL gate plus 150 pF capacitance, unless otherwise noted.

Waveforms

Slave Mode Write Timing

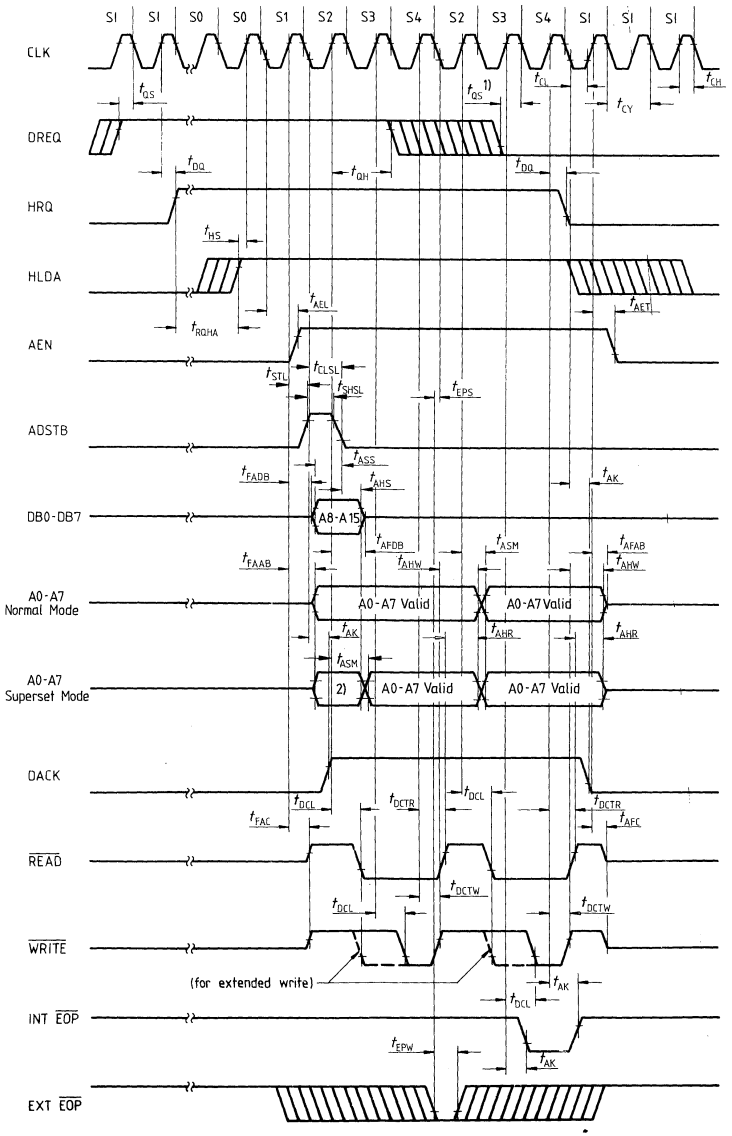


Slave Mode Read Timing



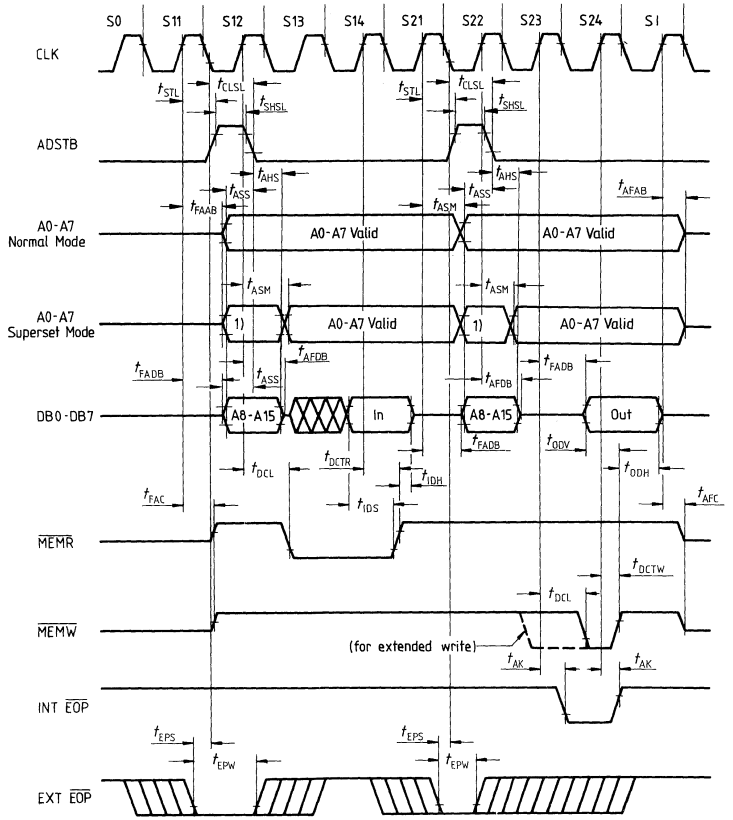
1) Successive read or write operations by the CPU to access the SAB 82C37B registers must meet recovery times:
   400 ns at least for the SAB 82C37B-5
   300 ns at least for the SAB 82C37B-8

DMA Transfer Timing



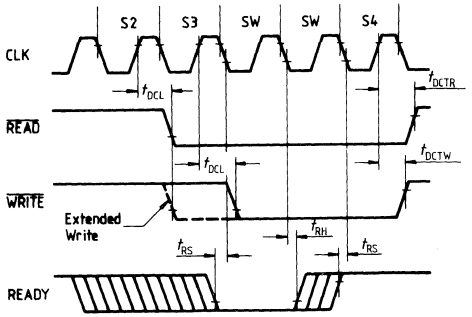
1) DREQ should be held active until DACK is returned.
2) A16-A23 valid

Memory-to-Memory Transfer Timing

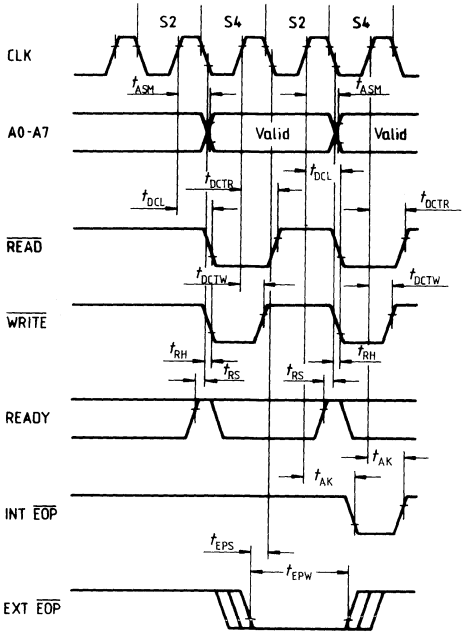


1) A16-A23 valid

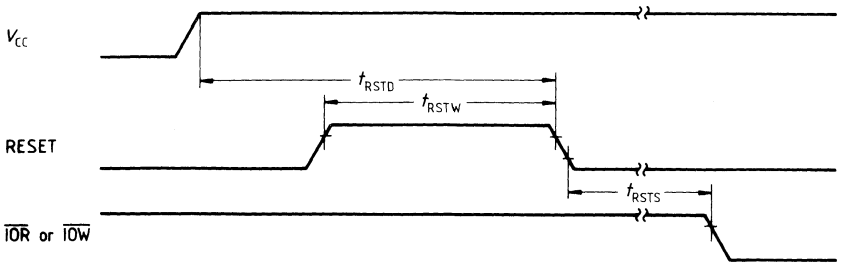
Ready Timing



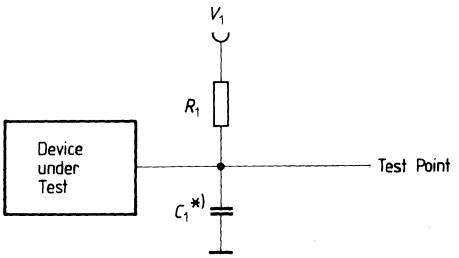
Compressed Transfer Timing



Reset Timing



AC Test Circuits

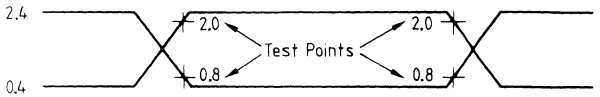


*) Includes stray and jig capacitance

Test Condition Definition

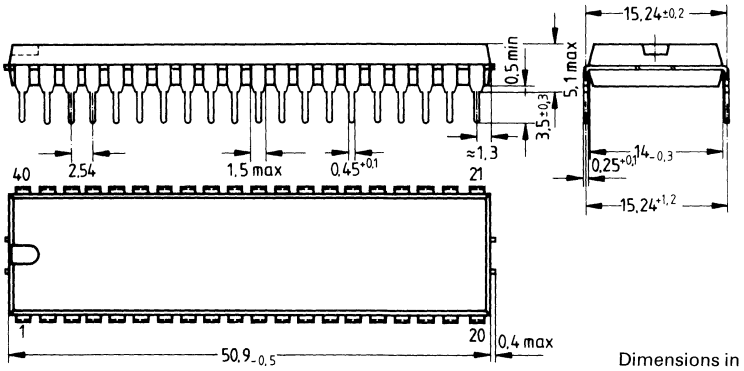
Pins	V_1	R_1	C_1
All Outputs Except $\overline{EOP}$	1.7 V	520 Ω	100 pF
$\overline{EOP}$	V_{CC}	1.6 KΩ	50 pF

Input Waveforms for AC Tests



Package Outlines

Plastic Package, P-DIP-40



Dimensions in mm

Ordering Information

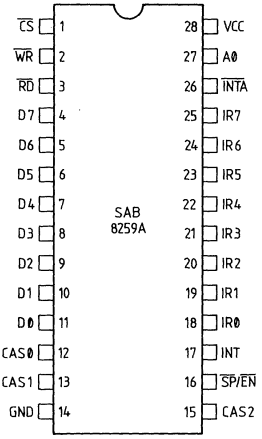
Type	Ordering code	Description
SAB 82C37B-5-P	Q 67120-P243	Programmable DMA controller 5 MHz (P-DIP-40)
SAB 82C37B-8-P	Q 67120-P244	Programmable DMA controller 8 MHz (P-DIP-40)

Preliminary

SAB 8259A, SAB 8259A-2 Programmable Interrupt Controller

- Compatible with SAB 8086/88, SAB 80186/188 and SAB 80286 processor families
- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Single +5 V supply (no clocks)
- 28-pin dual-in-line package

Pin Configuration



Pin Names

D7-D0	Data Bus (Bidirectional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0	Command Select Address
$\overline{CS}$	Chip Select
CAS2-CAS0	Cascade Lines
$\overline{SP}/\overline{EN}$	Slave Programm/Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0-IR7	Interrupt Request Inputs

The SAB 8259A programmable interrupt controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without requiring additional circuitry. The SAB 8259A is fabricated in +5 V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 28-pin DIP. The circuitry is static, requiring no clock input.

The SAB 8259A is designed to minimize the software and real-time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

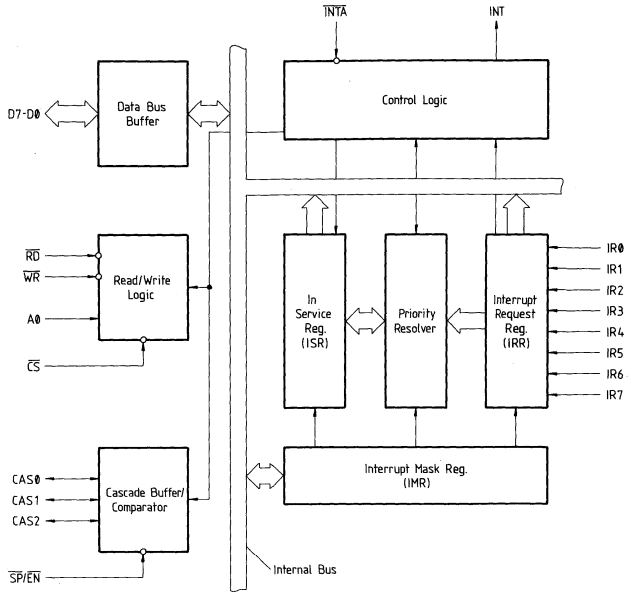
9.86

Pin Definitions and Functions

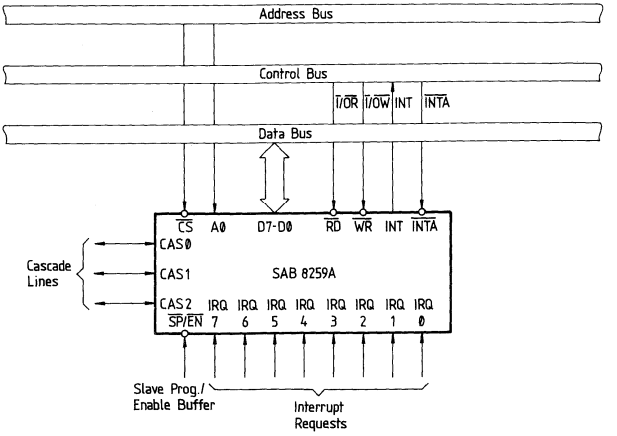
Symbol	Pin	Input (I) Output (O)	Function
$\overline{CS}$	1	I	CHIP SELECT A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the SAB 8259A. $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{WR}$	2	I	$\overline{WRITE}$ A low on this pin when $\overline{CS}$ is low, enables the SAB 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	$\overline{READ}$ A low on this pin when $\overline{CS}$ is low, enables the SAB 8259A to release status onto the data bus for the CPU.
D7-D0	4-11	I/O	BIDIRECTIONAL DATA BUS Control, status and interrupt vector information is transferred via this bus.
CAS0-CAS1	12, 13, 15	I/O	CASCADE LINES The CAS lines form a private SAB 8259A bus to control a multiple SAB 8259A structure. These pins are outputs for a master SAB 8259A and inputs for a slave SAB 8259A.
$\overline{SP}/\overline{EN}$	16	I/O	$\overline{SLAVE\ PROGRAM}/\overline{ENABLE\ BUFFER}$ This is a dual function pin. When in buffered mode it can be used as an output to control buffer transceivers (EN). When not in buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	INTERRUPT [1] This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR0-IR7	18-25	I	INTERRUPT REQUESTS Asynchronous inputs. An interrupt request can be generated by raising an IR input (low to high) and holding it high until it is acknowledged (edge triggered mode), or just by a high level on an IR input (level triggered mode).
$\overline{INTA}$	26	I	$\overline{INTERRUPT\ ACKNOWLEDGE}$ This pin is used to enable SAB 8259A interrupt-vector data onto the data bus. This is done by a sequence of interrupt acknowledge pulses issued by the CPU.
A0	27	I	A0 ADDRESS LINE This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. It is used by the SAB 8259A to destinguish between various command words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for SAB 8086/80186/80286).
VCC	28	I	POWER SUPPLY (+5V)
GND	14	I	GROUND (0V)

[1] An active low signal on $\overline{WR}$ during an INT high signal may force INT to low.

Functional Block Diagram



Interface to Standard System Bus



Functional Description

General

The SAB 8259A is a device specifically designed for use in real-time, interrupt-driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other SAB 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral.
A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the SAB 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during an $\overline{\text{INTA}}$ pulse.

Interrupt Mask Register (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The VOH level on this line is designed to be fully compatible with the SAB 8080A/8085A/8086/8088/80186/80188/80286.

$\overline{\text{INTA}}$ (Interrupt Acknowledge)

$\overline{\text{INTA}}$ pulses will cause the SAB 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the SAB 8259A.

Data Bus Buffer

This tristate, bidirectional 8-bit buffer is used to interface the SAB 8259A to the system data bus. Control words and status information are transferred through the data bus buffer.

Read/Write Control Logic

The function of this block is to accept output commands from CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the SAB 8259A to be transferred onto the data bus.

$\overline{\text{CS}}$ (Chip Select)

A low on this input enables the SAB 8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{\text{WR}}$ (Write)

A low on this input enables the CPU to write control words (ICWs and OCWs) to the SAB 8259A.

$\overline{\text{RD}}$ (Read)

A low on this input enables the SAB 8259A to send the status of the Interrupt Request Register (IRR), In-Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level onto the data bus.

A0

This input signal is used in conjunction with $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all SAB 8259As used in the system. The associated three I/O pins (CAS0-2) are outputs when the SAB 8259A is used as a master and are inputs when the SAB 8259A is used as a slave. As a master, the SAB 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the data bus during the next one or two consecutive $\overline{\text{INTA}}$ pulses.

Interrupt Sequence

The powerful features of the SAB 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an SAB 8080/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The SAB 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{\text{INTA}}$ pulse.
4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The SAB 8259A will also release a CALL instruction code (11001101) onto the 8-bit data bus through its D7-0 pins.
5. This CALL instruction will initiate two more $\overline{\text{INTA}}$ pulses to be sent to the SAB 8259A from the CPU group.
6. These two $\overline{\text{INTA}}$ pulses allow the SAB 8259A to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first $\overline{\text{INTA}}$ pulse and the higher 8-bit address is released at the second $\overline{\text{INTA}}$ pulse.
7. This completes the 3-byte CALL instruction released by the SAB 8259A. In the AEOI[1] mode the ISR bit is reset at the end of the third $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an SAB 8086/8088/80186/80188/80286 system are the same until step 4.

4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The SAB 8259A does not drive the data bus during this cycle.
5. The CPU will initiate a second $\overline{\text{INTA}}$ pulse. During this pulse, the SAB 8259A releases an 8-bit pointer onto the data bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e. the request was too short in duration) the SAB 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

[1] Automatic End of Interrupt

Absolute Maximum Ratings [1]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to 7 V
Power dissipation	1 W

DC Characteristics

TA = 0 to 70°C; VCC = 5 V ±10%

Symbol	Parameter	Limit values		Unit	Test conditions
		min.	max.		
VIL	Input low voltage	−0.5	0.8	V	–
VIH	Input high voltage	2.0	VCC +0.5 V		
VOL	Output low voltage	–	0.45		IOL = 2.2 mA
VOH	Output high voltage	2.4	–		IOH = −400 µA
VOH (INT)	Interrupt output high voltage	3.5			IOH = −100 µA
		2.4			IOH = −400 µA
ILI	Input load current	–	±10	µA	0V ≤ VIN ≤ VCC
ILOL	Output leakage current				0.45 V ≤ VOUT ≤ VCC
ICC	VCC supply current		85	mA	All outputs open
ILIR	IR input load current		−300	µA	VIN = 0V
			10		VIN = VCC

Capacitance

TA = 25°C; VCC = GND = 0V

Symbol	Parameter	Limit values		Unit	Test conditions
		min.	max.		
CIN	Input capacitance	–	10	pF	fC = 1 MHz
CI/O	I/O capacitance		20		Unmeasured pins returned to GND

[1]) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics

TA = 0 to 70°C; VCC = 5V ±10%

Timing Requirements

Symbol	Parameter	Limit values				Unit	Test conditions
		SAB 8259A		SAB 8259A-2			
		min.	max.	min.	max.		
TAHRL	A0/$\overline{CS}$ setup to $\overline{RD}$/$\overline{INTA}\downarrow$	0	–	0	–	ns	–
TRHAX	A0/$\overline{CS}$ hold after $\overline{RD}$/$\overline{INTA}\uparrow$						
TRLRH	$\overline{RD}$ pulse width	235		160			
TAHWL	A0/$\overline{CS}$ setup to $\overline{WR}\downarrow$	0		0			
TWHAX	A0/$\overline{CS}$ hold after $\overline{WR}\uparrow$						
TWLWH	$\overline{WR}$ pulse width	290		190			
TDVWH	Data setup to $\overline{WR}\uparrow$	240		160			
TWHDX	Data hold after $\overline{WR}\uparrow$	0		0			
TJLJH	Interrupt request width (low)	100		100			[1]
TCVIAL	Cascade setup to second or third $\overline{INTA}\downarrow$ (slave only)	55		40			–
TRHRL	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160		160			
TWHRL	End of $\overline{WR}$ to next $\overline{WR}$	190		190			
TCHCL[2]	End of command to next command (not same command type)	210		210			
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	500		500			

Timing Responses

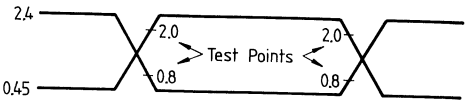
Symbol	Parameter	Limit values				Unit	Test conditions
		SAB 8259A		SAB 8259A-2			
		min.	max.	min.	max.		
TRLDV	Data valid from $\overline{RD}$/$\overline{INTA}\downarrow$	–	200	–	120	ns	C of data bus:
TRHDZ	Data float after $\overline{RD}$/$\overline{INTA}\uparrow$	10	100	10	85		max. test C =
TJHIH	Interrupt output delay	–	350	–	300		100 pF
TIALCV	Cascade valid from first $\overline{INTA}\downarrow$ (master only)		565		360		min. test C = 15 pF
TRLEL	Enable active from $\overline{RD}\downarrow$ or $\overline{INTA}\downarrow$		125		100		CINT = 100 pF
TRHEH	Enable inactive from $\overline{RD}\uparrow$ or $\overline{INTA}\uparrow$		150		150		C cascade = 100 pF
TAHDV	Data valid from stable address		200		200		
TCVDV	Cascade valid to valid data		300				

[1] This is the low time required to clear the input latch in the edge-triggered mode.

[2] Worst-case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns.

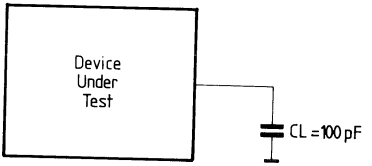
AC Testing Input, Output Waveform

Input/Output



AC testing: inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

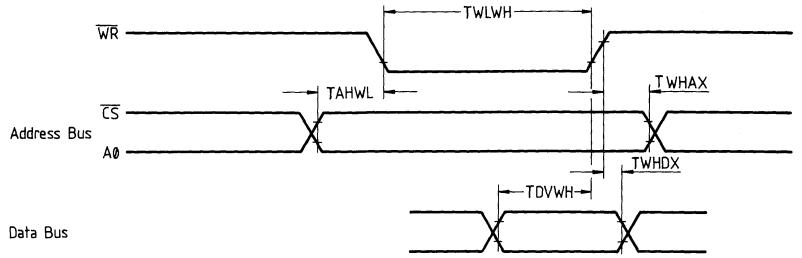
AC Testing Load Circuit



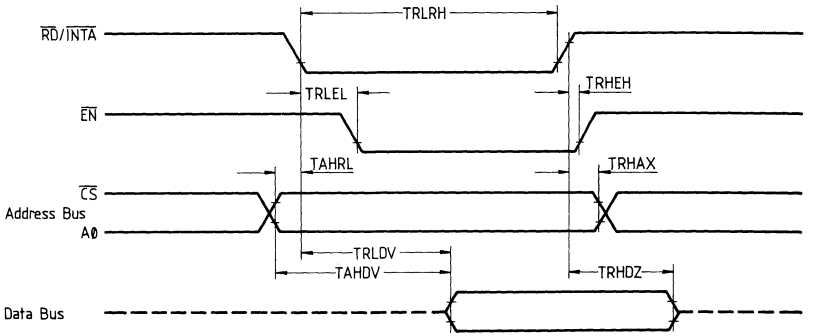
CL includes jig capacitance

Waveforms

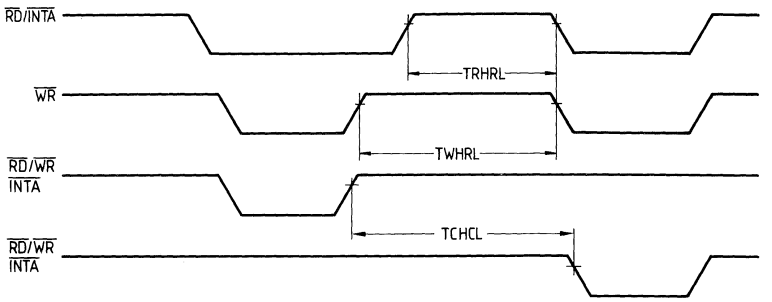
Write



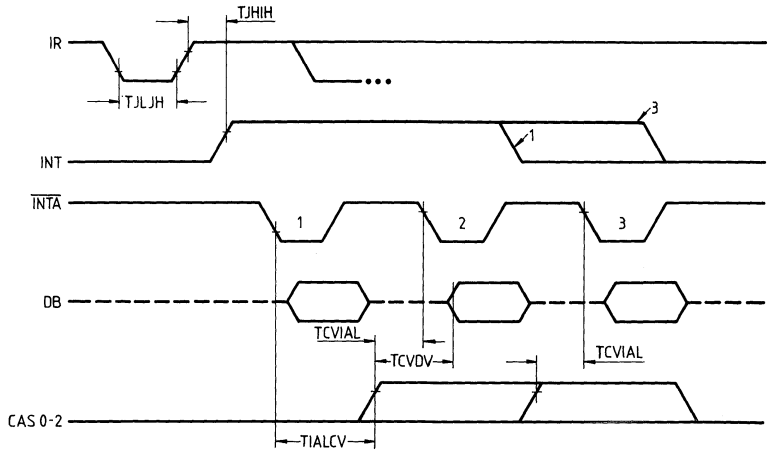
Read/INTA



Other Timings



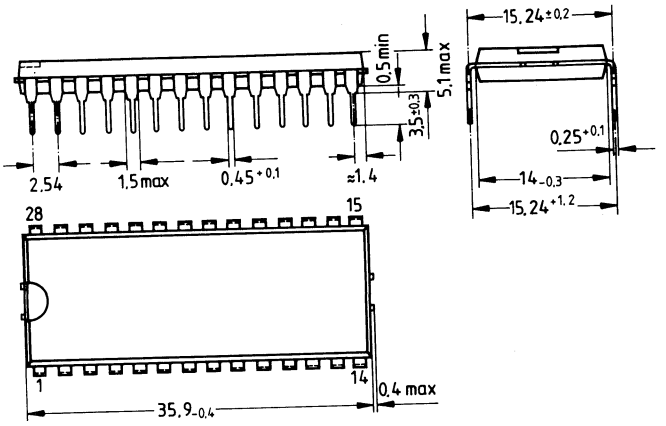
$\overline{\text{INTA}}$ Sequence



Notes: Interrupt output must remain high at least until leading edge of first $\overline{\text{INTA}}$.
[1]) Cycle 1 in SAB 8086/88 systems, the data bus is not active.
[2]) Cycle 2.
[3]) Cycle 3 in SAB 8085 systems only.

Package Outline

28-Pin Plastic Package, Type P



Dimensions in mm

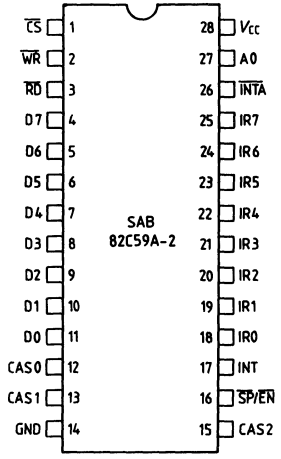
Ordering Information

Type	Description	Ordering Code
SAB 8259A	Programmable interrupt controller, 5 MHz, plastic package	Q67120-P46
SAB 8259A-2-P	Programmable interrupt controller, 8 MHz, plastic package	Q67120-P81

SAB 82C59A-2
CMOS Programmable Interrupt Controller

- Compatible with NMOS and CMOS 8085A, SAB 8086/8088, SAB 80186/80188, SAB 80286 and 80386 processor families
- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Fully static design
- Low standby power dissipation
- Compatible with the industry standard NMOS SAB 8259A-2

Pin Configuration



Pin Names

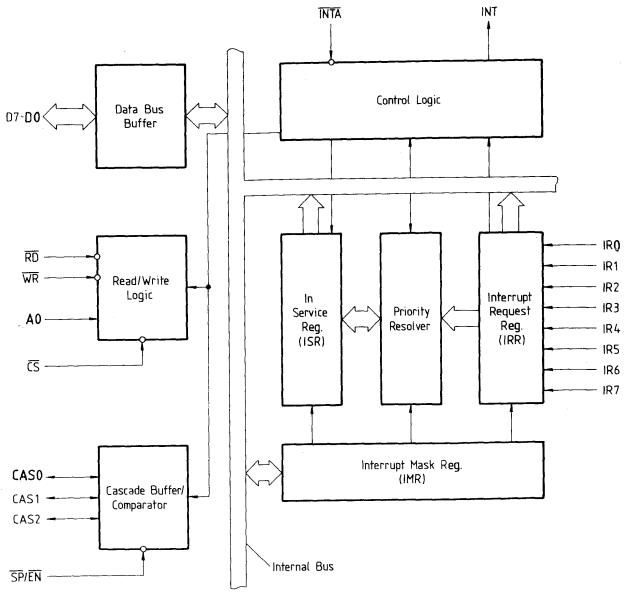
D7-D0	Data Bus (bidirectional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0	Command Select Address
$\overline{CS}$	Chip Select
CAS2-CAS0	Cascade Lines
$\overline{SP}/\overline{EN}$	Slave Program/Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0-IR7	Interrupt Request Inputs

The SAB 82C59A-2 Programmable Interrupt Controller is a high-performance CMOS version of the NMOS SAB 8259A-2. The SAB 82C59A-2 is fabricated in Siemens ACMOS technology and compatible with the industry standard 8259A.
The SAB 82C59A-2 handles up to 8 vectored interrupts to the CPU. It is designed to minimize the software and real-time overhead in handling multilevel priority interrupts. It offers several modes, permitting optimization for a variety of system requirements. Packaged in a 28-pin plastic dual-in-line package, the SAB 82C59A-2 as a static CMOS circuit insures low operating power.

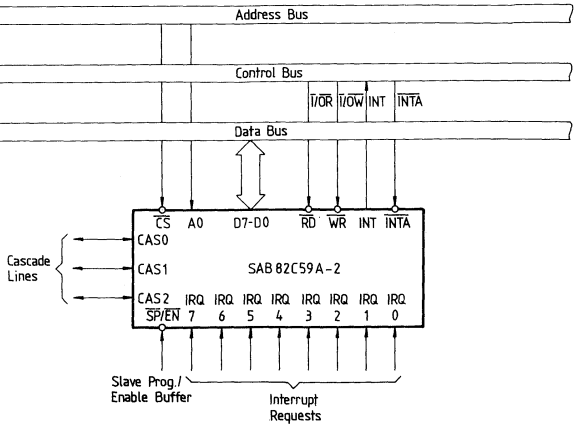
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{CS}$	1	I	$\overline{CHIP\ SELECT}$ A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the SAB 82C59A-2. $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{WR}$	2	I	$\overline{WRITE}$ A low on this pin, when $\overline{CS}$ is low, enables the SAB 82C59A-2 to accept command words from the CPU.
$\overline{RD}$	3	I	$\overline{READ}$ A low on this pin, when $\overline{CS}$ is low, enables the SAB 82C59A-2 to release status onto the data bus for the CPU.
D7-D0	4-11	I/O	BIDIRECTIONAL DATA BUS Control, status, and interrupt vector information is transferred via this bus.
CAS0-CAS2	12, 13, 15	I/O	CASCADE LINES The CAS lines form a private SAB 82C59A-2 bus to control a multiple SAB 82C59A-2 structure. These pins are outputs for a master SAB 82C59A-2 and inputs for a slave SAB 82C59A-2.
$\overline{SP}/\overline{EN}$	16	I/O	$\overline{SLAVE\ PROGRAM}/\overline{ENABLE\ BUFFER}$ This is a dual-function pin. When in buffered mode it can be used as an output to control buffer transceivers ($\overline{EN}$). When not in buffered mode it is used as an input to designate a master ($\overline{SP} = 1$) or slave ($\overline{SP} = 0$).
INT	17	O	INTERRUPT This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU and is, therefore, connected to the CPU's interrupt pin.
IR0-IR7	18-25	I	INTERRUPT REQUESTS These are asynchronous inputs. An interrupt request can be generated by raising an IR input (low to high) and holding it high until it is acknowledged (edge-triggered mode), or just by a high level on an IR input (level-triggered mode).
$\overline{INTA}$	26	I	$\overline{INTERRUPT\ ACKNOWLEDGE}$ This pin is used to enable SAB 82C59A-2 interrupt vector data onto the data bus. This is done by a sequence of interrupt acknowledge pulses issued by the CPU.
A0	27	I	A0 ADDRESS LINE This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. It is used by the SAB 82C59A-2 to distinguish between various command words written by the CPU and the status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for SAB 8086/80186/80286).
V_{CC}	28	–	POWER SUPPLY (+5 V)
GND	14	–	GROUND (0 V)

Functional Block Diagram



Interface to Standard System Bus



Functional Description

General

The SAB 82C59A-2 is a device specifically designed for use in real-time, interrupt-driven microcomputer systems. It manages eight levels of requests and has built-in features for expandability to other SAB 82C59A-2 devices (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the SAB 82C59A-2 can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two cascaded registers: the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during an $\overline{\text{INTA}}$ pulse.

Interrupt Mask Register (IMR)

The IMR stores the bits which mask the interrupt lines. The IMR operation is based on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the SAB 8085A/8086/8088/80186/80188/80286 and 80386.

$\overline{\text{INTA}}$ (Interrupt Acknowledge)

$\overline{\text{INTA}}$ pulses will cause the SAB 82C59A-2 to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the SAB 82C59A-2.

Data Bus Buffer

This tristate, bidirectional 8-bit buffer is used to interface the SAB 82C59A-2 to the system data bus. Control words and status information are transferred through the data bus buffer.

Read/Write Control Logic

The function of this block is to accept output commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the SAB 82C59A-2 to be transferred onto the data bus.

$\overline{\text{CS}}$ (Chip Select)

A low on this input enables the SAB 82C59A-2. No reading or writing of the chip will occur unless the device has been selected.

$\overline{\text{WR}}$ (Write)

A low on this input enables the CPU to write control words (ICWs and OCWs) to the SAB 82C59A-2.

$\overline{\text{RD}}$ (Read)

A low on this input enables the SAB 82C59A-2 to send the status of the Interrupt Request Register (IRR), the In-Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level onto the data bus.

A0

This input signal is used in conjunction with $\overline{\text{WR}}$ and $\overline{\text{RD}}$ signals to write commands into the various command registers, as well as to read the various status registers of the chip. This line can be tied directly to one of the address lines.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all SAB 82C59A-2 devices used in the system. The associated three I/O pins (CAS0-2) are outputs when the SAB 82C59A-2 is used as a master and are inputs when the SAB 82C59A-2 is used as a slave. As a master, the SAB 82C59A-2 sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the data bus during the next one or two consecutive $\overline{\text{INTA}}$ pulses.

Interrupt Sequence

The powerful features of the SAB 82C59A-2 in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

In an SAB 8085A system the events occur as follows:

1. One or more of the interrupt request lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The SAB 82C59A-2 evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{\text{INTA}}$ pulse.
4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The SAB 82C59A-2 will also release a "call" instruction code (11001101) onto the 8-bit data bus through its D7-0 pins.
5. This "call" instruction will initiate two more $\overline{\text{INTA}}$ pulses to be sent to the SAB 82C59A-2 from the CPU group.
6. These two $\overline{\text{INTA}}$ pulses allow the SAB 82C59A-2 to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first $\overline{\text{INTA}}$ pulse and the higher 8-bit address is released at the second $\overline{\text{INTA}}$ pulse.
7. This completes the 3-byte "call" instruction released by the SAB 82C59A-2. In the AEOI (automatic end of interrupt) mode the ISR bit is reset at the end of the third $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an SAB 8086/8088/80186/80188/80286 or 80386 system are the same until step 4.

4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The SAB 82C59A-2 does not drive the data bus during this cycle.
5. The CPU will initiate a second $\overline{\text{INTA}}$ pulse. During this pulse, the SAB 82C59A-2 releases an 8-bit pointer onto the data bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode, the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e. the request duration was too short), the SAB 82C59A-2 will issue an interrupt level 7. Both, the vectoring bytes and the CAS lines will look as if an interrupt level 7 was requested.

Absolute Maximum Ratings [1]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to V_{CC}+0.5 V
Supply voltage with respect to ground	−0.5 to 7.0 V
Power dissipation	1 W

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±10%; GND = 0V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage	−0.5	0.8	V	–
V_{IH}	Input high voltage	2.0	V_{CC} +0.5	V	–
V_{OL}	Output low voltage	–	0.4	V	I_{OL} = 2.5 mA
V_{OH}	Output high voltage	3.0 V_{CC} −0.4	–	V	I_{OH} = −2.5 mA I_{OH} = −100 µA
I_{LI}	Interrupt leakage current	–	±1	µA	0 V < V_{IN} < V_{CC}
I_{LOL}	Output leakage current	–	±10	µA	0 V < V_{OUT} < V_{CC}
I_{LIR}	IR input leakage current	–	−300 +10	µA	V_{IN}= 0 V V_{IN} = V_{CC}
I_{CC}	Operating supply current	–	5	mA	[2]
I_{CCS}	Standby supply current	–	10	µA	V_{CC} = 5.5 V, outputs unloaded, V_{IN} = V_{CC} or GND All IR inputs = V_{CC}

Capacitance

T_A = 25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	5	pF	f_c = 1 MHz Unmeasured pins returned to GND
C_{IO}	I/O capacitance	–	20	pF	
C_{OUT}	Output capacitance	–	15	pF	

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Repeated data input with 8086-2 timings.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5 V ±10%; GND = 0 V

Timing Requirements

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{AHRL}	A0/$\overline{CS}$ setup to $\overline{RD}$/$\overline{INTA}\downarrow$	0	–	ns	–
t_{RHAX}	A0/$\overline{CS}$ hold after $\overline{RD}$/$\overline{INTA}\uparrow$	0	–	ns	–
t_{RLRH}	$\overline{RD}$ pulse width	160	–	ns	–
t_{AHWL}	A0/$\overline{CS}$ setup to $\overline{WR}\downarrow$	0	–	ns	–
t_{WHAX}	A0/$\overline{CS}$ hold after $\overline{WR}\uparrow$	0	–	ns	–
t_{WLWH}	$\overline{WR}$ pulse width	190	–	ns	–
t_{DVWH}	Data setup to $\overline{WR}\uparrow$	160	–	ns	–
t_{WHDX}	Data hold after $\overline{WR}\uparrow$	0	–	ns	–
t_{JLJH} [1]	Interrupt request width (low)	100	–	ns	–
t_{CVIAL}	Cascade setup to second or third $\overline{INTA}\downarrow$ (slave only)	40	–	ns	–
t_{RHRL}	End of $\overline{RD}$ to next $\overline{RD}$ End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160	–	ns	–
t_{WHRL}	End of $\overline{WR}$ to next $\overline{WR}$	190	–	ns	–
t_{CHCL} [2]	End of command to next command (not same command type)	180	–	ns	–
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	400	–	ns	–

Timing Responses

Symbol	Parameter	Limit values		Unit	Test condition[3]
		min.	max.		
t_{RLDV}	Data valid from $\overline{RD}$/$\overline{INTA}\downarrow$	–	120	ns	1
t_{RHDZ}	Data float after $\overline{RD}$/$\overline{INTA}\uparrow$	10	85	ns	2
t_{JHIH}	Interrupt output delay	–	300	ns	1
t_{IALCV}	Cascade valid from first $\overline{INTA}\downarrow$ (master only)	–	360	ns	1
t_{RLEL}	Enable active from $\overline{RD}\downarrow$ or $\overline{INTA}\downarrow$	–	100	ns	1
t_{RHEH}	Enable inactive from $\overline{RD}\uparrow$ or $\overline{INTA}\uparrow$	–	150	ns	1
t_{AHDV}	Data valid from stable address	–	200	ns	1
t_{CVDV}	Cascade valid to valid data	–	200	ns	1

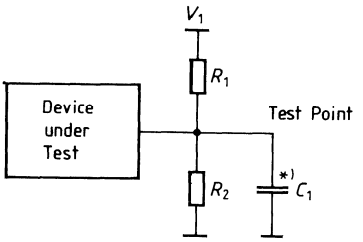
[1]) This is the low time required to clear the input latch in the edge-triggered mode.

[2]) Worst-case timing for t_{CHCL} in an actual microprocessor system is typically much greater than 400 ns.

[3]) See diagrams on next page.

AC Testing

Load Circuit

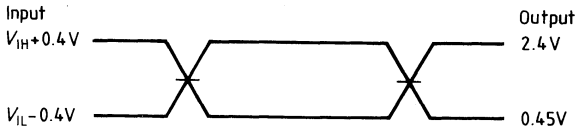


*) Includes Stray and Jig Capacitance

Test Condition Definition

Test Condition	V_1	R_1	R_2	C_1
1	1.7 V	523 Ω	Open	100 pF
2	4.5 V	1.8 kΩ	1.8 kΩ	30 pF

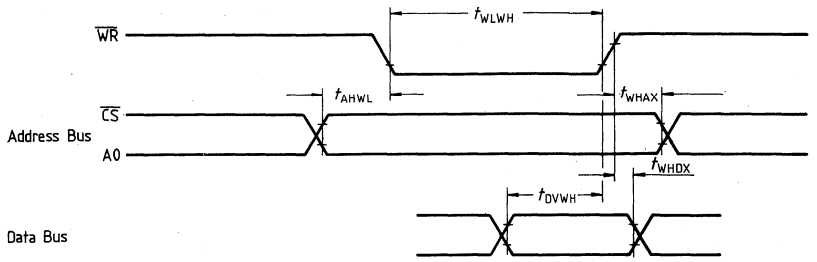
I/O Waveform



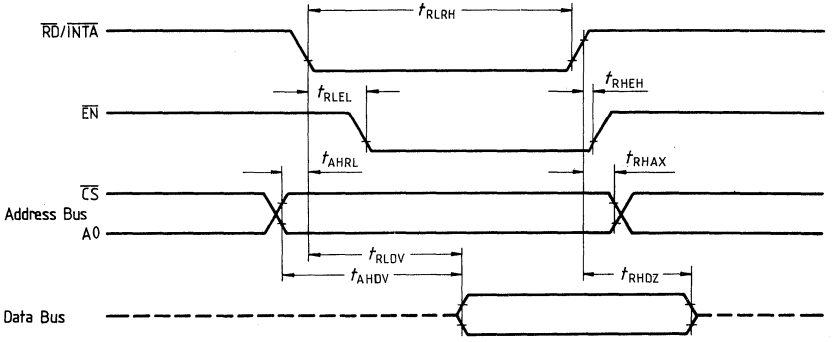
AC testing: All input signals must switch between V_{IL} −0.4 V and V_{IH} + 0.4 V. Input rise and fall times must be ≤15 ns. All timing measurements are made at 2.4 V and 0.45 V.

Waveforms

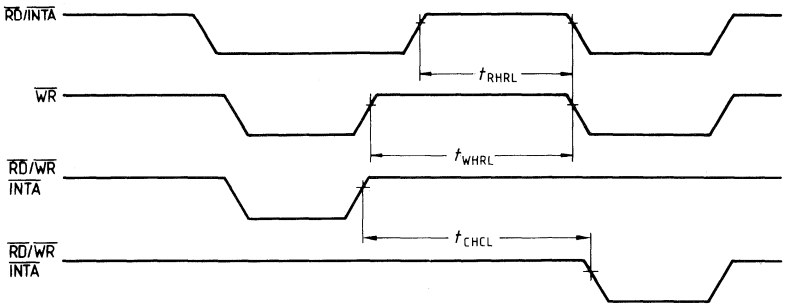
Write



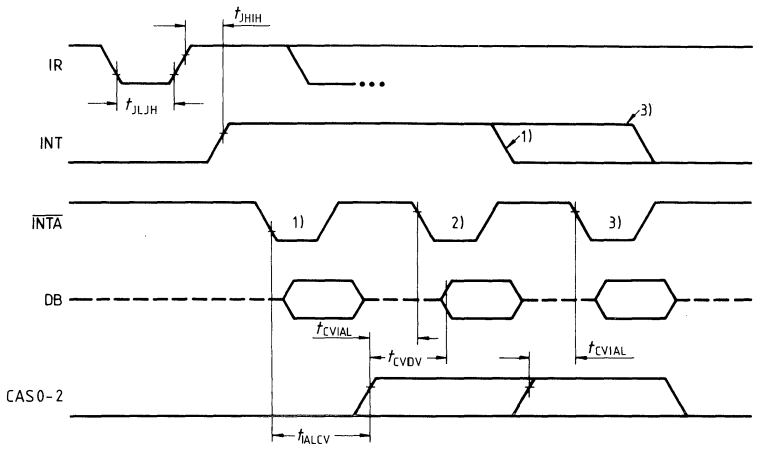
Read/$\overline{INTA}$



Other Timings



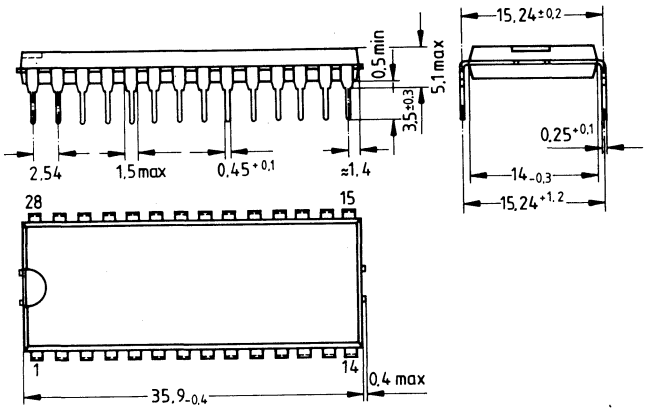
$\overline{\text{INTA}}$ Sequence



Interrupt output must remain high at least until leading edge of first $\overline{\text{INTA}}$.
[1]) Cycle 1 in SAB 8086/8088/80186/80188/80286 and 80386 systems, the data bus is not active.
[2]) Cycle 2.
[3]) Cycle 3 in SAB 8085 systems only.

Package Outlines

Plastic Package, P-DIP-28
(dual-in-line package)
20 B 28 DIN 41870 T 10



Dimensions in mm

Ordering Information

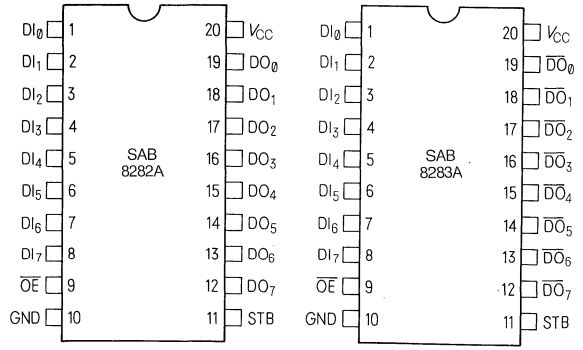
Type	Ordering code	Description
SAB 82C59A-2-P	Q67120-P238	Programmable interrupt controller, 8 MHz, plastic package

Preliminary

SAB 8282A/SAB 8283A Octal Latch

- Fully compatible with SAB 8282/SAB 8283
- 40% Less Power Supply Current than Standard SAB 8282/SAB 8283
- Address Latch for SAB 80286, SAB 80186, SAB 8086, SAB 8085, SAB 8048 and SAB 8051 Families
- High Output Drive Capability for Driving System Data Bus
- Fully Parallel 8-Bit Data Register and Buffer
- No Output Low Noise when Entering or Leaving High Impedance State
- 3-State Outputs
- Transparent during Active Strobe
- 20-Pin Package

Pin Configuration



Pin Names

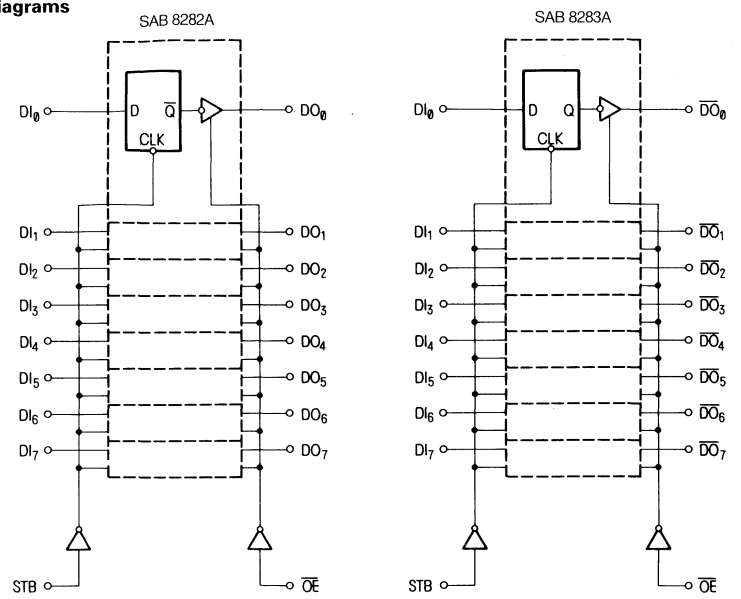
DI_0–DI_7	Data In
DO_0–DO_7	Data Out
$\overline{OE}$	Output Enable
STB	Strobe
V_{CC}	Power Supply (+5V)
GND	Ground (0V)

The SAB 8282A and SAB 8283A are 8-bit bipolar latches with 3-state output buffers. They can be used to implement latches, buffers, or multiplexers. The SAB 8283A inverts the input data at its outputs while the SAB 8282A does not.

Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with these devices. This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

1.85

Logic Diagrams



Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
STB	11	I	STROBE – STB is an input control pulse used to strobe data at the data input pins ($A_\emptyset$–A_7) into the data latches. This signal is active HIGH to admit input data. The data is latched at the HIGH to LOW transition of STB.
$\overline{OE}$	9	I	OUTPUT ENABLE – $\overline{OE}$ is an input control signal which when active LOW enables the contents of the data latches onto the data output pin ($DO_\emptyset$–DO_7 or $\overline{DO_\emptyset}$–$\overline{DO_7}$). $\overline{OE}$ being inactive HIGH forces the output buffers to their high impedance state.
$DI_\emptyset$–DI_7	1–8	I	DATA INPUT PINS – Data presented at these pins satisfying setup time requirements when STB is strobed and latched into the data input latches.
$DO_\emptyset$–DO_7 (SAB 8282A) $\overline{DO_\emptyset}$–$\overline{DO_7}$ (SAB 8283A)	12–19	O	DATA OUTPUT PINS – When $\overline{OE}$ is true, the data in the data latches is presented as inverted (SAB 8283A) or non-inverted (SAB 8282A) data onto the data output pins.
V_{CC}	20	–	Power Supply (+5V)
GND	10	–	Ground (0V)

Functional Description

The SAB 8282A and SAB 8283A octal latches are 8-bit latches with 3-state output buffers.
Data having satisfied the setup time requirements is latched into the data latches by strobing the STB line HIGH to LOW. Holding the STB line in its active HIGH state makes the latches appear transparent.

Data is presented to the data output pins by activating the $\overline{OE}$ input line. When $\overline{OE}$ is inactive HIGH the output buffers are in their high impedance state. Enabling or disabling the output buffers will not cause negative-going transients to appear on the data output bus.

Absolute Maximum Ratings[1)]

Temperature Under Bias	0 to +70°C
Storage Temperature	−65 to +150°C
All Output and Supply Voltages	−0.5 to +7V
All Input Voltages	−1.0 to +5.5V
Power Dissipation	1W

D. C. Characteristics

T_A = 0 to 70°C; V_{CC} = +5V ±10%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_C	Input Clamp Voltage	–	−1	V	I_C = −5 mA
I_{CC}	Power Supply Current SAB 8282A SAB 8283A	–	100 90	mA	all outputs open
I_F	Forward Input Current	–	−0.2		V_F = 0.45V
I_R	Reverse Input Current		50	µA	V_R = 5.25V
V_{OL}	Output LOW Voltage		0.45	V	I_{OL} = 32 mA
V_{OH}	Output HIGH Voltage	2.4	–		I_{OH} = −5 mA
I_{OFF}	Output Off Current	–	±50	µA	V_{OFF} = 0.45 to 5.25V
V_{IL}	Input LOW Voltage		0.8	V	V_{CC} = 5.0V [2)]
V_{IH}	Input HIGH Voltage	2.0	–		
C_{IN}	Input Capacitance	–	12	pF	F = 1 MHz V_{BIAS} = 2.5V, V_{CC} = 5V T_A = 25°C

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) Output Loading: I_{OL} = 32 mA; I_{OH} = −5 mA; C_L = 300 pF

A.C. Characteristics

T_A = 0 to +70°C; V_{CC} = +5 V ± 10%

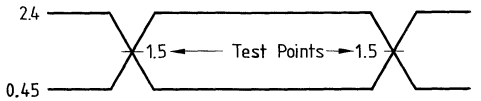
Loading

Outputs: I_{OL} = 32 mA; I_{OH} = −5 mA; C_L = 300 pF

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
t_{IVOV}	Input to Output Delay			ns	2)
	−Inverting	5	22		
	−Non-Inverting	5	30		
t_{SHOV}	STB to Output Delay				
	−Inverting	10	40		
	−Non-Inverting	10	45		
t_{EHOZ}	Output Disable Time	5	18		
t_{ELOV}	Output Enable Time	10	30		
t_{IVSL}	Input to STB Setup Time	0	–		
t_{SLIX}	Input to STB Hold Time	25			
t_{SHSL}	STB HIGH Time	15			
t_{ILIH}, t_{OLOH}	Input, Output Rise Time	–	20		From 0.8 to 2.0 V
t_{IHIL}, t_{OHOL}	Input, Output Fall Time		12		From 2.0 to 0.8 V

A.C. Testing Input, Output Waveform

Input/Output

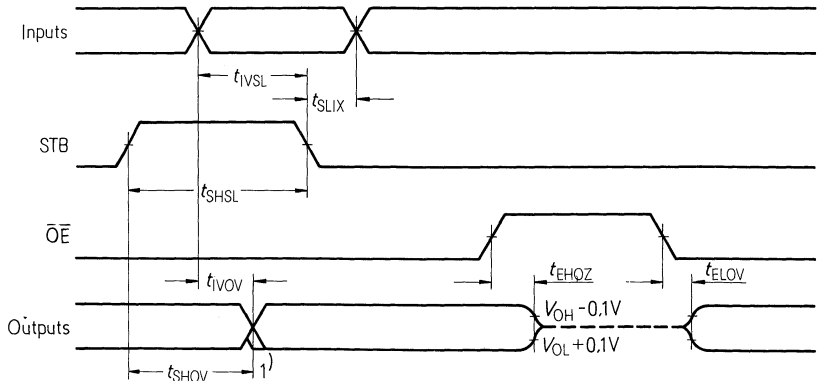


A.C. Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 1.5 V for both a logic "1" and "0".

Waveforms

All timing measurements are made at 1.5 V unless otherwise noted.

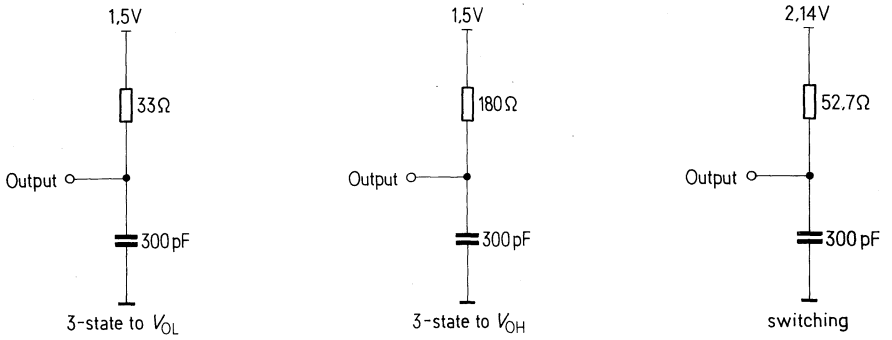
Timing



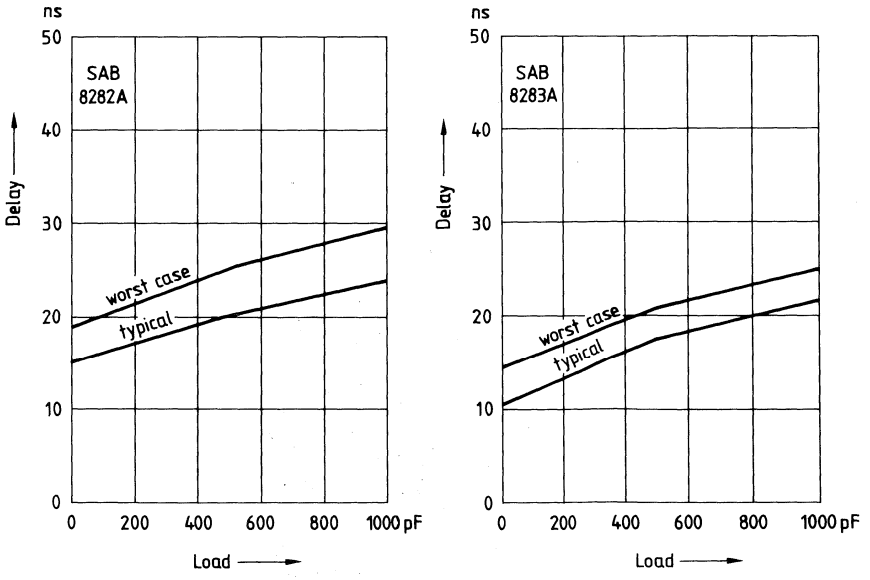
1) SAB 8283A Only – Output may be momentarily invalid following the high going STB transition.

2) See waveforms and test load circuit.

Output Test Load Circuits

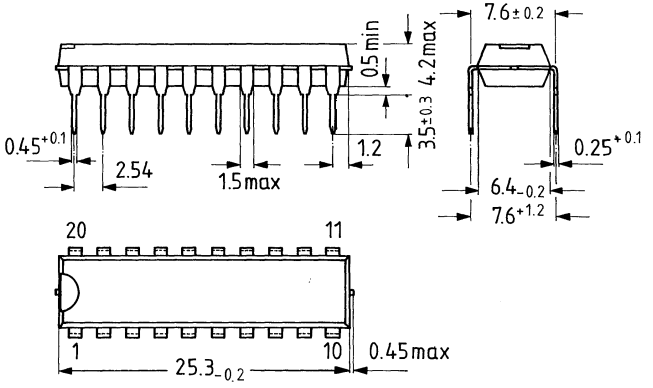


Output Delay vs. Capacitance



Package Outline

20 Pin Plastic Package – Type P



Dimensions in mm

Ordering Information

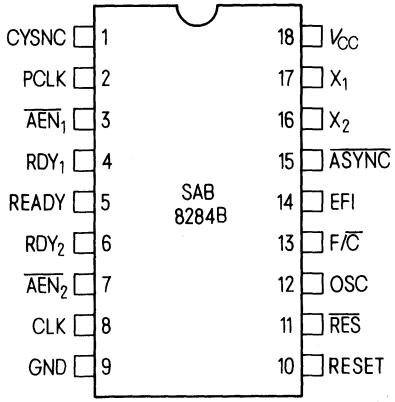
Type	Description	Ordering code
SAB 8282A–P	Octal Latch, non inverting (plastic)	Q 67020–Y149
SAB 8283A–P	Octal Latch, inverting (plastic)	Q 67020–Y150

Preliminary

SAB 8284B, SAB 8284B-1 Clock Generator and Driver for SAB 8086 Family Processors

- Fully compatible with SAB 8284A, SAB 8284A-1
- 30% Less Power Supply Current than Standard SAB 8284A, SAB 8284A-1
- Generates the System clock for SAB 8086 and SAB 8088 Processors: upto 8 MHz with SAB 8284B upto 10 MHz with SAB 8284B-1
- Uses a Crystal or a TTL Signal for Frequency Source upto 30 MHz
- Provides Synchronization for Synchronous and Asynchronous READY Signals
- 18-Pin Package
- Single +5V Power Supply
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with Other SAB 8284Bs

Figure 1
Pin Configuration



Pin Names	
X_1 X_2	Connections for crystal
F/$\overline{C}$	Clock source select
EFI	External clock input
CSYNC	Clock synchronization input
$\overline{ASYNC}$	Ready synchronization select
RDY_1 RDY_2	Ready signal
$\overline{AEN_1}$ $\overline{AEN_2}$	Address enabled qualifiers for $RDY_{1,2}$
$\overline{RES}$	Reset input
RESET	Synchronized reset output
OSC	Oscillator output
CLK	MOS Clock for the processor
PCLK	TTL Clock for peripherals
READY	Synchronized ready output
V_{CC}	Power Supply (+5V)
GND	Ground (OV)

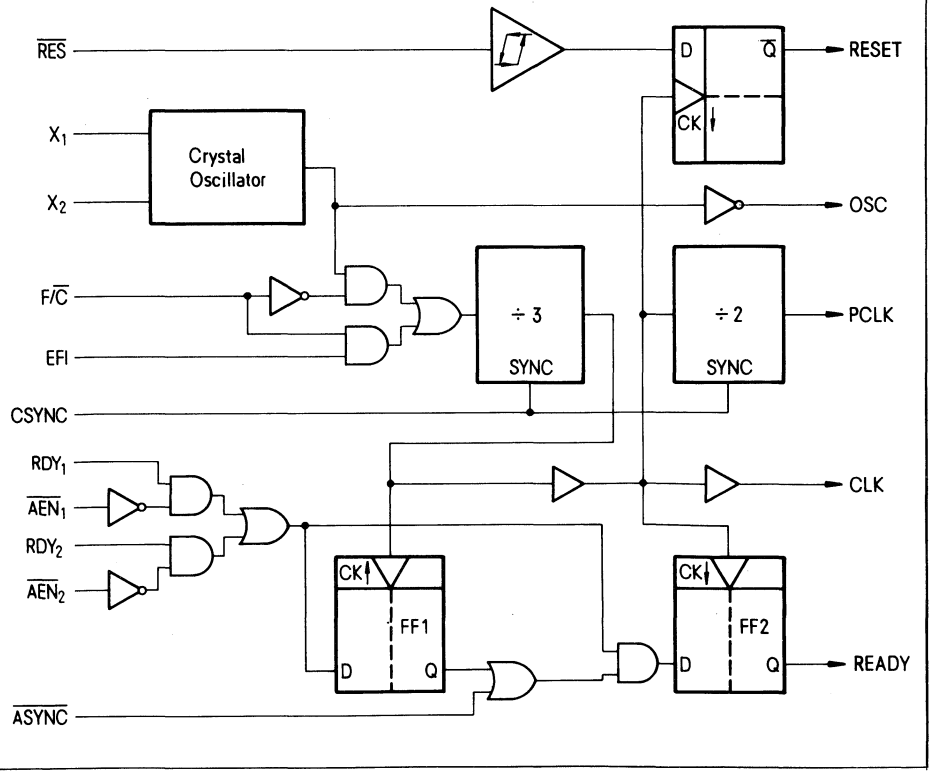
SAB 8284B is a bipolar clock generator/driver designed to provide clock signals for SAB 8086 and SAB 8088 processors and peripherals. It also contains READY logic for operation with two bus systems and provides the processors required READY synchronization and timing. Reset logic with hysteresis and synchronization is also provided. This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
$\overline{AEN_1}$ $\overline{AEN_2}$	3, 7	I	ADDRESS ENABLE. $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY_1 or RDY_2). $\overline{AEN_1}$ validates RDY_1 while $\overline{AEN_2}$ validates RDY_2. Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY_1, RDY_2	4, 6	I	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN_1}$ while RDY2 is qualified by $\overline{AEN_2}$.
$\overline{ASYNC}$	15	I	READY SYNCHRONIZATION SELECT. $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	5	O	READY. READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X_1, X_2	16, 17	I	CRYSTAL IN. X_1 and X_2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.
F/$\overline{C}$	13	I	FREQUENCY/CRYSTAL SELECT. F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processors clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	14	I	EXTERNAL FREQUENCY IN. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	8	O	PROCESSOR CLOCK. CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle. An output HIGH of 4.5 volts (V_{CC} = 5V) is provided on this pin to drive MOS devices.
PCLK	2	O	PERIPHERAL CLOCK. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has 50% duty cycle.
OSC	12	O	OSCILLATOR OUTPUT. OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	11	I	RESET IN. $\overline{RES}$ is an active LOW signal which is used to generate RESET. The SAB 8284B provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.

Symbol	Number	Input (I) Output (O)	Function
RESET	10	O	RESET. RESET is an active HIGH signal which is used to reset the SAB 8086 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION. CSYNC is an active HIGH signal which allows multiple SAB 8284B to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hard-wired to ground.
V_{CC}	18	–	Power Supply (+5V)
GND	9	–	Ground (OV)

Figure 2
Block Diagram



Functional Description

General

The SAB 8284B is a single chip clock generator/ driver for SAB 8086 and SAB 8088 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, "Ready" synchronization and reset logic. Refer to Figure 2 for "Block Diagram" and Figure 1 for "Pin Configuration".

Oscillator

The oscillator circuit of the SAB 8284B is designed primarily for use with an external series resonant fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two series resistors ($R_1 = R_2 = 510\ \Omega$) as shown in figure 7 are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

It is advisable to limit stray capacitances to less than 10pF on X1 and X2 to minimize deviation from operating at the fundamental frequency.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another SAB 8284B clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the SAB 8284B. This is accomplished with two Schottky flip-flops (see figure 3). The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle MOS clock driver designed to drive the SAB 8086 and SAB 8088 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the SAB 8284B. Waveforms for clocks and reset signals are illustrated in Figure 4.

READY Synchronization

Two READY inputs (RDY_1, RDY_2) are provided to accomodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN_1}$ and $\overline{AEN_2}$, respectively).

The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

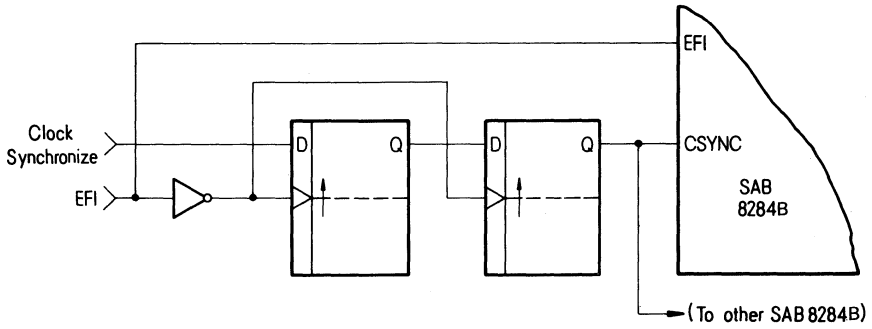
The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time t_{R1VCH}) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, t_{R1VCL}, on each bus cycle (Refer to Figure 5).

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices **that can be guaranteed to meet the required RDY time** (Refer to Figure 6).

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

Figure 3
CSYNC Synchronization



Absolute maximum ratings [1]

Temperature Under Bias	0 to 70°C
Storage Temperature	− 65 to 150°C
All Output and Supply Voltages	−0.5 to 7 V
All Input Voltages	−1.0 to V_{CC} +0.5 V
Power Dissipation	1W

D.C. Characteristics

T_A = 0 to 70°C; V_{CC} = +5V ±10%

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
I_F	Forward Input Current ($\overline{ASYNC}$) Other Inputs	–	−1.3 −0.5	mA	V_F = 0.45 V V_F = 0.45 V
I_R	Reverse Input Current ($\overline{ASYNC}$) Other Inputs	–	50	µA	$V_R = V_{CC}$
V_C	Input Forward Clamp Voltage	–	−1.0	V	I_C = −5 mA
I_{CC}	Power Supply Current	–	110	mA	All outputs open Oscillator circuit inactive (X_1 tied to V_{CC}, X_2 open)
V_{IL}	Input LOW Voltage	–	0.8	V	–
V_{IH}	Input HIGH Voltage	2.0	–		
V_{IHR}	Reset Input HIGH Voltage	2.6			
V_{OL}	Output LOW Voltage	–	0.45		5 mA
V_{OH}	Output HIGH Voltage CLK Other Outputs	4 2.4	–		−1 mA −1 mA
$V_{IHR}-V_{ILR}$	$\overline{RES}$ Input Hysteresis	0.25			–

[1]) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

T_A = 0 to +70°C; V_{CC} = +5 V ±10%

Timing Requirements

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
t_{EHEL}	External Frequency HIGH Time	13		ns	90%–90% V_{IN}
t_{ELEH}	External Frequency LOW Time		–		10%–10% V_{IN}
t_{ELEL}	EFI Period	$t_{EHEL}+t_{ELEH}+\delta$			[3]
	XTAL Frequency	12	25 [7]	MHz	–
t_{R1VCL}	RDY_1, RDY_2 Active Setup to CLK	35	–	ns	$\overline{ASYNC}$ = HIGH
t_{R1VCH}	RDY_1, RDY_2 Active Setup to CLK				$\overline{ASYNC}$ = LOW
t_{R1VCL}	RDY_1, RDY_2 Inactive Setup to CLK				–
t_{CLR1X}	RDY_1, RDY_2 Hold to CLK	0			
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK	50			
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK	0			
t_{A1VR1V}	$\overline{AEN_1}$, $\overline{AEN_2}$ Setup to RDY_1, RDY_2	15			
t_{CLA1X}	$\overline{AEN_1}$, $\overline{AEN_2}$ Hold to CLK	0			
t_{YHEH}	CSYNC Setup to EFI	20			
t_{EHYL}	CSYNC Hold to EFI	10			
t_{YHYL}	CSYNC Width	$2 \cdot t_{ELEL}$			
t_{I1HCL}	$\overline{RES}$ Setup to CLK	65			[4]
t_{CLI1H}	$\overline{RES}$ Hold to CLK	20			
t_{ILIH}	Input Rise Time	–	20		From 0.8 V to 2.0 V
t_{IHIL}	Input Fall Time		12		From 2.0 V to 0.8 V

Notes see next page.

Timing Responses

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
t_{CLCL}	CLK Cycle Period	100			–
t_{CHCL}	CLK HIGH Time	[1]	–		Fig. 7 & Fig. 8
t_{CLCH}	CLK LOW Time	[2]			Fig. 7 & Fig. 8
t_{CH1CH2} t_{CL2CL1}	CLK Rise or Fall Time	–	10		1.0 V to 3.5 V
t_{PHPL}	PCLK HIGH Time	t_{CLCL}–20			–
t_{PLPH}	PCLK LOW Time	t_{CLCL}–20	–		
t_{RYLCL}	Ready Inactive to CLK [6]	–8		ns	Fig. 9 & Fig. 10
t_{RYHCH}	Ready Active to CLK [5]	[2]			Fig. 9 & Fig. 10
t_{CLIL}	CLK to Reset Delay		40		
t_{CLPH}	CLK to PCLK HIGH Delay	–			–
t_{CLPL}	CLK to PCLK LOW Delay		22		
t_{OLCH}	OSC to CLK HIGH Delay	–5			
t_{OLCL}	OSC to CLK LOW Delay	2	35		
t_{OLOH}	Output Rise Time (except CLK)		20		From 0.8 V to 2.0 V
t_{OHOL}	Output Fall Time (except CLK)	–	12		From 2.0 V to 0.8 V

[1]) ($^1/_3$ t_{CLCL}) +2 for CLK Freq. ≤ 8 MHz
($^1/_3$ t_{CLCL}) +6 for CLK Freq. = 10 MHz

[2]) ($^2/_3$ t_{CLCL}) −15 for CLK Freq. ≤ 8 MHz
($^2/_3$ t_{CLCL}) −14 for CLK Freq. = 10 MHZ

[3]) δ = EFI rise (5 ns max) + EFI fall (5 ns max).

[4]) Setup and hold necessary only to guarantee recognition at next clock.

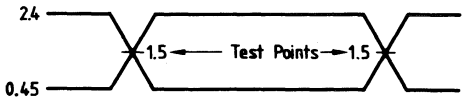
[5]) Applies only to T_3 and T_W states.

[6]) Applies only to T_2 states.

[7]) 30 MHz for SAB 8284B–1

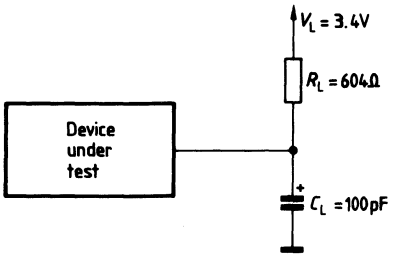
A.C. Testing

Input/Output Waveform

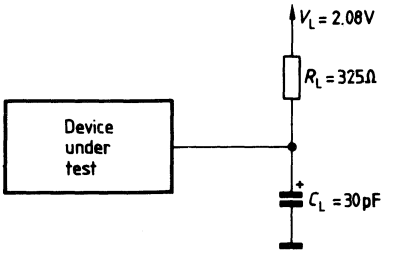


A.C. Testing: Input are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0".
Timing Measurements are made at 1.5 V for Both a Logic "1" and "0".

Load Circuit for CLK output

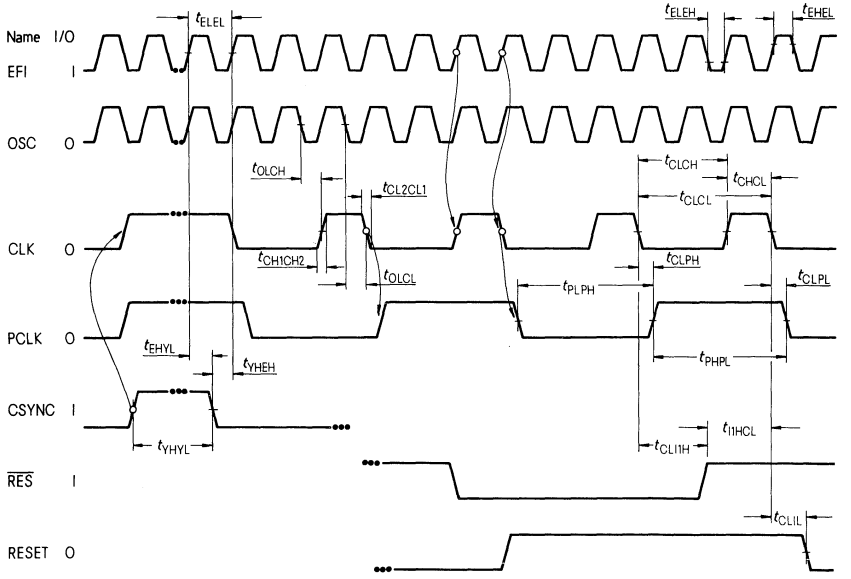


Load Circuit for all other output



Waveforms

Figure 4
Clocks and Reset Signals



Note: All timing measurements are made at 1.5 V,unless otherwise noted.

Figure 5
Ready Signals – Asynchronous Devices

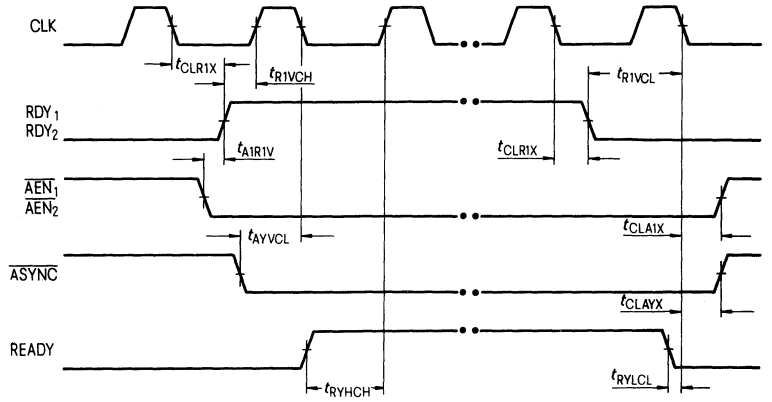
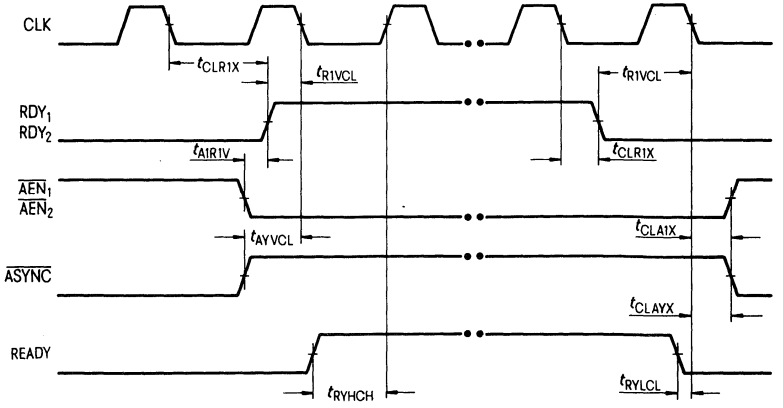


Figure 6
Ready Signals – Synchronous Devices



Testconditions

Figure 7
Clock High- and Low Time; Using X1, X2

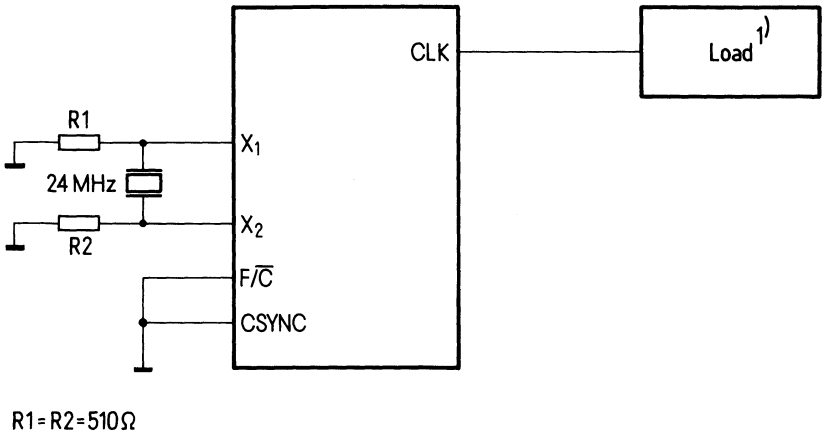
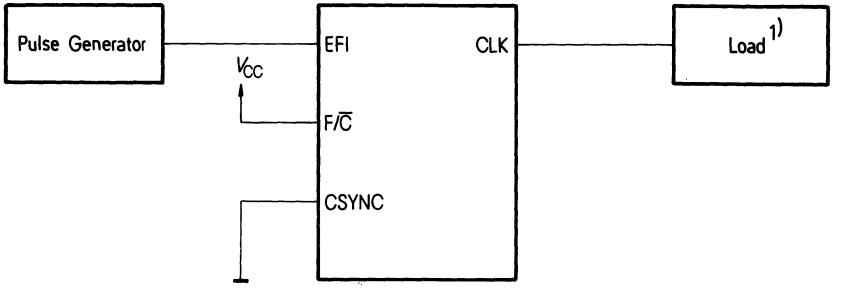
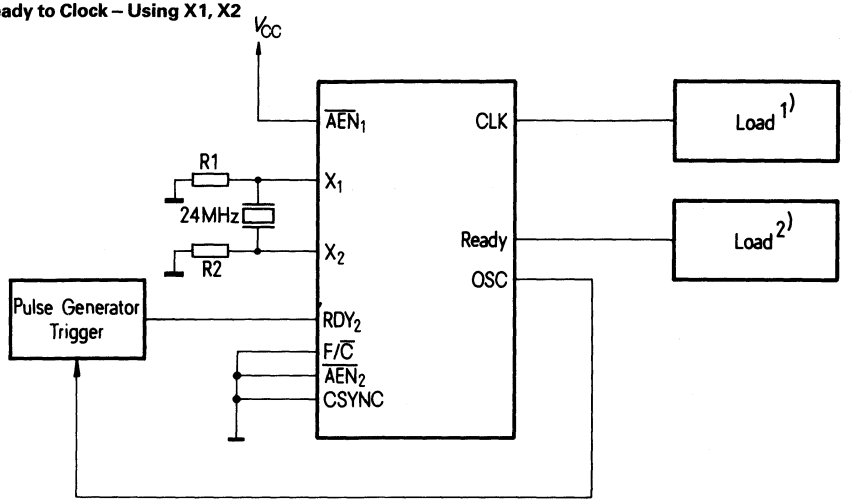


Figure 8
Clock High- and Low Time; Using EFI



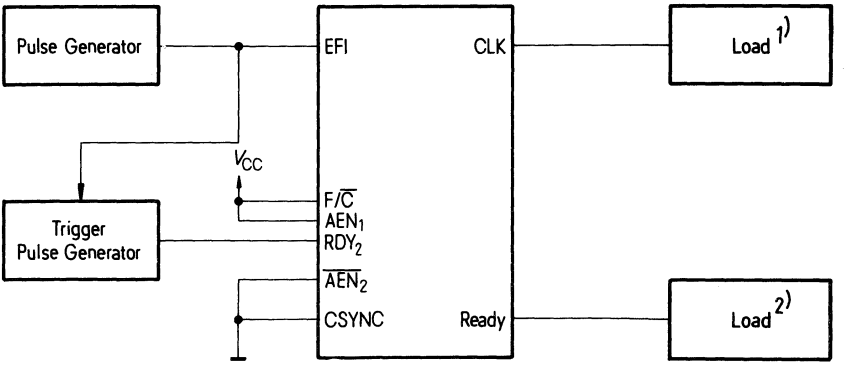
1) C_L = 100 pF

Figure 9
Ready to Clock – Using X1, X2



R1 = R2 = 510 Ω

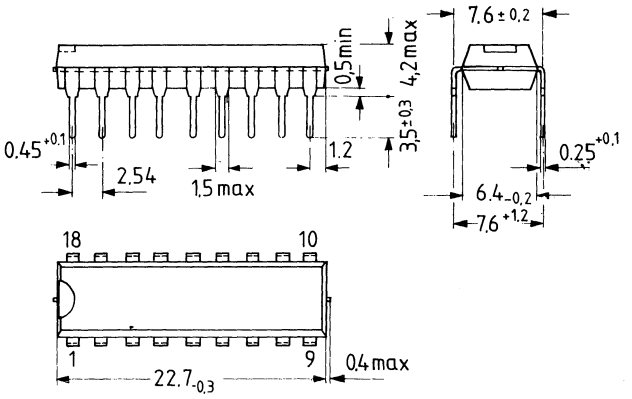
Figure 10
Ready to Clock – Using EFI



1) C_L = 100 pF
2) C_L = 30 pF

Package Outline

18 Pin Plastic Package – Type P



Ordering information

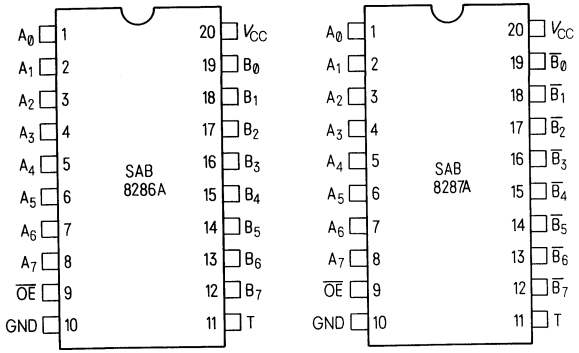
Component	Description	Ordering Code
	Clock Generator- (Plastic Package)	
SAB 8284B – P	upto 8 MHz	Q67020–Y151
SAB 8284B-1 – P	upto 10 MHz	Q67020–Y152

Preliminary

SAB 8286A/SAB 8287A Octal Bus Transceiver

- Fully compatible with SAB 8286/SAB 8287
- 40% Less Power Supply Current than Standard SAB 8286/SAB 8287
- Data Bus Buffer Driver for SAB 80286, SAB 80186, SAB 8086, SAB 8085, SAB 8048 and SAB 8051 Families
- High Output Drive Capability for Driving System Data Bus
- Fully Parallel 8-Bit Transceivers
- 3-State Outputs
- 20-Pin Package
- No Output Low Noise when Entering or Leaving High Impedance State

Pin Configuration

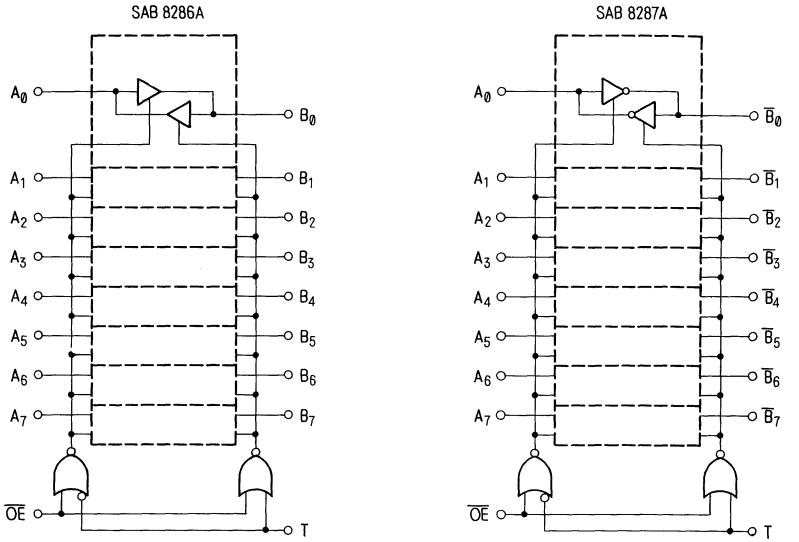


Pin Names

A_0–A_7	Local Bus Data
B_0–B_7	System Bus Data
$\overline{OE}$	Output Enable
T	Transmit
V_{CC}	Power Supply (+5V)
GND	Ground (0V)

The SAB 8286A and SAB 8287A are 8-bit bipolar transceivers with 3-state outputs. The SAB 8287A inverts the input data at its outputs while the SAB 8286A does not. Thus, a wide variety of applications for buffering in microcomputer systems can be met. This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

Logic Diagrams



Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
T	11	I	TRANSMIT – T is an input control signal used to control the direction of the transceivers. When HIGH, it configures the transceiver's B_0–B_7 as outputs with A_0–A_7 as inputs. T LOW configures A_{0-7} as the outputs with B_0–B_7 serving as the inputs.
$\overline{OE}$	9	I	OUTPUT ENABLE – $\overline{OE}$ is an input control signal used to enable the appropriate output driver (as selected by T) onto its respective bus. This signal is active LOW.
A_0–A_7	1–8	I/O	LOCAL BUS DATA PINS – These pins serve to either present data to or accept data from the processor's local bus depending upon the state of the T pin.
B_0–B_7 (SAB 8286A) $\overline{B_0}$–$\overline{B_7}$ (SAB 8287A)	12–19	I/O	SYSTEM BUS DATA PINS – These pins serve to either present data to or accept data from the system bus depending upon the state of the T pin.
V_{CC}	20	–	Power Supply (+5V)
GND	10	–	Ground (0V)

Functional Description

The SAB 8286A and SAB 8287A transceivers are 8-bit transceivers with high impedance outputs. With T active HIGH and $\overline{OE}$ active LOW, data at the A_0–A_7 pins is driven onto the B_0–B_7 pins.

With T inactive LOW and $\overline{OE}$ active LOW, data at the B_0–B_7 pins is driven onto the A_0–A_7 pins. No output low glitching will occur whenever the transceivers are entering or leaving the high impedance state.

Absolute Maximum Ratings[1)]

Temperature Under Bias	0 to +70°C
Storage Temperature	−65 to +150°C
All Output and Supply Voltages	−0.5 to +7V
All Input Voltages	−1.0 to +5.5V
Power Dissipation	1W

D. C. Characteristics

T_A = 0 to 70°C; V_{CC} = +5V ±10%

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
V_C	Input Clamp Voltage	–	−1	V	I_C = −5 mA
I_{CC}	Power Supply Current	–	90	mA	All outputs open
I_F	Forward Input Current	–	−0.2	mA	V_F = 0.45V
I_R	Reverse Input Current	–	50	µA	V_R = 5.25V
V_{OL}	Output LOW Voltage – B Outputs – A Outputs	–	0.45 0.45	V	I_{OL} = 32 mA I_{OL} = 16 mA
V_{OH}	Output HIGH Voltage – B Outputs – A Outputs	2.4 2.4	–	V	I_{OH} = −5 mA I_{OH} = −1 mA
I_{OFF} I_{OFF}	Output Off Current Output Off Current	–	I_F I_R	–	V_{OFF} = 0.45V V_{OFF} = 5.25V
V_{IL}	Input LOW Voltage – A Side – B Side	–	0.8 0.9	V	V_{CC} = 5.0V, See Note 2 V_{CC} = 5.0V, See Note 2
V_{IH}	Input HIGH Voltage	2.0		V	V_{CC} = 5.0V, See Note 2
C_{IN}	Input Capacitance	–	12	pF	F = 1 MHz V_{BIAS} = 2.5V, V_{CC} = 5V T_A = 25°C

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) B Outputs: I_{OL} = 32 mA; I_{OH} = −5 mA; C_L = 300 pF
A Outputs: I_{OL} = 16 mA; I_{OH} = −1 mA; C_L = 100 pF

A.C. Characteristics

T_A = 0 to +70°C; V_{CC} = +5 V ± 10%

Loading
B Outputs: I_{OL} = 32 mA; I_{OH} = −5 mA; C_L = 300 pF A Outputs: I_{OL} = 16 mA; I_{OH} = −1 mA; C_L = 100 pF

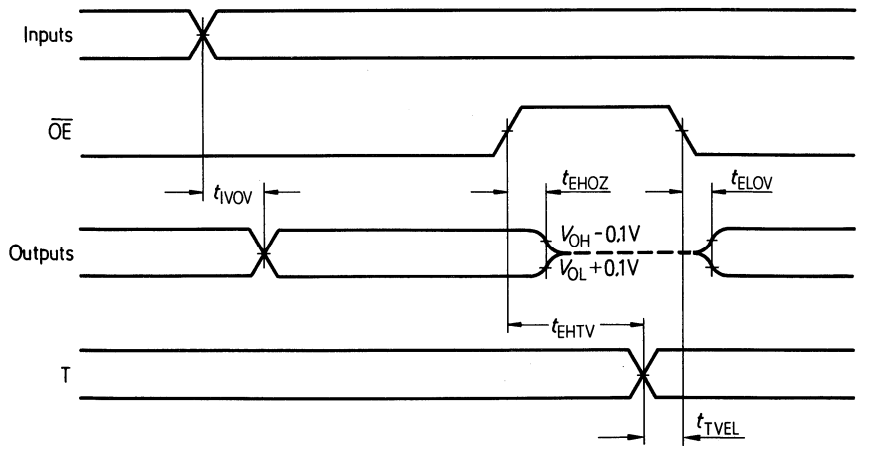
Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
t_{IVOV}	Input to Output Delay Inverting Non-Inverting	 5 5	 22 30	ns	1)
t_{EHTV}	Transmit/Receive Hold Time	5	–		
t_{TVEL}	Transmit/Receive Setup	10			
t_{EHOZ}	Output Disable Time	5	18		
t_{ELOV}	Output Enable Time	10	30		
t_{ILIH}, t_{OLOH}	Input, Output Rise Time	–	20		From 0.8 to 2.0 V
t_{IHIL}, t_{OHOL}	Input, Output Fall Time		12		From 2.0 to 0.8 V

1) See waveforms and test load circuit.

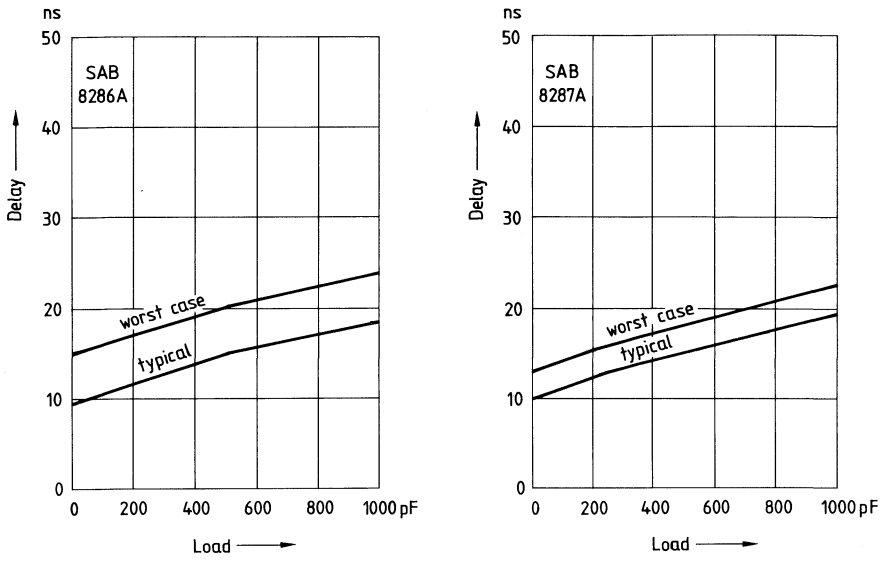
Waveforms

All timing measurements are made at 1.5 V unless otherwise noted.

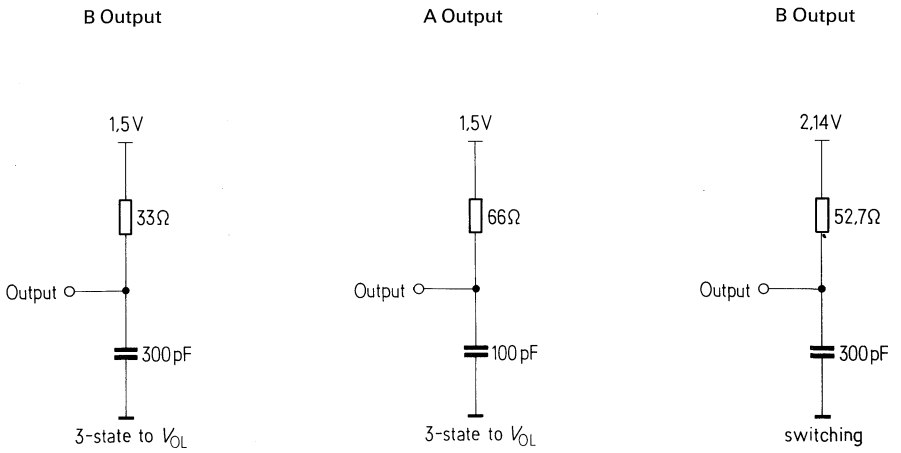
Timing



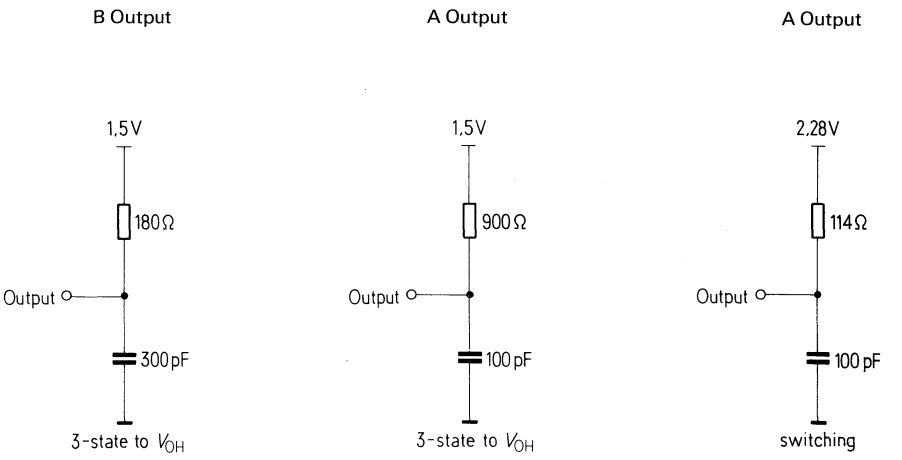
Output Delay vs. Capacitance



Output Test Load Circuit

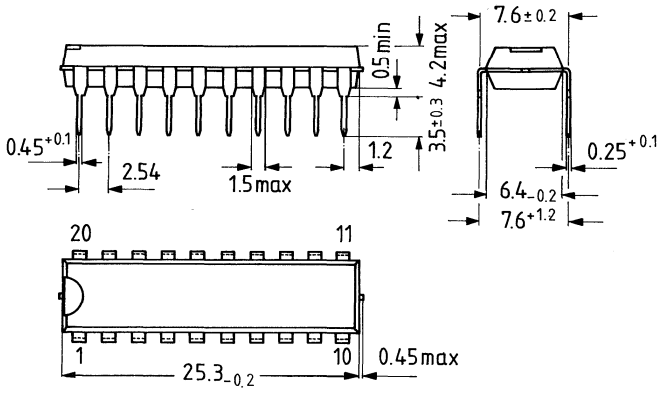


Output Test Load Circuit



Package Outline

20 Pin Plastic Package – Type P



Ordering Information

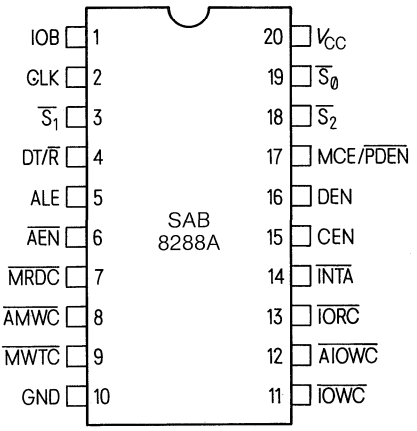
Type	Description	Ordering code
SAB 8286A–P	Octal Bus Transceiver, non inverting (plastic)	Q 67020–Y 153
SAB 8287A–P	Octal Bus Transceiver, inverting (plastic)	Q 67020–Y 154

Preliminary

SAB 8288A Bus Controller for SAB 8086 Family Processors

- Fully compatible with SAB 8288
- 40% Less Power Supply Current than Standard SAB 8288
- Bipolar Drive Capability
- Provides Advanced Commands
- Provides Wide Flexibility in System Configurations
- 3-State Command Output Drivers
- Configurable for Use with an I/O Bus
- Facilitates Interface to One or Two Multi-Master Busses

Pin Configuration



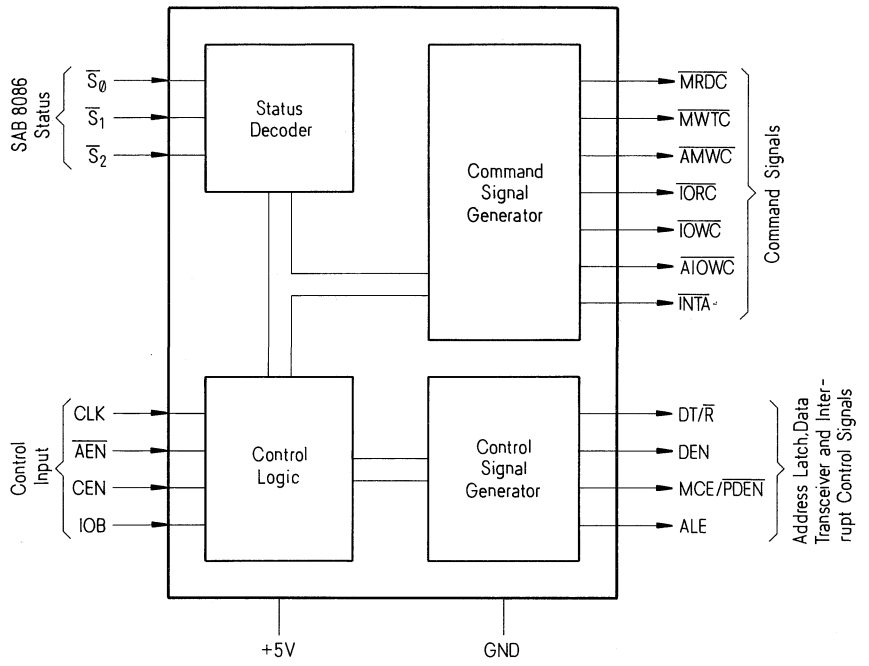
Pin Names

$\overline{S_0} - \overline{S_2}$	Status
CLK	Clock
ALE	Adress Latch Enable
DEN	Data Enable
DT/$\overline{R}$	Data Transmit/Receive
$\overline{AEN}$	Address Enable
CEN	Command Enable
IOB	Input/Output Bus Mode
$\overline{AIOWC}$	Advanced I/O Write
$\overline{IOWC}$	I/O Write
$\overline{IORC}$	I/O Read
$\overline{AMWC}$	Advanced Memory Write
$\overline{MWTC}$	Memory Write
$\overline{MRDC}$	Memory Read
$\overline{INTA}$	Interrupt Acknowledge
MCE/$\overline{PDEN}$	Master Cascade/Peripheral Data
V_{CC}	Power Supply (+5V)
GND	Ground (0V)

SAB 8288A Bus Controller is a 20-pin bipolar component for use with medium-to-large SAB 80186, SAB 80188, SAB 8086 and SAB 8088 processing systems. The bus controller provides command and control timing generation as well as bipolar bus drive capability while optimizing system performance.

A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.
This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

Block Diagram



Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
IOB	1	I	INPUT/OUTPUT BUS MODE – When the IOB is strapped HIGH the SAB 8288A functions in the I/O Bus mode. When it is strapped LOW, the SAB 8288A functions in the System Bus mode. (See sections on I/O Bus and Systems Bus modes).
CLK	2	I	CLOCK – This is a clock signal from the SAB 8284A or SAB 8284B clock generator and serves to establish when command and control signals are generated.
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	3, 18, 19	I	STATUS INPUT PINS – These pins are the status input pins from the SAB 80186, SAB 80188, SAB 8086 or SAB 8088 processors. The SAB 8288A decodes these inputs to generate command and control signals at the appropriate time. When these pins are not in use (passive) they are all HIGH. (See chart under Functional Description).

Symbol	Number	Input (I) Output (O)	Function
DT/$\overline{R}$	4	O	DATA TRANSMIT/RECEIVE – This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (write to I/O or memory) and a LOW indicates Receive (Read).
ALE	5	O	ADDRESS LATCH ENABLE – This signal serves to strobe an address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches.
$\overline{AEN}$	6	I	ADDRESS ENABLE – $\overline{AEN}$ enables command outputs of the SAB 8288A Bus Controller at least 105 ns after it becomes active (LOW). $\overline{AEN}$ going inactive immediately 3-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the SAB 8288A is in the I/O Bus mode (IOB tied HIGH).
$\overline{MRDC}$	7	O	MEMORY READ COMMAND – This command line instructs the memory to drive its data onto the data bus. This signal is active LOW.
$\overline{AMWC}$	8	O	ADVANCED MEMORY WRITE COMMAND – The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	9	O	MEMORY WRITE COMMAND – This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{IOWC}$	11	O	I/O WRITE COMMAND – This command line instructs an I/O device to read the data on the data bus. This signal is active LOW.
$\overline{AIOWC}$	12	O	ADVANCED I/O WRITE COMMAND – The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IORC}$	13	O	I/O READ COMMAND – This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
$\overline{INTA}$	14	O	INTERRUPT ACKNOWLEDGE – This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
CEN	15	I	COMMAND ENABLE – When this signal is LOW all SAB 8288A command outputs and the DEN and $\overline{PDEN}$ control outputs are forced to their inactive state. When this signal is HIGH, these same outputs are enabled.
DEN	16	O	DATA ENABLE – This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
MCE/$\overline{\text{PDEN}}$	17	O	This is a dual function pin: MCE (IOB is tied LOW) – **Master Cascade Enable** occurs during an interrupt sequence and serves to read a Cascade. Address from a master PIC (Priority Interrupt Controller) onto the data bus. The MCE signal is active HIGH. $\overline{\text{PDEN}}$ (IOB is tied HIGH) – **Peripheral Data Enable** enables the data bus transceiver for the I/O bus during I/O instructions. It performs the same function for the I/O bus that DEN performs for the system bus. $\overline{\text{PDEN}}$ is active LOW.
V_{CC}	20	–	Power Supply (+5V)
GND	10	–	Ground (0V)

Functional Description

The command logic decodes the three SAB 80186, SAB 80188, SAB 8086 or SAB 8088 CPU status lines ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) to determine what command is to be issued. This chart shows the meaning of each status "word".

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Processor State	SAB 8288A Command
0	0	0	Interrupt Acknowledge	$\overline{\text{INTA}}$
0	0	1	Read I/O Port	$\overline{\text{IORC}}$
0	1	0	Write I/O Port	$\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{\text{MRDC}}$
1	0	1	Read Memory	$\overline{\text{MRDC}}$
1	1	0	Write Memory	$\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$
1	1	1	Passive	None

The command is issued in one of two ways dependent on the mode of the SAB 8288A Bus Controller.

I/O Bus Mode – The SAB 8288A is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode all I/O command lines ($\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$, $\overline{\text{INTA}}$) are always enabled (i.e., not dependent on $\overline{\text{AEN}}$). When an I/O command is initiated by the processor, the SAB 8288A immediately activates the command lines using $\overline{\text{PDEN}}$ and DT/$\overline{\text{R}}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one SAB 8288A Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{\text{AEN}}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode – The SAB 8288A is in the System Bus mode if the IOB pin is strapped LOW. In this mode no command is issued until 115 ns after the $\overline{\text{AEN}}$ Line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{\text{AEN}}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

Command Outputs

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

The command output are:
$\overline{MRDC}$ – Memory Read Command
$\overline{MWTC}$ – Memory Write Command
$\overline{IORC}$ – I/O Read Command
$\overline{IOWC}$ – I/O Write Command
$\overline{AMWC}$ – Advanced Memory Write Command
$\overline{AIOWC}$ – Advanced I/O Write Command
$\overline{INTA}$ – Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

Control Outputs

The control outputs of the SAB 8288A are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$). The DEN signal determines when the external bus should be enable onto the local bus and the DT/$\overline{R}$ determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ pin changes function with the two modes of the SAB 8288A. When the SAB 8288A is in the IOB mode (IOB HIGH) the PDEN signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

Interrupt Acknowledge and MCE

The MCE signal is used during an interrupt acknowledge cycle if the SAB 8288A is in the System Bus mode (IOB LOW). During any interrupt sequence there are two interrupt acknowledge cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable and Halt

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the address latches. ALE also serves to strobe the status ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) into a latch for halt state decoding.

Command Enable

The Command Enable (CEN) input acts as a command qualifier for the SAB 8288A. If the CEN pin is high the SAB 8288A functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

Absolute Maximum Ratings [1]

Temperature Under Bias	0 to +70°C
Storage Temperature	−65 to +150°C
All Output and Supply Voltages	−0.5 to +7 V
All Input Voltages	−1.0 to +5.5 V
Power Dissipation	1 W

D.C. Characteristics

T_A = 0 to 70°C; V_{CC} = +5 V ±10%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_C	Input Clamp Voltage		−1	V	I_C = −5 mA
I_{CC}	Power Supply Current		140	mA	All outputs open
I_F	Forward Input Current	–	−0.7		V_F = 0.45 V
I_R	Reserve Input Current		50	µA	$V_R = V_{CC}$
V_{OL}	Output Low Voltage Command Outputs Control Outputs		 0.5 0.5		 I_{OL} = 32 mA I_{OL} = 16 mA
V_{OH}	Output High Voltage Command Outputs Control Outputs	 2.4 2.4	 –	V	 I_{OH} = −5 mA I_{OH} = −1 mA
V_{IL}	Input Low Voltage	–	0.8		–
V_{IH}	Input High Voltage	2.0	–		
I_{OFF}	Output Off Current	–	100	µA	V_{OFF} = 0.4 to 5.25 V

A.C. Characteristics

T_A = 0 to 70°C; V_{CC} = +5 V ±10%

Timing Requirements

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
t_{CLCL}	CLK Cycle Period	100			
t_{CLCH}	CLK Low Time	50			
t_{CHCL}	CLK High Time	30			
t_{SVCH}	Status Active Setup Time	35	–	ns	–
t_{CHSV}	Status Active Hold Time	10			
t_{SHCL}	Status Inactive Setup Time	35			
t_{CLSH}	Status Inactive Hold Time	10			
t_{ILIH}	Input, Rise Time	–	20		From 0.8V to 2.0V
t_{IHIL}	Input, Fall Time		12		From 2.0V to 0.8V

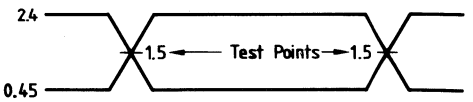
1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Timing Responses

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
t_{CVNV}	Control Active Delay	5	45	ns	
t_{CVNX}	Control Inactive Delay	10			
t_{CLLH}, t_{CLMCH}	ALE MCE Active Delay (from CLK)	–	20		
t_{SVLH}, t_{SVMCH}	ALE MCE Active Delay (from Status)				
t_{CHLL}	AIE Inactive Delay	4	15		$\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{IOWC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{AIOWC}$: $I_{OL} = 32$ mA, $I_{OH} = -5$ mA, $C_L = 300$ pF
t_{CLML}	Command Active Delay	10	35		
t_{CLMH}	Command Inactive Delay				
t_{CHDTL}	Direction Control Active Delay	–	50		
t_{CHDTH}	Direction Control Inactive Delay		30		
t_{AELCH}	Command Enable Time		40		Other: $I_{OL} = 16$ mA, $I_{OH} = -1$ mA, $C_L = 80$ pF
t_{AEHCZ}	Command Disable Time				
t_{AELCV}	Enable Delay Time	115	200		
t_{AEVNV}	$\overline{AEN}$ to DEN	–	20		
t_{CEVNV}	CEN to DEN, PDEN		25		
t_{CELRH}	CEN to Command		t_{CLML}		
t_{OLOH}	Output, Rise Time		20		From 0.8V to 2.0V
t_{OHOL}	Output, Fall Time		12		From 2.0V to 0.8V

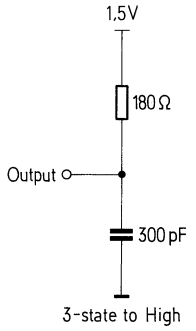
A.C. Testing Input, Output Waveform

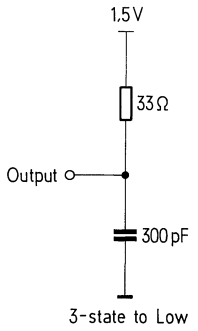
Input/Output



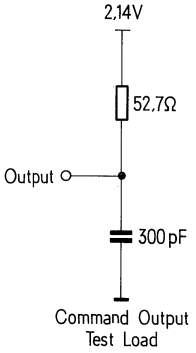
A.C. Testing Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". The clock is driven at 4.3V and 0.25V timing measurements are made at 1.5V for both a logic "1" and "0"

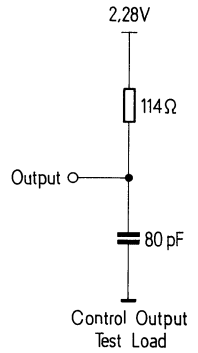
Test Load Circuits – 3-State Command Output Test Load





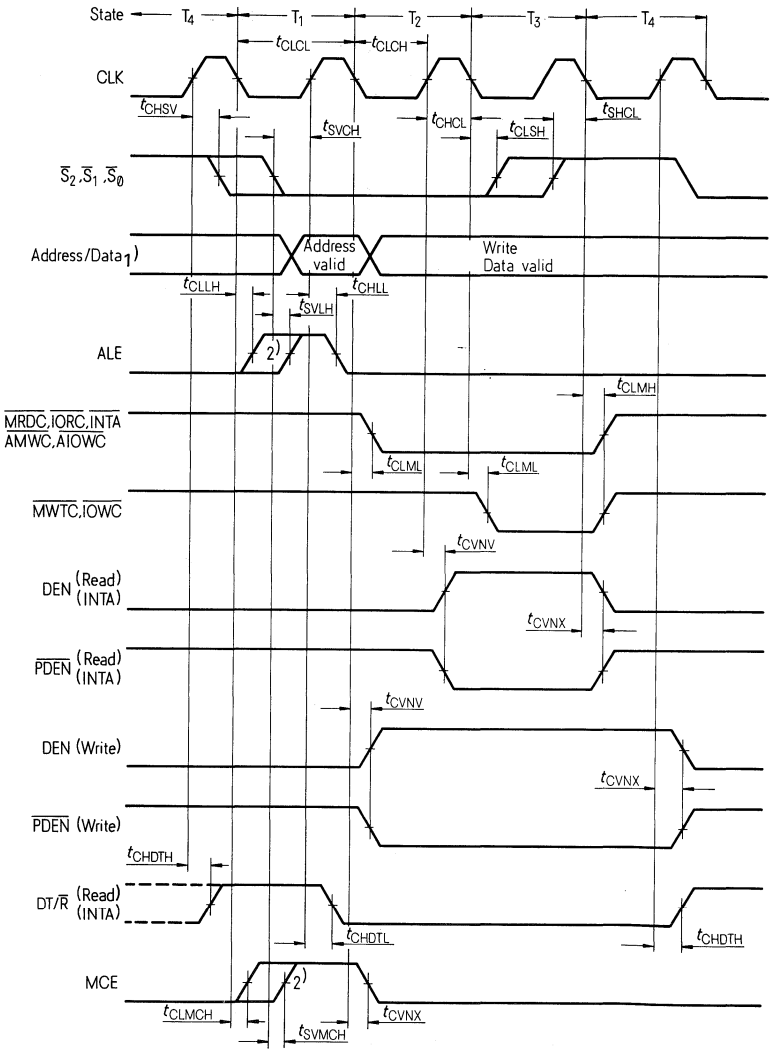
Test Load Circuits – 3-State Command Output Test Load





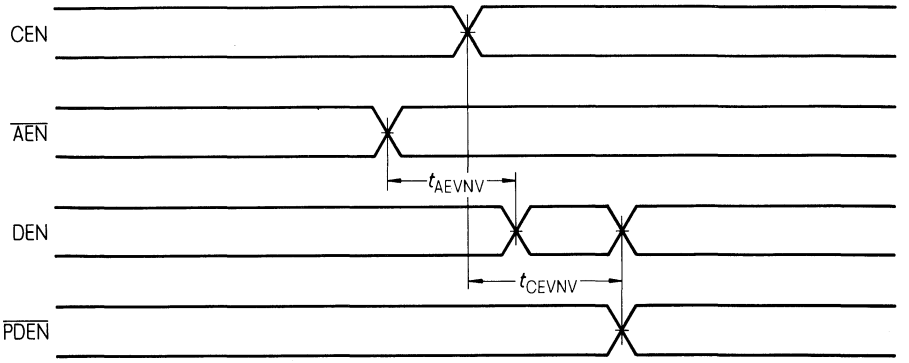
Waveforms

Timing Diagram

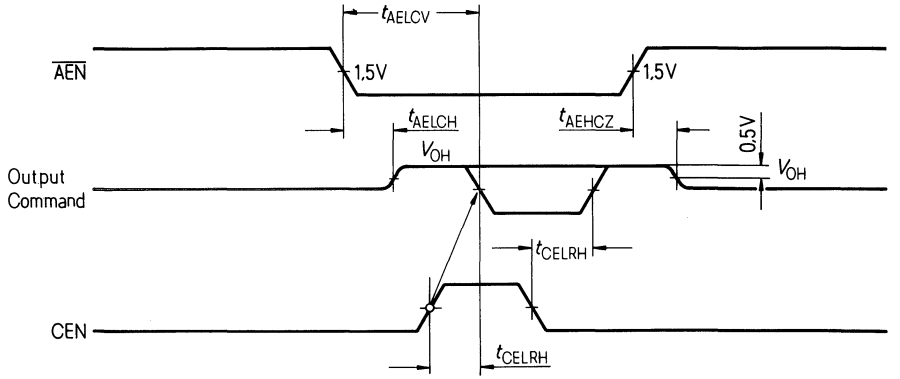


1) Address/Data Bus is shown only for reference purposes
2) Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active, whichever occurs last.
3) All timing measurements are made at 1.5V unless specified otherwise.

DEN, PDEN Qualification Timing



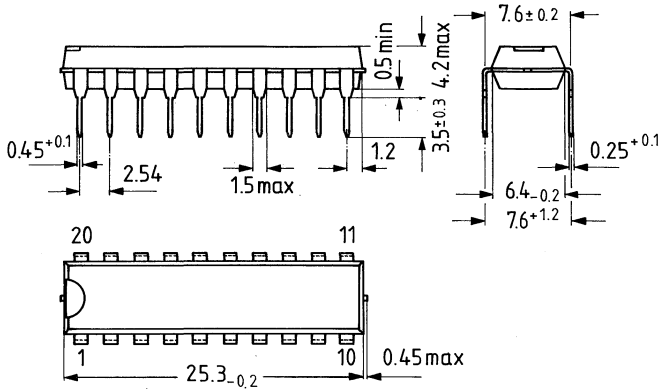
Address Enable (AEN) Timing (3-State Enable/Disable)



CEN must be low or valid prior to T2 to prevent the command from being generated.

Package Outline

20 Pin Plastic Package – Type P



Ordering Information

Type	Description	Ordering code
SAB 8288A-P	Bus Controller (plastic)	Q 67020-Y 155

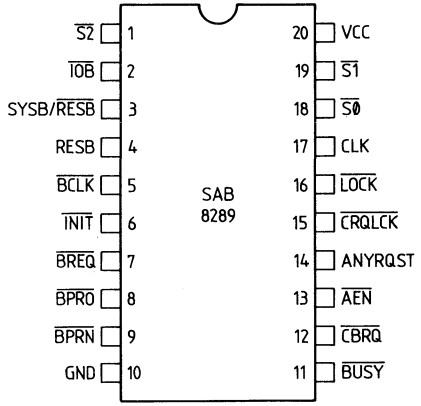
Preliminary

SAB 8289
Bus Arbiter

SAB 8289 8 MHz
SAB 8289-1 10 MHz

- Provides Multi-Master System Bus Protocol
- Synchronizes SAB 8086/SAB 8088 Processors with Multi-Master Bus
- Provides Simple Interface with SAB 8288 Bus Controller
- Four Operating Modes for Flexible System Configuration
- Compatible with Intel Bus Standard MULTIBUS™ (MULTIBUS is a trademark of INTEL Corporation USA)
- Provides System Bus Arbitration for SAB 8089 IOP in Remote Mode

Pin Configuration



Pin Names

S0-2	Status
IOB	I/O Bus Present
SYSB/RESB	System/Resident Bus
RESB	Resident Bus Present
BCLK	Bus Clock
INIT	Initialisation
BREQ	Bus Request
BPRO	Bus Priority Out
BPRN	Bus Priority In
CLK	System Clock
AEN	Address Enable
ANYRQST	Any Request
CRQLCK	Common Request Lock
CBRQ	Common Bus Request
LOCK	Bus Lock
VCC	+5 V
GND	Ground (0V)

The SAB 8289 Bus Arbiter is a 20-pin, 5-volt-only bipolar component for use with medium to large SAB 8086/SAB 8088 multi-master/multiprocessing systems. The SAB 8289 provides system bus arbitration for systems with multiple bus masters, such as an SAB 8086 CPU with SAB 8089 IOP in its REMOTE mode, while providing bipolar buffering and drive capability.

Pin Definitions and Functions

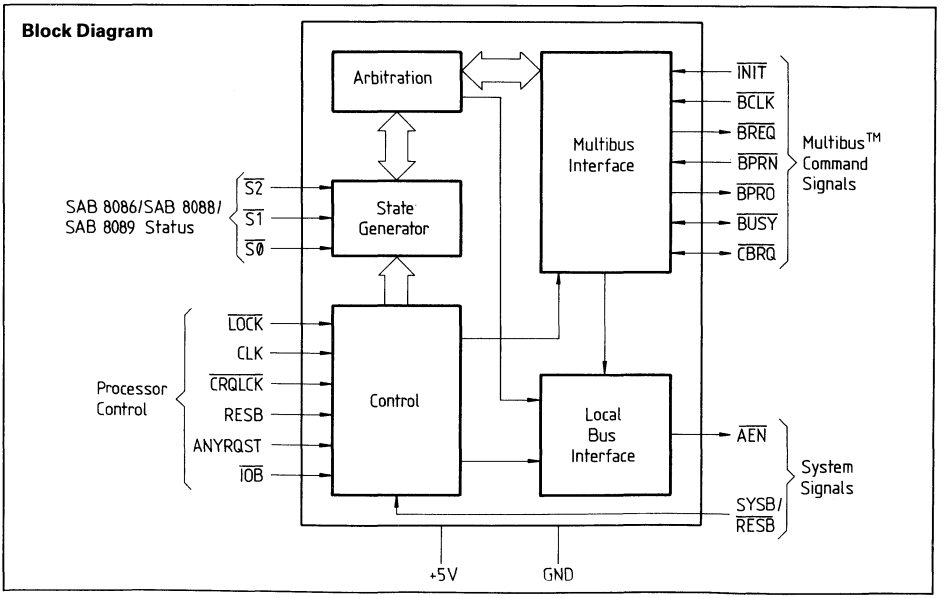
Symbol	Number	Input (I) Output (O)	Function
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	1, 18, 19	I	**Status Input Pins** These pins are the status input pins from a SAB 8086, SAB 8088 or SAB 8089 processor. The SAB 8289 decodes these pins to initiate bus request and surrender actions.
CLK	17	I	**Clock** This is the clock from the SAB 8284A clock chip and serves to establish when bus arbiter actions are initiated.
$\overline{LOCK}$	16	I	**Lock** $\overline{LOCK}$ is a processor generated signal which when activated (low) serves to prevent the arbiter from surrendering the multi-master system bus to any other bus arbiter, regardless of its priority.
$\overline{CRQLCK}$	15	I	**Common Request Lock** $\overline{CRQLCK}$ is an active low signal which serves to prevent the arbiter from surrendering the multi-master system bus to any other bus arbiter requesting the bus through the $\overline{CBRQ}$ input pin.
RESB	4	I	**Resident Bus** RESB is a strapping option to configure the arbiter to operate in systems having both a multi-master system bus and a Resident Bus. When it is strapped high the multi-master system bus is requested or surrendered as a function of the SYSB/$\overline{RESB}$ input pin. When it is strapped low the SYSB/$\overline{RESB}$ input is ignored.
ANYRQST	14	I	**Any Request** ANYRQST is a strapping option which permits the multimaster system bus to be surrendered to a lower priority arbiter as though it were an arbiter of higher priority (i.e., when a lower priority arbiter requests the use of the multi-master system bus, the bus is surrendered as soon as it is possible). Strapping $\overline{CBRQ}$ low and ANYRQST high forces the SAB 8289 arbiter to surrender the multi-master system bus after each transfer cycle. Note that when surrender occurs $\overline{BREQ}$ is driven false (high).
$\overline{IOB}$	2	I	**IO Bus** $\overline{IOB}$ is a strapping option which configures the SAB 8289 Arbiter to operate in systems having both an IO Bus (Peripheral Bus) and a multimaster system bus. The arbiter requests and surrenders the use of the multimaster system bus as a function of the status line, $\overline{S2}$. The multi-master system bus is permitted to be surrendered while the processor is performing IO commands and is requested whenever the processor performs a memory command. Interrupt cycles are assumed as coming from the peripheral bus and are treated as would be an IO command.
$\overline{AEN}$	13	O	**Address Enable** $\overline{AEN}$ is the output of the SAB 8289 Arbiter to the processor's address latches, to the SAB 8288 Bus Controller and SAB 8284A Clock Generator. $\overline{AEN}$ serves to instruct the Bus Controller and address latches when to tri-state their output drivers.

Symbol	Number	Input (I) Output (O)	Function
SYSB/$\overline{\text{RESB}}$	3	I	**System Bus/Resident Bus** SYSB/$\overline{\text{RESB}}$ is an input signal when the arbiter is configured in the S.R. Mode (RESB is strapped high) which serves to determine when the multimaster system bus is requested and when the multi-master system bus surrendering is permitted. The signal is intended to originate from some form of address mapping circuitry such as a decoder or PROM attached to the resident address bus. Signal transitions and glitches are permitted on this pin from Ø1 of T4 to Ø1 to T2 of the processor cycle. During the period from Ø1 of T2 to Ø1 of T4 only clean transitions are permitted on this pin (no glitches). If a glitch does occur the arbiter may capture or miss it, and the multi-master system bus may be requested or surrendered, depending upon the state of the glitch. The arbiter requests the multi-master system bus in the S.R. Mode when the state of the SYSB/$\overline{\text{RESB}}$ pin is high and permits the bus to be surrendered when this pin is low.
$\overline{\text{CBRQ}}$	12	I/O	**Common Bus Request** $\overline{\text{CBRQ}}$ is an input signal which serves to instruct the arbiter if there are any other arbiters of lower priority requesting the use of the multi-master system bus. The $\overline{\text{CBRQ}}$ pins (open-collector output) of all the SAB 8289 Bus Arbiters which are to surrender the multi-master-system bus upon request are connected together. The Bus Arbiter running the current transfer cycle will not itself pull the $\overline{\text{CBRQ}}$ line low. Any other arbiter connected to the $\overline{\text{CBRQ}}$ line can request the multi-master system bus. The arbiter presently running the current transfer cycle drops its $\overline{\text{BREQ}}$ signal and surrenders the bus whenever the proper surrender conditions exist. Strapping $\overline{\text{CBREQ}}$ low and ANYRQST – high allows the multi-master system bus to be surrendered after each transfer cycle. See the pin definition of ANYRQST.
$\overline{\text{INIT}}$	6	I	**Initialize** $\overline{\text{INIT}}$ is an active low multimaster system bus input signal which is used to reset all the bus arbiters on the multi-master system bus. After initialization, no arbiters have the use of the multi-master system bus.
$\overline{\text{BCLK}}$	5	I	**Bus Clock** $\overline{\text{BCLK}}$ is the multi-master system bus clock to which all multimaster system bus interface signals are synchronized.
$\overline{\text{BREQ}}$	7	0	**Bus Request** $\overline{\text{BREQ}}$ is an active low output signal in the parallel Priority Resolving Scheme which the arbiter activates to request the use of the multi-master system bus.
$\overline{\text{BPRN}}$	9	I	**Bus Priority In** $\overline{\text{BPRN}}$ is the active low signal returned to the arbiter to instruct it that it may acquire the multimaster system bus on the next falling edge of BCLK. $\overline{\text{BPRN}}$ indicates to the arbiter that it is the highest priority requesting arbiter presently on the bus. The loss of $\overline{\text{BPRN}}$ instructs the arbiter that it has loss priority to a higher priority arbiter.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
$\overline{BPRO}$	8	O	**Bus Priority Out** $\overline{BPRO}$ is an active low output signal which is used in the serial priority resolving scheme where $\overline{BPRO}$ is daisy chained to $\overline{BPRN}$ of the next lower priority arbiter.
$\overline{BUSY}$	11	I/O	**Busy** $\overline{BUSY}$ is an active low open collector multi-master system bus interface signal which is used to instruct all the arbiters on the bus when the multi-master system bus is available. When the multi-master system bus is available the highest requesting arbiter (determined by $\overline{BPRN}$) seizes the bus and pulls $\overline{BUSY}$ low to keep other arbiters off of the bus. When the arbiter is done with the bus it releases the $\overline{BUSY}$ signal permitting it to go high and thereby allowing another arbiter to acquire the multi-master system bus.
VCC	20	I	**Power Supply** (+5 V ± 10%)
GND	10	I	**Ground** (0V)

Block Diagram



Functional Description

The SAB 8289 Bus Arbiter operates in conjunction with the SAB 8288 Bus Controller to interface SAB 8086/SAB 8088/ SAB 8089 processors to a multi-master system bus (both the SAB 8086 and the SAB 8088 are configured in their max mode). The processor is unaware of the arbiter's existence and issues commands as though it has exclusive use of the system bus. If the processor does not have the use of the multi-master system bus, the arbiter prevents the Bus Controller (SAB 8288), the data transceivers and the address latches from accessing the system bus (e.g. all bus driver outputs are forced into the high impedance state). Since the command sequence was not issued by the SAB 8288, the system bus will appear as "Not Ready" and the processor will enter wait states. The processor will remain in Wait until the Bus Arbiter acquires the use of the multi-master system bus whereupon the arbiter will allow the bus controller, the data transceivers, and the address latches to access the system. Typically, once the command has been issued and a data transfer has taken place, a transfer acknowledge (XACK) is returned to the processor to indicate "READY" from the accessed slave device. The processor then completes its transfer cycle. Thus the arbiter serves to multiplex a processor (or bus master) onto a multi-master system bus and avoid contention problems between bus masters.

Arbitration between Bus Masters

In general, higher priority masters obtain the bus when a lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus. A strapping option (ANYRQST) is provided to allow the arbiter to surrender the bus to a lower priority master as though it were a master of higher priority. If there are no other bus masters requesting the bus, the arbiter maintains the bus so long as its processor has not entered the HALT State. The arbiter will not voluntarily surrender the system bus and has to be forced off by another master's bus request, the HALT State being the only exception. Additional strapping options permit other modes of operation wherein the multimaster system bus is surrendered or requested under different sets of conditions.

Modes of Operation

There are two types of processors in the SAB 8086 family. An Input/Output processor (the SAB 8089 IOP) and the SAB 8086/SAB 8088 CPUs. Consequently, there are two basic operating modes in the SAB 8289 bus arbiter. One, the $\overline{\text{IOB}}$ (I/O Peripheral Bus) mode, permits the processor access to both an I/O Peripheral Bus and a multi-master system bus. The second, the RESB (Resident Bus mode), permits the processor to communicate over both a Resident Bus and a multi-master system bus. An I/O Peripheral Bus is a bus where all devices on that bus, including memory, are treated as I/O devices and are addressed by I/O commands. All memory commands are directed to another bus, the multi-master system bus. A Resident Bus can issue both memory and I/O commands, but it is a distinct and separate bus from the multi-master system bus. The distinction is that the Resident Bus has only one master, providing full availability and being dedicated to that one master.

The $\overline{\text{IOB}}$ strapping option configures the SAB 8289 Bus Arbiter into the $\overline{\text{IOB}}$ mode and the strapping option RESB configures it into the RESB mode. It might be noted at this point that if both strapping options are strapped false, the arbiter interfaces the processor to a multi-master system bus only. With both options strapped true, the arbiter interfaces the processor to a multi-master system bus, a Resident Bus, and an I/O Bus.

In the $\overline{\text{IOB}}$ mode, the processor communicates and controls a host of peripherals over the Peripheral Bus. When the I/O Processor needs to communicate with system memory, it does so over the system memory bus.

The SAB 8086 and SAB 8088 processor can communicate with a Resident Bus and a multi-master system bus. Two bus controllers and only one Bus Arbiter would be needed in such a configuration. In such a system configuration the processor would have access to memory and peripheral of both busses. Memory mapping techniques are applied to select which bus is to be accessed. The SYSB/$\overline{\text{RESB}}$ input on the arbiter serves to instruct the arbiter as to whether or not the system bus is to be accessed. The signal connected to SYSB/$\overline{\text{RESB}}$ also enables or disables commands from one of the bus controllers.

Summary of SAB 8289 Modes, Requesting and Relinquisting the Multi-master system bus

	Status Lines From SAB 8086 / 88 / 89			IOB Mode Only	RESB (Mode) Only IOB=High RESB=High		IOB Mode RESB Mode IOB=Low RESB=High		Single Bus Mode IOB=High RESB=Low
	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	IOB=Low	SYSB/$\overline{RESB}$ =High	SYSB/$\overline{RESB}$ =Low	SYSB/$\overline{RESB}$ =High	SYSB/$\overline{RESB}$ =Low	
I/O	0	0	0	x		x	x	x	
COMMANDS	0	0	1	x		x	x	x	
	0	1	0	x		x	x	x	
HALT	0	1	1	x	x	x	x	x	x
MEM	1	0	0			x		x	
COMMANDS	1	0	1			x		x	
	1	1	0			x		x	
IDLE	1	1	1	x	x	x	x	x	x

NOTE:
x = Multi-Master System Bus is allowed to be Surrendered.

Mode	Pin Strapping	Multi-Master System Bus	
		Requested**	Surrendered*
Single Bus Multi-Master Mode	$\overline{IOB}$=High RESB=Low	Whenever the processor's status lines go active	HLT+TI•CBRQ+HPBRQ***
$\overline{RESB}$ Mode Only	$\overline{IOB}$=High RESB=High	SYSB/$\overline{RESB}$=High• ACTIVE STATUS	(SYSB/$\overline{RESB}$=Low+TI)• CRBQ+HLT+HPBRQ
IOB Mode Only	IOB=Low RESB=Low	Memory Commands	(I/O Status+TI)•CBRQ+ HLT+HPBRQ
IOB Mode•RESB Mode	$\overline{IOB}$=Low RESB=High	(Memory Command)• (SYSB/$\overline{RESB}$=High)	((I/O Status Commands)+ SYSB/RESB=LOW))•CBRQ +HPBRQ***+HLT

NOTES:
*$\overline{LOCK}$ prevents surrender of Bus to any other arbiter, $\overline{CRQLCK}$ prevents surrender of Bus to any lower priority arbiter.
**Except for HALT and Passive or IDLE Status.
***HPBRQ, Higher priority Bus request or $\overline{BPRN}$=1.
1. $\overline{IOB}$ Active Low.
2. RESB Active High.
3. +is read as "OR" and•as "AND".
4. TI=Processor Idle Status $\overline{S2}$, $\overline{S1}$, $\overline{S0}$=111
5. HLT=Processor Halt Status $\overline{S2}$, $\overline{S1}$, $\overline{S0}$=011

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	–65 to 150°C
All Output and Supply Voltages	–0.5 to 7 V
All Input Voltages	–1.0 to 5.5 V
Power Dissipation	1.5 Watt

D.C. Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ± 10%

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
V_C	Input Clamp Voltage	–	–1.0	V	V_{CC}=4.5 V, I_C=–5 mA
I_F	Input Forward Current		–0.5	mA	V_{CC}=5.5 V, V_F=0.45 V
I_R	Reverse Input Leakage Current		60	µA	V_{CC}=5.5 V, V_R=5.5 V
V_{OL}	Output Low Voltage $\overline{BUSY}$, $\overline{CBRQ}$ $\overline{AEN}$ $\overline{BPRO}$, $\overline{BREQ}$		0.45	V	I_{OL}=20 mA I_{OL}=16 mA I_{OL}=10 mA
V_{OH}	Output High Voltage $\overline{BUSY}$, $\overline{CBRQ}$	Open Collector			–
	All Other Outputs	2.4	–	V	I_{OH}=400 µA
I_{CC}	Power Supply Current	–	165	mA	–
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0	–		
C_{in} Status	Input Capacitance	–	25	pF	
C_{in} (Others)	Input Capacitance		12		

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended perods may affect device reliability.

A.C. Characteristics

T_A=0 to 70°C, V_{CC}=5 V ± 10%

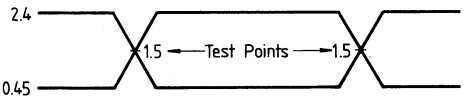
Timing Requirements

Symbol	Parameter	Limit Values				Unit	Test Condition
		SAB 8289		SAB 8289-1			
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	125	–	100	–	ns	–
TCLCH	CLK Low Time	65		53			
TCHCL	CLK High Time	35		35			
TSVCH	Status Active-Setup	65	TCLCL-10	55	TCLCL-10		
TSHCL	Status Inactive-Setup	50		45			
THVCH	Status Active Hold	10	–	10	–		
THVCL	Status Inactive Hold						
TBYSBL	Busy↑↓Setup to BCLK↓	20		20			
TCBSBL	CBRQ↑↓Setup to BCLK↓						
TBLBL	BCLK Cycle Time	100		100			
TBHCL	BCLK High Time	30	0.65 [TBLBL]	30	0.65 [TBLBL]		
TCLLL1	LOCK Inactive Hold	10	–	10	–		
TCLLL2	LOCK Active Setup	40		40			
TPNBL	BPRN↓↑ to BCLK Setup Time	15		15			
TCLSR1	SYSB/RESB Setup	0		0			
TCLSR2	SYSB/RESB Hold	20		20			
TNIH	Initialization Pulse Width	3TBLBL+ 3TCLCL		3TBLBL+ 3TCLCL			
TILIH	Input Rise Time	–	20	–	20		From 0.8 to 2.0 V
TIHIL	Input Fall Time		12		12		From 2.0 to 0.8 V

↑↓ Denotes the spec applies to both transitions of the signal.

A.C. Testing Input/Output Waveform

Input/Output



A.C. Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". The clock is driven at 4.3 V and 0.25 V. Timing measurements are made at 1.5 V for both a logic "1" and "0".

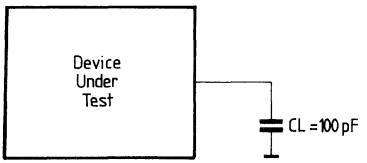
Timing Responses

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
TBLBRL	BCLK to BREQ Delay↓↑	–	35	–	–
TBLPOH	BCLK to BPRO↓↑[1]		40		
TPNPO	BPRN↓↑ to BPRO↓↑ Delay[1]		25		
TBLBYL	BCLK to BUSY Low		60		
TBLBYH	BCLK to BUSY Float[2]		35		
TCLAEH	CLK to AEN High		65	ns	
TBLAEL	BCLK to AEN Low		40		
TBLCBL	BCLK to CBRQ Low		60		
TBLCRH	BCLK to CBRQ Float[2]		35		
TOLOH	Output Rise Time		20		From 0.8 to 2.0 V
TOHOL	Output Fall Time		12		From 2.0 to 0.8 V

↓↑ Denotes the spec applies to both transitions of the signal.

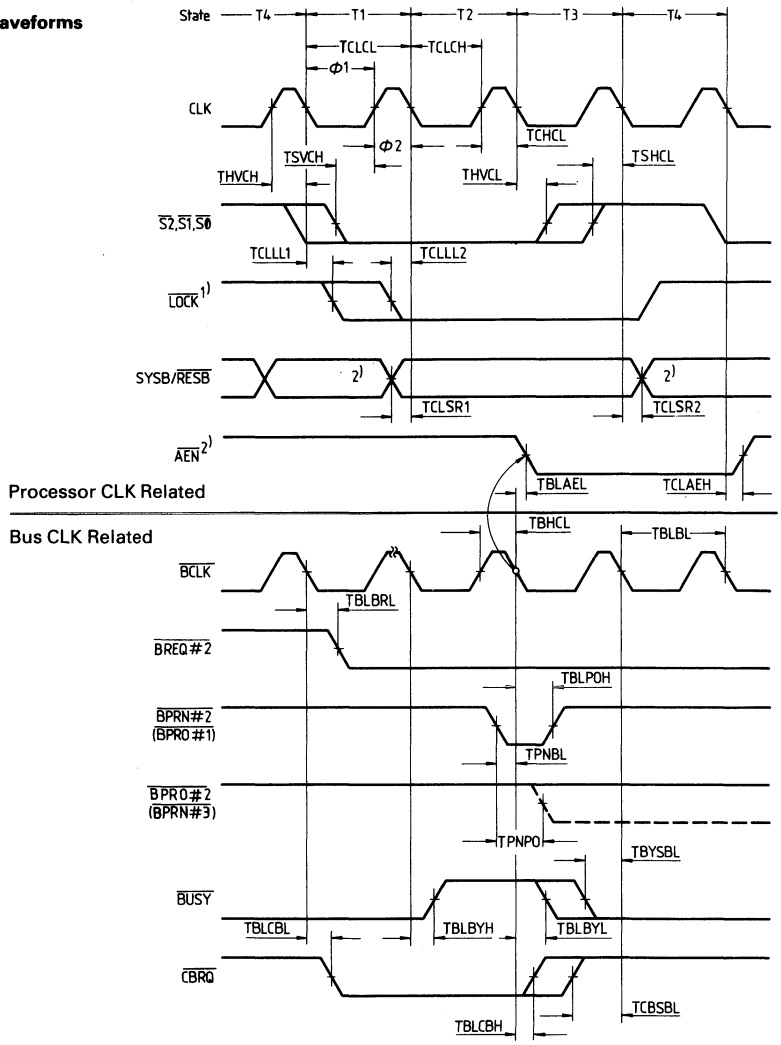
NOTES:
[1] BCLK generates the first BPRO wherein subsequent BPRO changes lower in the chain are generated through BPRON.
[2] Measured at 0.5 V above GND.

A.C. Testing Load Circuit



CL = 100 pF
CL Includes jig capacitance

Waveforms



NOTES:

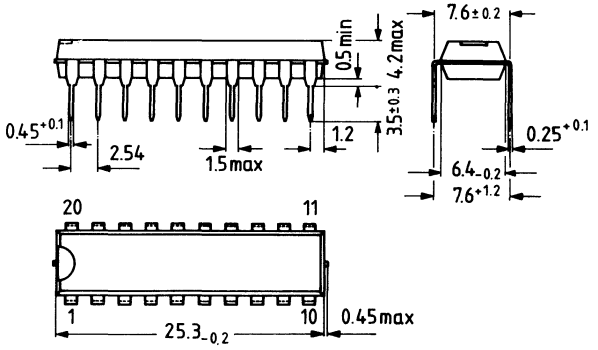
1. LOCK active can occur during any state, as long as the relationships shown above with respect to the CLK are maintained.
   LOCK inactive has not critical time and can be asynchronous.
   CRQLCK has no critical timing and is considered an asynchronous input signal.
2. Glitching of SYSB/RESB pin is permitted during this time. After I 2 of T1, and before I 1 of T4, SYSB/RESB should be stable.
3. AEN leading edge is related to BCLK, trailing edge to CLK. The trailing edge of AEN occurs after bus priority is lost.

Additional Notes:
The signals related to CLK are typical processor signals, and do not relate to the depicted sequence of events of the signals referenced to $\overline{BCLK}$. The signals shown related to the $\overline{BCLK}$ represent a hypothetical sequence of events for illustration. Assume 3 bus arbiters of priorities 1, 2 and 3 configured in serial priority resolving scheme as shown in Figure 6. Assume arbiter has the bus and is holding busy low. Arbiter #2 detects its processor wants the bus and pulls low $\overline{BREQ}$#2. If $\overline{BPRN}$#2 is high (as shown), arbiter #2 will pull low $\overline{CBRQ}$ line. $\overline{CBRQ}$ signals to the higher priority arbiter #1 that a lower priority arbiter wants the bus. [A higher priority arbiter would be granted BPRN when it makes the bus request rather than having to wait for another arbiter to release the bus through $\overline{CBRQ}$].** Arbiter #1 will relinquish the multi-master system bus when it enters a state not requiring it (see Table 1), by lowering its $\overline{BPRO}$#1 (tied to $\overline{BPRN}$#2) and releasing BUSY. Arbiter #2 now sees that it has priority from $\overline{BPRN}$#2 being low and releases CBRQ. As soon as BUSY signifies the bus is available (high), arbiter #2 pulls BUSY low on next falling edge of BCLK. Note that if arbiter #2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority arbiter by lowering its $\overline{BPRO}$#2 [TPNPO].

**Note that even a higher priority arbiter which is acquiring the bus through $\overline{BPRN}$ will momentarily drop $\overline{CBRQ}$ until it has acquired the bus.

Package Outline

20 Pin Plastic Package-Type P



Ordering Information

Component	Description	Ordering Code
SAB 8289-P	Bus-Arbiter 8 MHz (plastic)	Q67020-Y74
SAB 8289-1-P	Bus-Arbiter 10 MHz (plastic)	Q67120-Y85

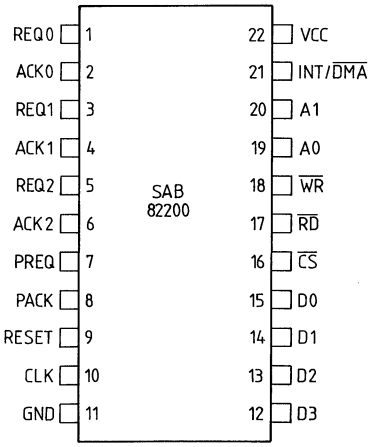
SAB 82200
Local Bus Arbiter (LBA)

DMA mode
- Arbitrates local processor bus between up to four potential bus masters (CPU plus three coprocessors)

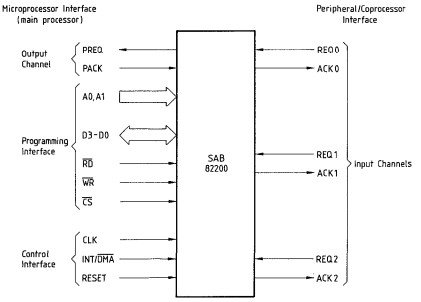
Interrupt mode
- Multiplexes up to three vectored interrupt sources to one processor interrupt channel

General features
- Flexible, programmable priority schemes
- Nested mode of operation possible
- Each input channel separately maskable
- Directly cascadable for expansion
- Glitch and race condition free operation due to synchronous logic (on-chip oscillator)

Pin Configuration



Logic Symbol



The SAB 82200 Local Bus Arbiter (LBA) is a system support component integrating functions for use in complex state-of-the-art microcomputer systems. In DMA mode it directly arbitrates the processor's local bus between the processor and up to three coprocessors, DMA controllers or peripherals with on-chip DMA controller. Easy adaption to system requirements is supported by flexible priority schemes and programmability. Arbitration for more than four bus masters is implemented by directly cascading two or more LBAs.

In interrupt mode, the LBA can be used to connect several interrupt controllers with vector capability to one processor interrupt channel without requiring compatibility with a specific cascading scheme. In interrupt mode the number of devides handled can be expanded also by cascading two or more LBAs. The flexible and programmable priority schemes are provided in this case, too.
The LBA is fabricated in high-speed ASBC technology and comes in a 22-pin plastic package.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
REQ 0 – REQ 2	1, 3, 5	I	REQUEST (0 TO 2) Are the request inputs of the three input channels. A pending request must be active until it is acknowledged by the corresponding ACKn signal. Otherwise the PREQ output may glitch. The request inputs are sampled by the internal clock.
ACK 0 – ACK 2	2, 4, 6	O	ACKNOWLEDGE (0 TO 2) Are the acknowledge outputs of the input channels. The acknowledge output of the highest-priority non-masked channel with pending request is activated when PACK becomes active. The acknowledge outputs are glitch-free.
PREQ	7	O	PROCESSOR REQUEST This output is activated whenever there is a pending non-masked request on any of the request inputs. The processor request output is glitch-free if the request inputs REQn meet certain requirements.
PACK	8	I	PROCESSOR ACKNOWLEDGE The acknowledging signal for a request on PREQ is expected at this input. When the acknowledge input is activated the acknowledge output of the highest-priority channel with pending request is set high. Which channel is serviced first is decided on the rising edge of PACK (DMA mode) or on the first falling edge of PACK (interrupt mode).
RESET	9	I	RESET A high on this input sets the device into initial state.
CLK	10	I	CLOCK The CLOCK input should be connected to the bus clock of the arbitrated bus. CLK is used as timing reference only to prevent e.g. deadlock situations.
D0 – D3	12 – 15	I/O	DATA (0 TO 3) Control and status information is transferred on these bidirectional lines.
$\overline{CS}$	16	I	$\overline{CHIP\ SELECT}$ A low on this input enables read/write communication via D0 to D3 with the register selected by A0, A1.
$\overline{RD}$	17	I	READ CONTROL If $\overline{CS}$ is low, a low on this input gates the contents of the selected register (A0, A1) to D0 to D3.
$\overline{WR}$	18	I	WRITE CONTROL If $\overline{CS}$ is low, a low on this input latches the data from D0 to D3 into the selected (A0, A1) register.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
A0, A1	19, 20	I	ADDRESS LINE (0, 1) These inputs select the internal registers while $\overline{CS}$ is active.
INT/$\overline{DMA}$	21	I	INTERRUPT/DMA MODE This is a static operating mode strapping input. If tied low the DMA mode is selected; if high the interrupt mode is selected.
GND	11		GROUND (0V)
VCC	22		POWER SUPPLY (+5V)

Functional Description

Basic Operating Modes

The LBA has two basic operating modes
– DMA mode and
– interrupt mode.

In DMA mode the LBA is configured to handle HOLD/HLDA lines, in interrupt mode to handle INT/$\overline{\text{INTA}}$ lines.

In interrupt mode, the channel acknowledge lines exactly follow the actions on the processor acknowledge line PACK, whereas in DMA mode this is not necessarily the case.

Channel Priority

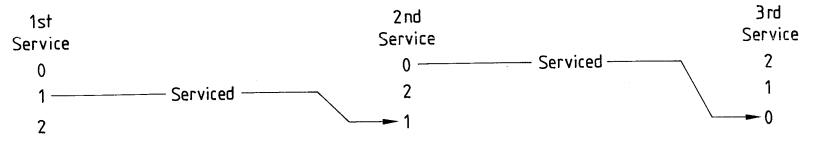
The decision which channel is acknowledged when the processor activates PACK depends on the priority of the channels. Two priority modes are programmable:

- Fixed priority
  Channel 0 has highest, channel 2 lowest priority.
- Full rotating priority
  In the beginning the priority scheme is the same as with fixed priority. The last channel serviced becomes the channel of lowest priority with the others shifted accordingly (see figure 1).

The resulting new channel priorities are assigned at the end of the acknowledge cycle performed on the serviced channel.

The priority modes are programmed via the command register.

Figure 1
Rotating Priority Scheme



Channel Service

DMA Mode

The DMA mode is selected by connecting pin INT/$\overline{\text{DMA}}$ to ground. In DMA mode the LBA is intended to handle HOLD/HLDA signal pairs.

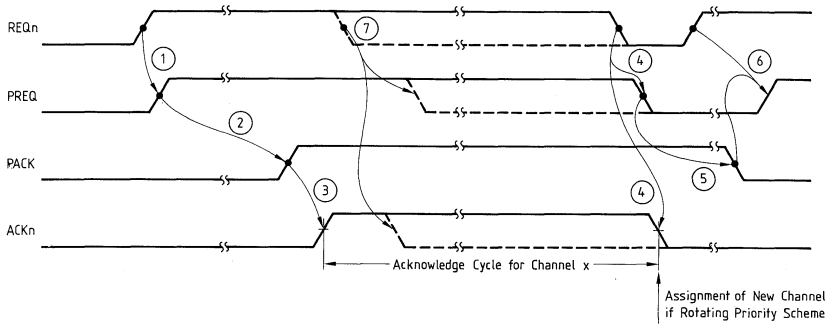
Single-channel operation

If the request line of an enabled channel is activated and no other channel is active at that time, the processor request line PREQ is set active high.

When the processor has relinquished control of the bus it must activate the PACK signal.

This causes the appropriate channel acknowledge signal to be activated (see figure 2). If the rotating priority scheme is selected, the new channel priorities are assigned at the end of the channel acknowledge cycle (falling edge of ACKn).

Figure 2
DMA Mode, Single-Channel Operation



① Activation of request input directly activates PREQ.
② When the processor has released the bus it activates PACK.
③ This acknowledge is immediately passed to the channel output ACKn.
④, ⑤ When the peripheral has finished its transfers, it deactivates the request. This causes PREQ and ACKn also to be deactivated and the processor can gain the control over the bus again.
⑥ A request activated in the time frame between deactivation of PREQ and PACK is processed only after the deactivation of PACK.
⑦ If REQn is deactivated ACKn is deactivated immediately, too. (No minimum ACKn high time).

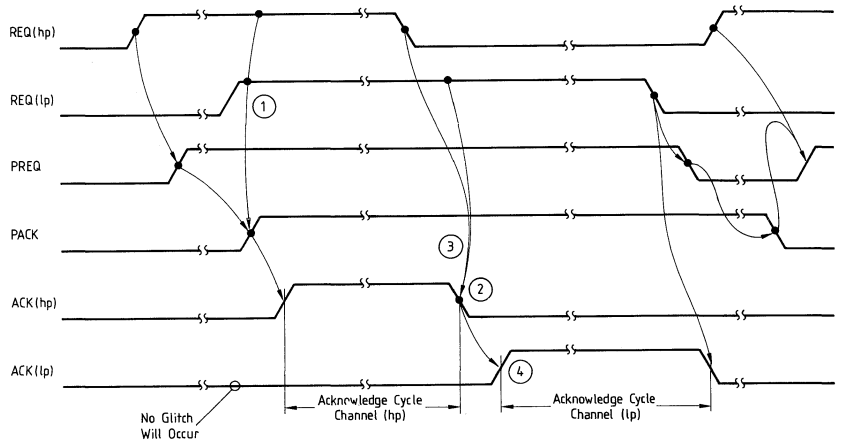
Multiple channel operation

- Non-nested mode

If there is more than one request pending when the processor releases the bus, the highest priority request is acknowledged (see figure 3).

If the rotating priority scheme is selected, the new channel priorities are assigned at the end of the acknowledge cycle of the highest priority request. When this acknowledge cycle is finished, the now highest priority request is acknowledged. This sequence will be continued as long as non-masked requests are pending.

Figure 3
DMA Mode, Multiple Channel Operation, Non-Nested Mode



① With the rising edge of PACK the highest priority request is acknowledged.
② With the falling edge of channel acknowledge ACK (hp) the new channel priorities are assigned if rotating priority is enabled.
③ With the falling edge of the highest priority acknowledge the pending request with the currently (new) highest priority is acknowledged.
④ The new channel priorities assigned if rotating priority is selected.

hp = highest priority
lp = lowest priority

If there is already an active channel the new request will be acknowledged as soon as it becomes the highest priority request. The active channel will not be interrupted if the new request has higher priority as the active one.

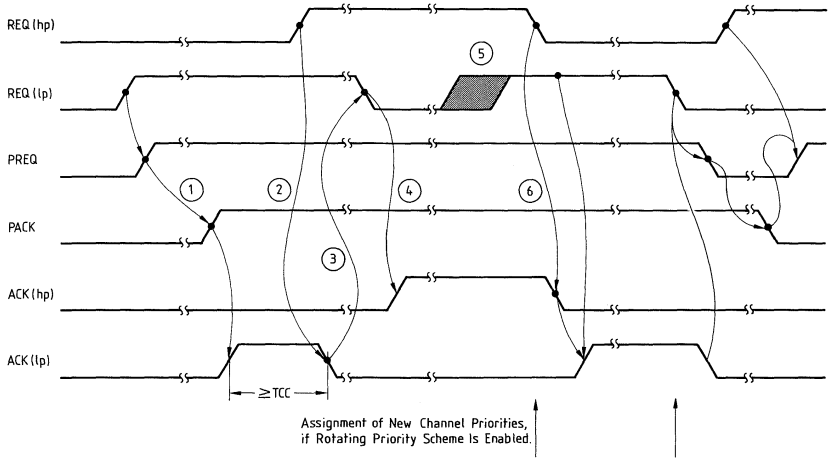
- Nested mode

In nested mode, a higher priority request can interrupt a lower priority channel. This is done by deactivating the peripheral acknowledge line. Most DMA controllers and peripherals with integrated DMA controllers release the bus and drop the request line when their DMA acknowledge input is deactivated. Thus a higher priority bus master can gain control over the bus (see figure 4).

To avoid deadlock situations an activated ACK line has to stay active until the coprocessor has recognized this activation. Therefore, the minimum time frame within which an activated ACK line remains in the high state is programmable from 1 to 4 CLK cycles.

If the rotating priority scheme is enabled, the assignment of the new channel priorities in nested mode is done upon deactivation of a request that has not been disrupted by a higher priority channel.

Figure 4
DMA Mode, Multiple Channel Operation, Nested Mode



① A lower priority peripheral gets control of the bus.
② A higher priority request causes the LBA to drop the lower priority acknowledge.
③ The peripheral releases the bus and drops the request line.
④ Now the higher priority request can be acknowledged.
⑤ The disrupted peripheral normally raises its request line again to continue.
⑥ After the higher priority peripheral has finished, the now highest priority request is processed.

To avoid deadlock situations an acknowledge has to remain in high state for a minimum time frame. This time programmable from 1 to 4 CLK cycles.

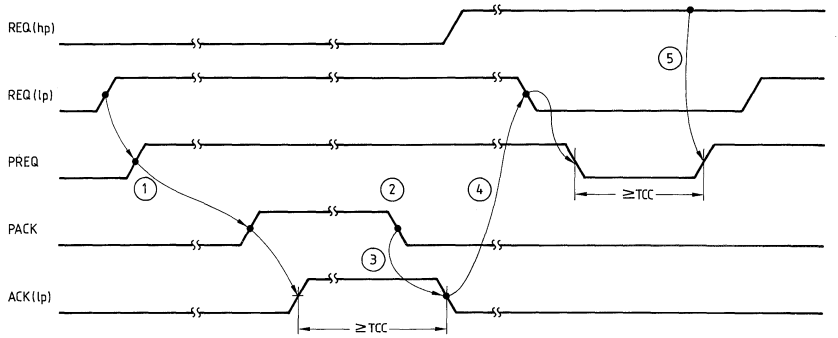
hp = highest priority
lp = lowest priority

- Premature deactivation of PACK

An active channel can be stopped by the premature deactivation of PACK, too. For each channel this PACK stop feature can be individually enabled or disabled via the PACK channel control register.

If the PACK stop is enabled for a channel and this channel is active, its ACK line is dropped when the PACK line goes inactive (see figure 5).

Figure 5
Premature Deactivation of PACK



① A peripheral gets control of the bus.
② Another (higher-priority) bus master needs the bus – PACK is deactivated.
③ If the PACK channel control is enabled the channel acknowledge line is deactivated. A minimum high time of TCC is guaranteed.
④ This causes the peripheral to release the bus.
⑤ Subsequent requests are processed only after PREQ was inactive for a certain amount of time to ensure proper synchronization.
hp = highest priority
lp = lowest priority

After the peripheral has dropped its request the PREQ output is deactivated to signal the release of the bus.

A subsequent channel request, occurring in the time frame between the deactivation of PACK and PREQ, is processed only after the PREQ output has been inactive for a certain amount of time. This time TCC is programmable from 1 to 4 CLK cycles.

If the active channel has disabled the premature deactivation, the PREQ output will go inactive after the request is deactivated.

Interrupt Mode

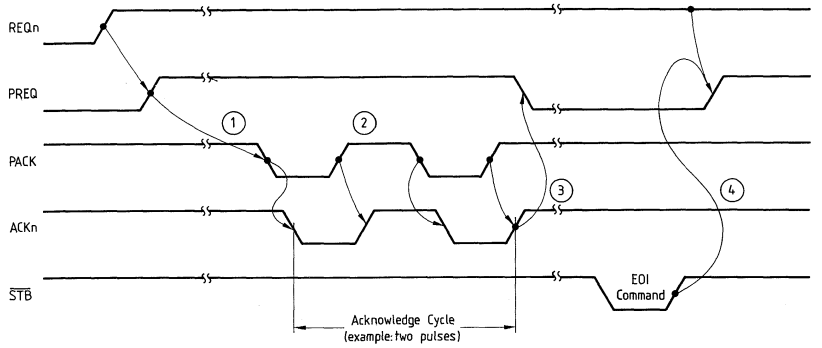
The interrupt mode is selected by connecting pin INT/$\overline{\text{DMA}}$ to VCC. In interrupt mode the LBA is intended to handle INT/$\overline{\text{INTA}}$ signal pairs.

Single-channel operation

If the request line of an enabled channel is activated the processor request line PREQ is immediately set to active high. When the processor acknowledges the interrupt request with the interrupt acknowledge pulse(s) on PACK they are immediately passed to the channel with the pending request (see figure 6).

During the acknowledge cycle no other requests are accepted. The acknowledge cycle lasts from the beginning of the first acknowledge pulse to the end of the last pulse. The number of pulses within on acknowledge cycle is programmable.

Figure 6
Interrupt Mode, Single-Channel Operation



① A request at one of the request inputs is passed to the CPU via PREQ.
② This causes the CPU to respond with an interrupt acknowledge cycle consisting of one or more $\overline{\text{INTA}}$ pulses.
③ At the end of the acknowledge cycle the PREQ output is deactivated regardless of the state of the request input (the related bit in the in-service register ISR is set).
④ After getting an EOI (end of interrupt) command for this channel (bit in ISR is reset) further requests on this channel are reenabled.

If no request is pending when the acknowledge cycle starts (premature deactivation of request), the acknowledge pulse(s) on PACK will not be passed to an output channel. If the request is deactivated while an acknowledge cycle is running, the cycle is aborted immediately on the peripheral channel (i.e. ACKn glitches are possible in this case).

At the end of the acknowledge cycle (rising edge of last pulse), the PREQ output is deactivated and the serviced channel is disabled by setting the related bit in the in-service register ISR.

Further requests on this channel are processed only after this bit has been reset by an EOI command.

Multiple channel operation

- Non nested mode

In the non-nested mode every enabled request is transferred to the processor regardless of the priority.

The priority scheme only decides which request is processed first if more than one request is active at the falling edge of the first pulse on PACK (see figure 7).

Every acknowledged request is disabled until it is reenabled by a specific EOI command defining which channel has to be reenabled. Thus a dynamic channel priority scheme can be implemented by software.

If the rotating priority scheme is selected, the new channel priorities are assigned at the end of each acknowledge cycle.

- Nested Mode

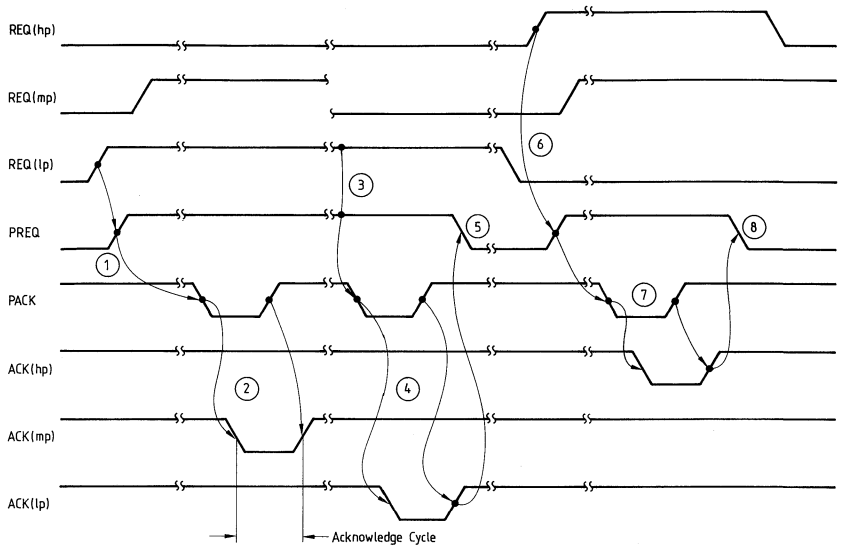
In the nested mode a request is transferred only if it is the currently highest-priority non-masked request and no higher priority request is being serviced. This means, that if more than one request is pending at the beginning of the acknowledge cycle only the highest priority request is serviced. The other request(s) is serviced only after the in-service bit of this request has been reset by an EOI command.

If a subsequent request has a higher priority than the highest request that is currently in-service, it will be transferred to the CPU (see figure 8).

In general, each request is masked by the in-service bits set related to its own level and of higher levels. The in-service bits can be reset by a non-specific EOI command (the highest priority bit that is set will be reset) or a specific EOI command (the bit specified in the command is reset).

In case of nested-mode fixed priority is automatically selected, no rotating priority is possible.

Figure 7
Interrupt Mode, Multiple Channel Operating, Non-Nested Mode

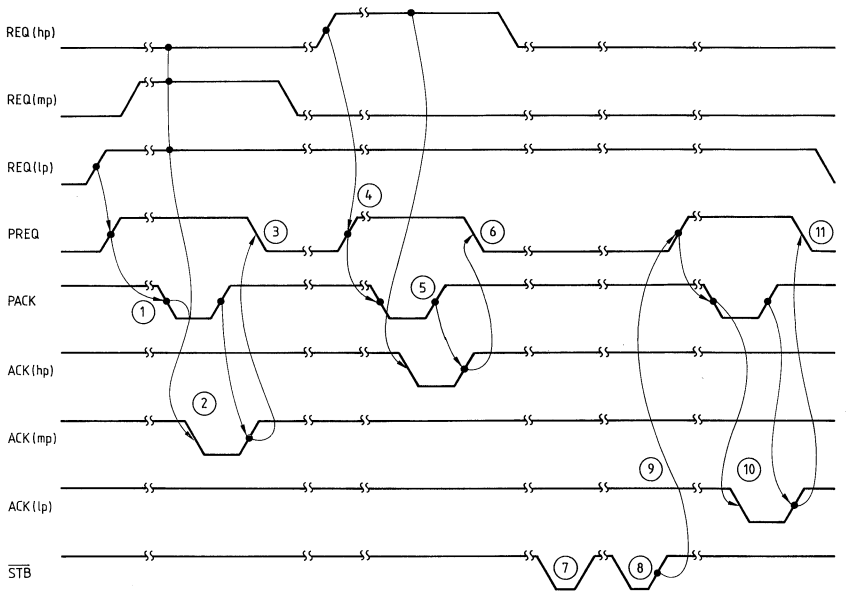


Assumtions: all request inputs enabled, 1 pulse acknowledge cycle, fixed priority.

① A pending request is passed to the CPU.
② The request with the highest priority at the beginning of the acknowledge cycle (falling edge of PACK) is serviced.
③ PREQ stays in active state because another unmasked, unacknowledged request is pending.
④ The second request is acknowledged.
⑤ PREQ is deactivated because no unmasked request is pending. REQ (lp) is masked via its in-service bit.
⑥, ⑦ REQ (hp) is transferred to the CPU and acknowledged.
⑧ PREQ goes inactive regardless of the pending request REQ (mp) because its still masked via its in-service bit. Further requests will be processed only when the appropriate in-service bits will be reset by a specific EOI command.

hp = highest priority
mp = medium priority
lp = lowest priority

Figure 8
Interrupt Mode, Multiple Channel Operation, Nested Mode



Assume fixed priority,channels enabled.

① A request at REQ (lp) is passed to the CPU.
② The acknowledge signal from the CPU is passed to the highest priority request pending (REQ (mp)).
③ PREQ is deactivated because no request with higher priority than the highest in-service request is pending.
④ REQ (hp) is passed to the CPU because it has higher priority than the highest in-service request.
⑤ The request is acknowledged.
⑥ PREQ is deactivated (see ④).
⑦ EOI command for highest priority level is issued.
⑧ EOI command for medium priority level is issued.
⑨ No higher request than REQ (lp) is being serviced or pending thus it is passed to the processor.
⑩ The request is acknowledged.
⑪ PREQ is deactivated because no unserviced request is pending.

hp = highest priority
mp = medium priority
lp = lowest priority

$\overline{\text{INTA}}$ cycle conversion mode

For easy connection of interrupt vector sources requiring only one $\overline{\text{INTA}}$ pulse with processors that issue two $\overline{\text{INTA}}$ pulses, the LBA can be set into the $\overline{\text{INTA}}$ cycle conversion mode.

In this mode the first of the two $\overline{\text{INTA}}$ pulses on PACK is suppressed when passed to channel 1 or channel 2. Only the second pulse (related to the transfer of the interrupt vector) is passed to ACK1 or ACK2.

However, both $\overline{\text{INTA}}$ pulses will be issued on channel 0 in order to still have the possibility of connecting standard interrupt controllers or of cascading LBAs in this mode.

Cascading SAB 82200 Local Bus Arbiters

Two or more LBAs can easily be cascaded by connecting the PREQ/PACK lines to an input channel of another LBA.

In DMA mode, this daisy chaining has only effect on the response time. In interrupt mode, the skew between the request pulses ($\overline{INTA}$ pulses) and the associated data (cascade information, interrupt vector) limits the number of cascaded LBAs.

The nested DMA mode is supported by the possibility of deactivating an active channel if PACK is lost.

Programming the SAB 82200 Local Bus Arbiter

The LBA contains several registers that allow software control of most of the LBA's functions:

Write Registers	Read Registers
1) Command Register	1) Command Register
2) Channel Mask Register	2) Channel Mask Register
3) Channel Control Register (DMA mode only)	3) Channel Control Register (DMA mode only)
End-of-Interrupt Register (interrupt mode only)	In-service Status Register (interrupt mode only)
	4) Request Status Register

The basic operating modes are defined using the command register; with the channel mask register each of the three channels can be disabled separately.

The third register has a different meaning for interrupt mode and for DMA mode. In interrupt mode it is used for EOI commands, in DMA mode as control register to enable and disable the premature channel deactivation via PACK.

The read registers show the status of the device: the programming; which requests are pending; which channels are enabled (DMA mode); and which request levels are just in-service (interrupt mode). The following sections detail the registers separately for DMA mode and interrupt mode.

Programming in DMA Mode

The DMA mode of the LBA is selected by connecting the INT/$\overline{DMA}$ input to ground. The following tables show the register definitions for DMA mode.

Register selection

The LBA registers in DMA mode are accessed according to the following table:

$\overline{CS}$	A1	A0	$\overline{RD}$	$\overline{WR}$	Register
0	0	0	1	0	Command Register
0	0	1	1	0	Channel Mask Register
0	1	0	1	0	Channel Control Register
0	1	1	1	0	Reserved
0	0	0	0	1	Command Register
0	0	1	0	1	Channel Mask Register
0	1	0	0	1	Channel Control Register
0	1	1	0	1	Request Status Register
1	X	X	X	X	No Access

Command register (CR)

The operating mode of the LBA is defined with the command register.

D3	D2	D1	D0
C1	C0	NNM	PM

- **PM: Priority mode**

PM = 0: Fixed priority
PM = 1: Rotating priority

- **NNM: Non-nested mode enable**

NNM = 0: Nested mode
NNM = 1: Non-nested mode

- **C1, C0: Cycle count value**

These bits define the value of the timing parameter TCC.

C1	C0	Length of TCC
0	0	2 CLK Cycles
0	1	4 CLK Cycles
1	0	1 CLK Cycles
1	1	3 CLK Cycles

Channel mask register (CMR)

Each channel can be enabled and disabled separately using the channel mask register.

D3	D2	D1	D0
DISC	DIS2	DIS1	DIS0

- **DISn: Channel enable/disable**

DISn = 0: Channel n enabled
DISn = 1: Channel n disabled

- **DISC: Disable chip**

DISC = 0: The channels are enabled or disabled according to D0–D2.
DISC = 1: All channels are disabled, regardless of the status of D0–D2.

Channel control register (CCR)

The premature deactivation of the channel upon the premature deactivation of PACK can be enabled or disabled separately using the channel control register.

D3	D2	D1	D0
0	PCC2	PCC1	PCC0

- **PCCn: PACK channel control for channel n**

PCCn = 0: PACK channel control for channel n is enabled.
PCCn = 1: PACK channel control for channel n is disabled.

Request status register (RSR)

Reading the request status register gates the physical state of the request inputs onto the data lines.

D3	D2	D1	D0
X	REQ2	REQ1	REQ0

REQn = 0: Low input level on pin REQn
REQn = 1: High input level on pin REQn

Reading the channel mask and channel control registers

On reading these registers the contents of the selected register is gated onto the data bus.

Programming in Interrupt Mode

The interrupt mode of the LBA is selected by connecting the INT/$\overline{DMA}$ input to VCC.
The following tables show the register definitions for the interrupt mode.

Register selection

The LBA registers are accessed according to the following table:

$\overline{CS}$	A1	A0	$\overline{RD}$	$\overline{WR}$	Register
0	0	0	1	0	Command Register
0	0	1	1	0	Channel Mask Register
0	1	0	1	0	End-of-Interrupt Register
0	1	1	1	0	– Reserved –
0	0	0	0	1	Command Register
0	0	1	0	1	Channel Mask Register
0	1	0	0	1	In-Service Register
0	1	1	0	1	Request Status Register
1	X	X	X	X	No Access

Command register

The operating mode of the LBA is defined with the command register.

D3	D2	D1	D0
C1	C0	NNM	PM

PM: Priority mode
NNM: Non-nested mode

NNM	PM	Mode
0	X	Nested Mode, Fixed Priority
1	0	Non-Nested, Fixed Priority
1	1	Non-Nested, Rotating Priority

- **C1, C0: Acknowledge cycle definition**

These bits define the number of the processor interrupt acknowledge pulses on PACK and the number of acknowledge pulses on ACKn. In the case of reduction in pulse count the first pulse of PACK is suppressed.

C1	C0	Processor Acknowledge Cycle Count	Peripheral Acknowledge
0	0	PACK: 2	ACKn: 2[1)]
1	0	PACK: 1	ACKn: 1
0	1	PACK: 2	ACK0: 2 ACK1,2: 1
1	1	PACK: 2	ACKn: 1

[1)] Default after reset

Channel mask register

Each channel can be enabled and disabled separately using the channel mask register.

DISC	D2	D1	D0
DISC	DIS2	DIS1	DIS0

- **DISn: Channel enable/disable**

DISn = 0: Channel n enabled
DISn = 1: Channel n disabled

- **DISC: Disable chip**

DISC = 0: The channels are enabled or disabled according to D0–D2.
DISC = 1: All channels are disabled regardless of the status of D0–D2.

End-of-interrupt register

The end-of-interrupt (EOI) register is required to reset the in-service bits of the different channels.

D3	D2	D1	D0
RHPI	RIS2	RIS1	RIS0

- **RISn: Reset in-service bit n**

RHPI	RIS2	RIS1	RIS0	Action	Type
0	0	0	1	Reset In-Service Bit 0	Specific EOI Commands
0	0	1	0	Reset In-Service Bit 1	
0	1	0	0	Reset In-Service Bit 2	
1	x	x	x	Reset Highest Priority In-Service Bit that Is Set	Non-Specific EOI Command

If no in-service bit is set in the in-service register, a write operation to the EOI register is like a NOP.
If non-nested mode is programmed, a non-specific EOI acts like a NOP.
If the RHPI bit is set, setting of RISn bits has no effect.

Request status register

Reading the request status register gates the physical state of the request inputs onto the data bus.

D3	D2	D1	D0
X	REQ2	REQ1	REQ0

REQn = 0: Low input level on pin REQn
REQn = 1: High input level on pin REQn

In-service status register

Reading the in-service status register gates the state of the in-service bits onto the data bus.

D3	D2	D1	D0
X	ISB2	ISB1	ISB0

- **ISBn: In-service bit n**

ISBn = 0: Channel n is not being serviced
ISBn = 1: Channel n is serviced (a request has been acknowledged and no EOI command for this channel has been given yet)

Reading the command and channel mask register

On reading these registers the content of the selected register is gated onto the data bus D0–D3.

Reset

A high level on the RESET input sets the LBA into a defined state.
In the **DMA mode** this initial state is:

- all channels enabled
- fixed priority
- non-nested mode
- premature channel deactivation via PACK disabled
- TCC = 2 CLK cycles
- PREQ line inactive

In **interrupt mode** the initial state is:

- all channels enabled
- fixed priority
- nested mode
- acknowledge cycle length is two pulses
- PREQ line inactive

If this initial state is applicable no further programming is necessary.

Circuit Examples

Figures 9 and 10 show two possible applications

Figure 9

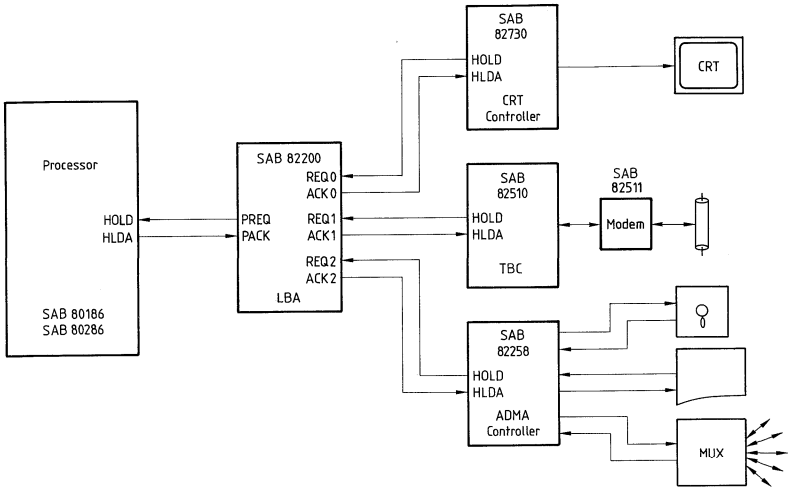
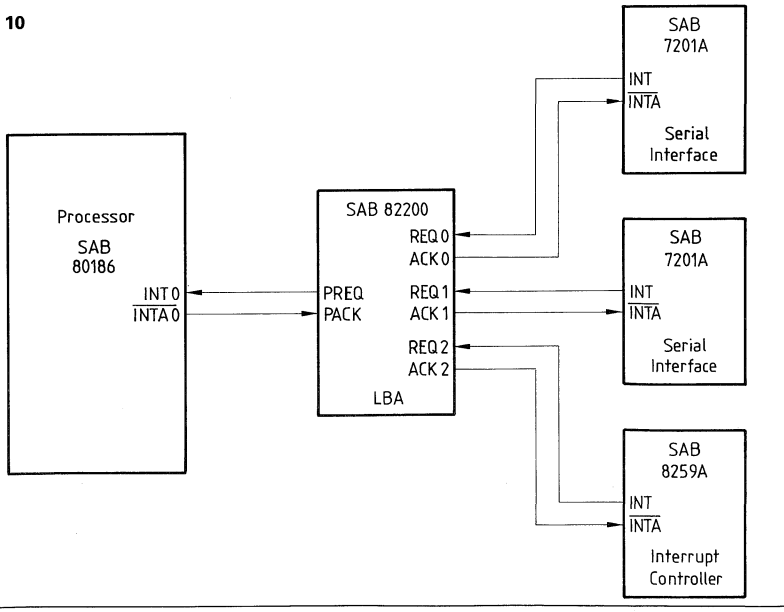


Figure 10



Absolute Maximum Ratings[1)]

Temperature under bias	0 to +70°C
Storage temperature	−65 to +125°C
All output and supply voltages	−0.5 to +7V
All input voltages	−1.0 to +5.5V
Power dissipation	1W

DC Characteristics

TA = 0 to 70°C, VCC = +5V ±10%

Symbol	Parameter	Limit values		Unit	Test Conditions
		min.	max.		
VC	Input clamp voltage	–	−1	V	IC = −5 mA
ICC	Power supply current	–	145	mA	VCC = 5.5 V, all outputs open; TA = 25°C
IF	Forward input current	–	−0.2	mA	VF = 0.45 V
IR	Reverse input current	–	50	µA	VR = VCC
VOL	Output low voltage, D0–D3 other outputs	–	0.45	V	IOL=32 mA, CL=300 pF IOL=10 mA, CL=100 pF
VOH	Output high voltage, D0–D3 other outputs	2.4	–	V	IOH=–5 mA, CL=300 pF IOH=–1 mA, CL=100 pF
IOFF	Output off current	–	±50	µA	VOFF = 0.45 to VCC
VIL	Input low voltage	–	0.8	V	–
VIH	Input high voltage	2.0	–	V	–
CIN	Input capacitance	–	12	pF	f = 1 MHZ VBIAS=2.5 V, VCC=5 V TA = 25°C
CIO	Input/output capacitance	–	20	pF	f = 1 MHz VBIAS=2.5 V, VCC=5 V TA = 25°C

[1)] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics

TA = 0 to 70°C, VCC = +5V ±10%

Symbol	Parameter	Limit values		Unit
		min.	max.	
t1	$\overline{RD}$ or $\overline{WR}$ pulse width	100	–	ns
t2	Address and $\overline{CS}$ setup time to $\overline{RD}$ ↓ or $\overline{WR}$ ↓	10	–	ns
t3	Address and $\overline{CS}$ hold time after $\overline{RD}$ ↑ or $\overline{WR}$ ↑	0	–	ns
t4	Data setup time to $\overline{WR}$ ↑	50	–	ns
t5	Data hold time after $\overline{WR}$ ↑	10	–	ns
t6	Data valid after $\overline{RD}$ ↓	–	60	ns
t7	Data bus active after $\overline{RD}$ ↓	20	–	ns
t8	Request setup time for recognition as highest priority request	100	–	ns
t9	PACK ↓ (premature) till ACK(n) ↓	–	150	ns
t10	Data valid after $\overline{RD}$ ↑	10	–	ns
t11	Data bus inactive after $\overline{RD}$ ↑	–	60	ns
t12	REQn ↑ to PREQ ↑	–	180	ns
t13	PACK ↑ to ACKn ↑ (DMA mode)	–	170	ns
t14	ACKn high time (DMA mode)	[1]	–	ns
t15	REQ(hp) ↑ to ACK(lp) ↓ (DMA mode)	–	270	ns
t16	REQ(lp) ↓ to ACK(hp) ↑ (DMA mode)	–	180	ns
t17	REQn low time (DMA mode)	250	–	ns
t18	REQn ↓ to ACKn ↓ (DMA mode)	–	240	ns
t19	REQ(hp) ↓ to ACK(lp) ↑ (DMA mode)	120	290	ns
t20	REQn ↓ to PREQ ↑ (DMA mode)	–	160	ns
t21	PACK ↓ to PREQ ↑ again (request pending)	45	210	ns
t22	PACK ↓ to ACKn ↓ (interrupt mode)	–	55	ns
t23	PACK low time (interrupt mode)	50	–	ns
t24	PACK ↑ to ACKn ↑ (interrupt mode)	–	50	ns
t25	End of acknowledge cycle (ACKn ↑) to PREQ ↓	–	100	ns
t26	EOI command ($\overline{WR}$ ↑) to PREQ ↑ again (request pending, interrupt mode)	–	110	ns

[1] TCC is programmable from 1 to 4 CLK cycles.

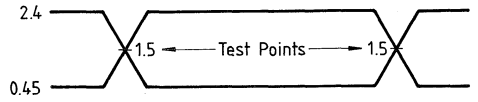
AC Characteristics (cont'd)

Symbol	Parameter	Limit values		Unit
		min.	max.	
t27	CLK cycle time	50	–	ns
t28	CLK high time	20	–	ns
t29	CLK low time	20	–	ns
t30	RESET high time	200	–	ns
t31	PREQ minimum low time (DMA mode)	[1]	–	ns
t32	PACK minimum high time (interrupt mode)	70	–	ns
t33	Minimum time interval between two active acknowledge outputs	15	–	ns
t34	Processor acknowledge minimum high time (DMA mode)	100	–	ns
t35	PREQ ↑ to PACK ↓ (interrupt mode)	200	–	ns
t36	REQn minimum high time for recognition	100	–	ns
t37	PACK minimum high time between different cycles	270	–	ns

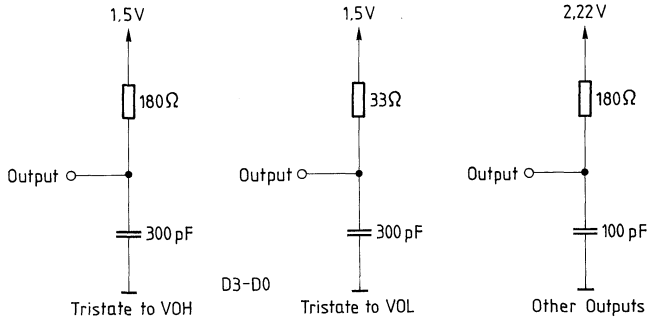
[1] TCC is programmable from 1 to 4 CLK cycles.

Waveforms

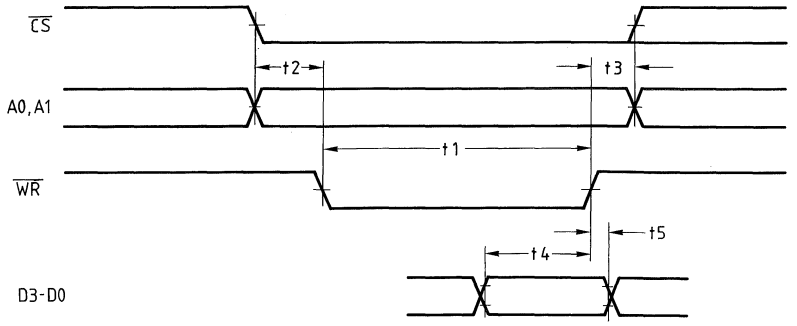
AC Testing Input, Output Waveform



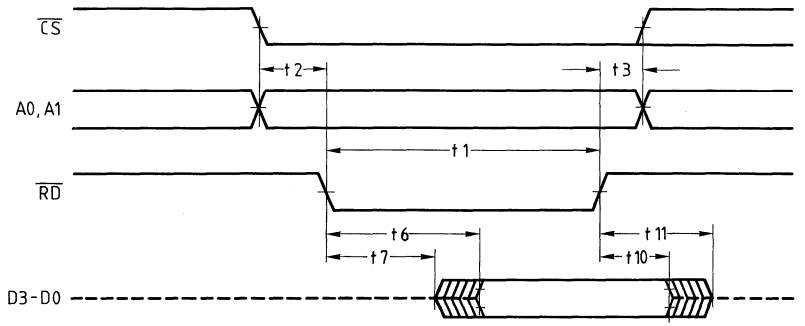
Output Test Load Circuits



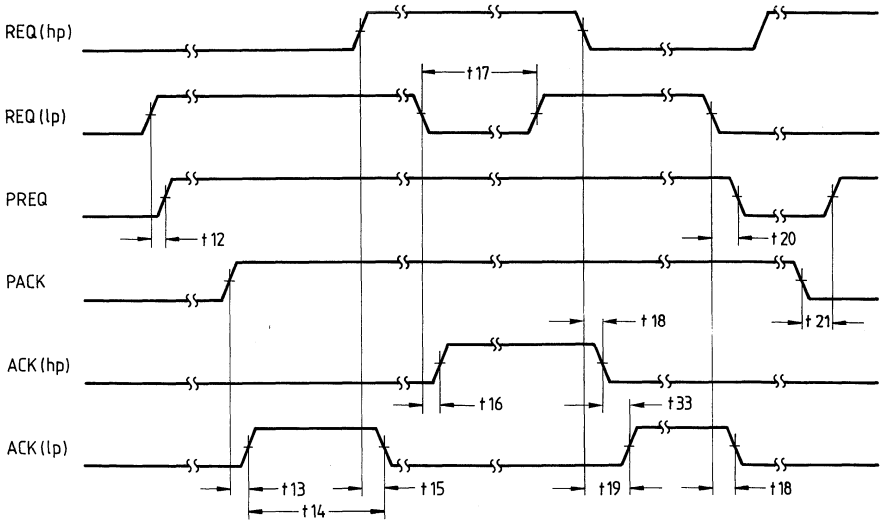
Write Timing



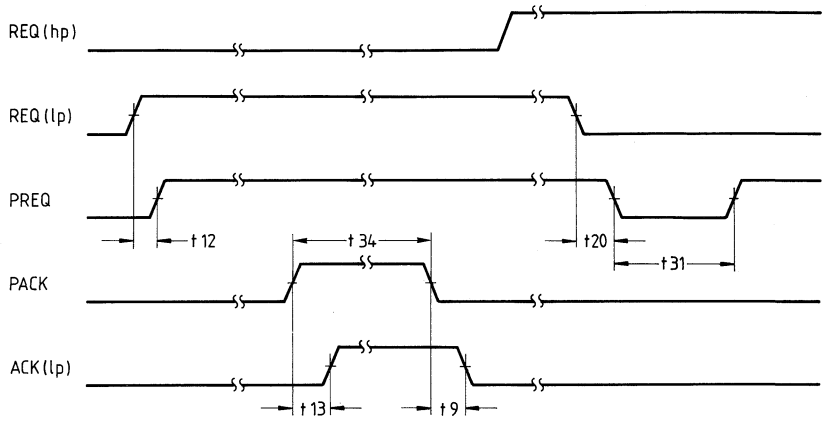
Read Timing



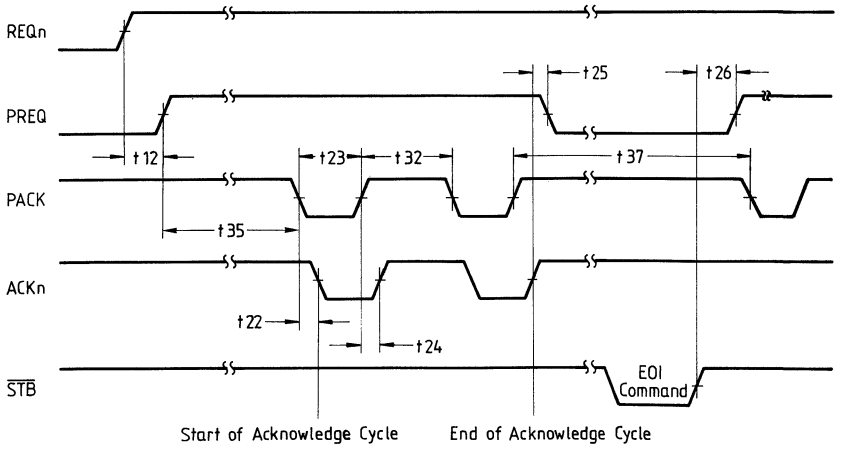
Basic DMA Mode Timings



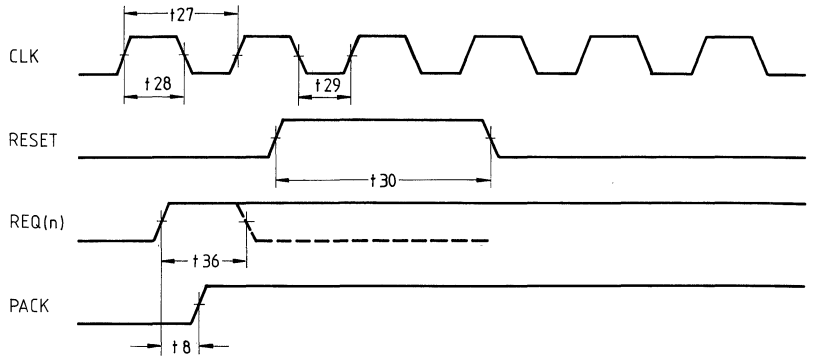
Premature Deactivation of PACK



Interrupt Mode Timings

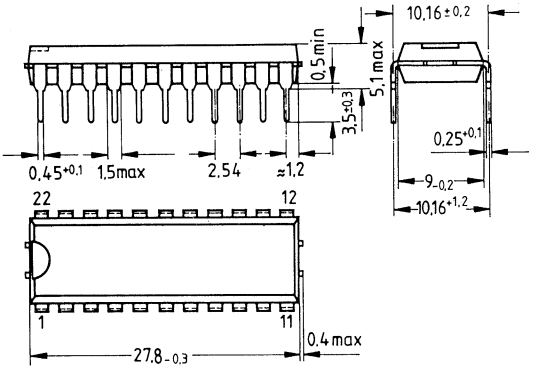


Other Timings



Package Outline

Plastic Package, DIP, 22 pins



Dimensions in mm

Ordering Information

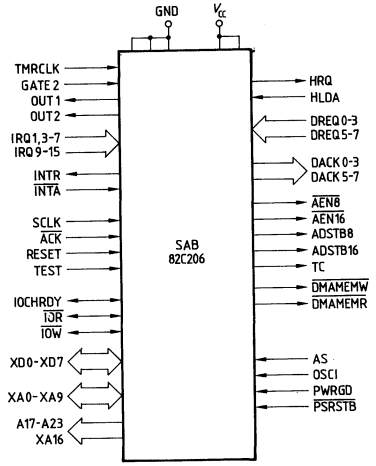
Type	Ordering code	Description
SAB 82200-P	Q67020-Y171	Local bus arbiter

Advance Information

SAB 82C206
Integrated Peripheral Controller

- 100% compatible to PC/AT designs
- Fully compatible to SAB 8237 DMA Controller, SAB 8259 Interrupt Controller, SAB 8254 Timer/Counter, and 146818 Real Time Clock
- 7 DMA Channels, 13 Interrupt Request Channels, 2 Timer/Counter Channels, and a Real Time Clock
- Reduced Recovery Time (120 ns) between Control Signals
- Programmable Wait States for the DMA Cycle and Internal Register Access
- 8 MHz DMA Clock
- 16 Mbytes of DMA Address Space
- 114 Bytes of CMOS RAM Memory
- Full Static Design
- PL-CC-84 Package
- Advanced CMOS (ACMOS) Technology
- Compatible with the Standard 82C206

Logic Symbol



The SAB 82C206 Integrated Peripheral Controller incorporates two 8237 DMA Controllers, two 8259 Interrupt Controllers, one 8254 Timer/Counter, one 146818 Real Time Clock, one 74LS612 Memory Mapper, in addition to several other TTL/SSI interface logic chips to provide a single-chip integration of all the peripherals attached to the peripheral bus (X-Bus) in the IBM™ PC/AT™. While offering complete compatibility to the IBM PC/AT architecture, the chip exhibits enhanced features and improved speed performance. These include additional 64 bytes of user RAM for the Real Time Clock and drastically reduced recovery specifications for the 8237, 8259 and 8254.

Variable wait state option is provided for the DMA cycles. Programmable delays are possible for CPU access to the internal registers of the chip. The chip allows selection of an 8 or 4 MHz DMA clock.

The SAB 82C206 provides a highly integrated high-performance system solution for PC/AT compatible implementations. It is compatible with the standard 82C206 IPC and offers compatibility to the CS8220, CS8221 and CS8230 PC chip sets.

The SAB 82C206 is fabricated in Siemens ACMOS technology and packaged in an 84-pin plastic leaded chip carrier (PL-CC-84) package.

Figure 1
Pin Configuration (Top View)

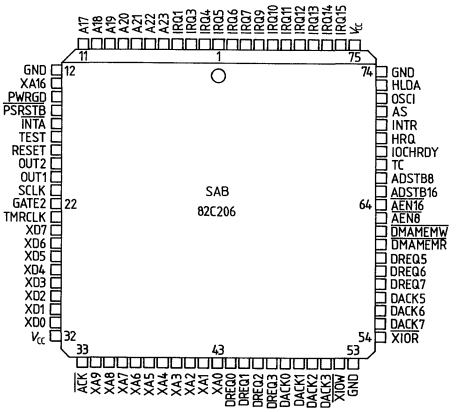
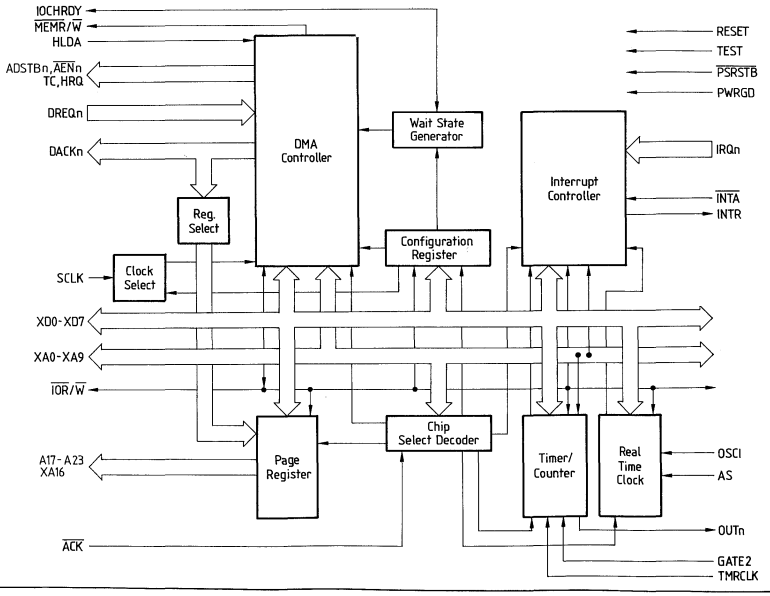


Figure 2
Block Diagram



Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
IRQ1 IRQ3-IRQ5 IRQ6, IRQ7 IRQ9-IRQ15	4 3–1 84, 83 82–76	I I I I	INTERRUPT REQUESTS Asynchronous inputs. An Interrupt Request is executed by raising an IRQ input low to high and holding it high until it is acknowledged (edge-triggered mode) or just by a high level on an IRQ input (level-triggered mode).
A23-A17 XA16	5–11 13	O O	DMA PAGE REGISTER ADDRESS XA16 and A17-A23 are tristate output pins. XA16 is the least significant bit of the DMA Page Register and is used for DMA transfers to 8-bit peripherals only (channel 0-3). XA16 is not used for DMA transfers to 16-bit peripherals (channel 5-7) as XA9-XA16 is provided by demultiplexing the Data Bus. A17-A23 are the upper 7 bits of the DMA Page Register.
PWRGD	14	I	PWRGOOD The Power Good pin must be high for bus cycles in which the CPU accesses the RTC. When PWRGD is low, all address, data, data strobe and R/W pins are disconnected from the processor.
$\overline{\text{PSRSTB}}$	15	I	This input is used to establish the condition of the control registers when power is applied to the device. In a PC/AT compatible design, this pin should be tied to the battery back-up circuit. When $\overline{\text{PSRSTB}}$ and TEST are both low, the following occurs: (a) Periodic Interrupt Enable (PIE) bit is cleared to zero. (b) Alarm Interrupt Enable (AIE) bit is cleared to zero. (c) Uptdate Ended Interrupt Enable (UIE) bit is cleared to zero. (d) Update Ended Interrupt Flag (UF) bit is cleared to zero. (e) Interrupt Request Status Flag (IRQF) is cleared to zero. (f) Periodic Interrupt Flag (PF) bit is cleared to zero. (g) The part is not accessible. (h) Alarm Interrupt Flag (AF) bit is cleared to zero. (i) Square Wave Output Enable list is cleared to zero.
$\overline{\text{INTA}}$	16	I	$\overline{\text{INTERRUPT ACKNOWLEDGE}}$ This pin is used to enable the interrupt vector data of the interrupt controllers to the data bus by a sequence of Interrupt Acknowledge pulses issued by the CPU.
TEST	17	I	TEST Test is an active high input. It initializes various internal registers so that a device test program starts in a known state. It should be tied low for normal operation.
RESET	18	I	RESET Reset is an active high input which affects the following registers: DMA Controllers: clears the Command, Status, DMA Request, Temporary Register, First/Last flipflop; sets the Mask Register. Following Reset, the DMA Controller is in an idle state. Interrupt Controllers: clears the edge sense circuit, the Interrupt Mask Register, all ICW4 functions, IRQ0 is assigned highest priority, slave address is set to 7, Special Mask Mode is disabled and Status Read is set to IRR.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
OUT 2	19	O	OUT 2 Output of Timer 2. In a PC/AT compatible design, OUT 2 is used to drive the speaker.
OUT 1	20	O	OUT 1 Output of Timer 1. In a PC/AT compatible design, Timer 1 is programmed as a rate generator to produce 15 µsec period signals used for Interrupt Request to initiate refresh cycles.
SCLK	21	I	CLOCK INPUT The Clock Input is used to generate the timing signals which control DMA operations. This input may be driven from DC to 16 MHz. The clock may be stopped in either state for standby operation. The internal clock used for DMA is either the SCLK or SCLK/2 depending on the setting of DMA CLOCK SELECT bit in the Configuration Register.
GATE2	22	I	GATE2 Gate input for Counter 2. In a PC/AT compatible design, the Counter 2 is used for tone generation for speaker. In this design, the GATE 2 input is driven by bit 0 of I/O Port 61H (called TIM2GATE SPK).
TMRCLK	23	I	TIMER CLOCK Clock input for Counter 0, Counter 1 and Counter 2.
XD7-XD0	24–31	I/O	DATA BUS The Data Bus lines are tristate bidirectional lines connected to the system Data Bus (XD Bus in a PC/AT design). The outputs are enabled in the program condition during the I/O Read to output the contents of the DMA Controller registers (Address Register, Status Register, the Temporary Register or a Word Count Register), the three Interrupt Controller registers (Interrupt Request Register, In Service Register and the Interrupt Mask Register), the Timer/Counters registers (namely the contents of these counters or states of the counters), the Real Time Clock's internal registers and page registers of the Memory Mapper. During an I/O write cycle, the outputs are disabled and the CPU can program the DMA Controller registers, the Interrupt Controller registers, the Timer/Counters registers, the DMA Page Register and the Real Time Clock registers and internal RAM. During DMA cycles, the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB8 or ADSTB16. During memory-to-memory operations, data from the memory comes into the DMA Controller on the Data Bus during read from the memory. In the Write to Memory transfer, the Data Bus outputs the data for the new memory location. During the interrupt acknowledge sequence, the Interrupt Controllers output the interrupt vector byte on the data bus. Data bus XD7-XD0 also acts as the multiplexed address/data bus for the Real Time Clock.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{ACK}$ (MSE)	33	I	MODULE SELECT ENABLE When high, it enables the Chip Select function on one of the modules (DMA Controller, INT Controller, Timer, RTC, DMA Page Register or the Configuration Register) for the programming function, i.e. CPU read or write of the Command, Status or other register of various modules of the SAB 82C206. When low, the SAB 82C206 is essentially disconnected from the System Bus. The SAB 82C206 at this time could be performing an active DMA or an interrupt cycle. In a PC/AT compatible design, this pin is tied to $\overline{ACK}$ signal.
XA9 XA8-XA0	34 35-43	I I/O	ADDRESS BUS This is the system address bus used to address various registers of the SAB 82C206. It is tied to the external bus (XA bus) in a PC/AT compatible design. During a non-DMA cycle, A3-A0 act as inputs and are used by the CPU to address the registers of the DMA Controller corresponding to DMA channels 0-3. A4-A1 address the registers of the DMA Controller corresponding to DMA channels 5-7. In the active DMA cycle, A7-A0 are outputs and carry address information for DMA channels 0-3. Correspondingly, A8-A1 are address outputs for 16-bit DMA channels 5-7. During program condition, A9-A0 are used to address the configuration register and the internal registers of DMA Controller, INT Controller, Timer, RTC and Memory Mapper.
DREQ0-3 DREQ5-7	44-47 60-58	I I	DMA REQUEST The DMA Request pins (DREQ) are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ7 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active. DREQ will not be recognized while the DMA clock is stopped. Unused DREQ inputs should be pulled high or low (inactive) and the corresponding mask bit set. DREQ0-DREQ3 support 8-bit transfers between 8-bit I/O and 8 or 16-bit system memory. DREQ5-DREQ7 support 16-bit data transfers between 16-bit peripheral and 16-bit system memory. DREQ4 is not available because it is used to cascade DREQ0-DREQ3.
DACK0-3 DACK7-5	48-51 55-57	O O	DMA ACKNOWLEDGE DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The active polarity of these lines is programmable. Reset initializes them to active low. Because these signals are used internally for cascading the DMA channels and for DMA page register selection, these signals must be programmed to be active low.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{XIOW}$	52	I/O	$\overline{I/O\ WRITE}$ I/O Write is a bidirectional active low tristate signal. In an idle cycle (non-DMA, non-interrupt), it is an input control signal used by the CPU to load information to the SAB 82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA Controller to load data to the peripheral devices during a DMA Read transfer.
$\overline{XIOR}$	54	I/O	$\overline{I/O\ READ}$ I/O Read is a bidirectional active low tristate line. In an idle cycle (non-DMA, non-interrupt), it is an input control signal used by the CPU to read the SAB 82C206 internal registers. In an active DMA cycle, it is an output control signal used by the DMA Controller to access data from a peripheral device during a DMA write transfer.
$\overline{DMAMEMR}$	61	O	$\overline{DMA\ MEMORY\ READ}$ This is an active low tristate output used to access data from the selected memory location during DMA Read or memory-to-memory transfer.
$\overline{DMAMEMW}$	62	O	$\overline{DMA\ MEMORY\ WRITE}$ This is an active low tristate output used to write data to the selected memory location during DMA write or a memory-to-memory transfer. In a PC/AT compatible design, this signal is connected to $\overline{XMEMW}$.
$\overline{AEN8}$	63	O	$\overline{ADDRESS\ ENABLE}$ for 8-bit DMA transfers. This signal is the output enable for the 8-bit latch containing the upper 8 address bits (A8-A15). It enables A8-A15 to the system address bus. It is inactive when the external bus master controls the system bus. $\overline{AEN8}$ is active low.
$\overline{AEN16}$	64	O	$\overline{ADDRESS\ ENABLE}$ for 16-bit DMA transfers. This signal enables the 8-bit latch containing the upper 8 address bits (A9-A16) on to system address bus. It is inactive when the external bus master controls the system bus. $\overline{AEN16}$ is active low.
ADSTB16	65	O	ADDRESS STROBE for 16-bit transfers This is an active high signal used to control latching of the upper address byte A9-A16 for 16-bit DMA transfers. Its function is just like ADSTB8. ADSTB16 is active for DMA channels 5-7.
ADSTB8	66	O	ADDRESS STROBE for 8-bit transfers This is an active high signal used to control latching of the upper address byte (A8-A15) for 8-bit peripherals. It will drive directly the strobe input of external transparent octal latches. During block operations, ADSTB8 will only be issued when the upper address byte must be updated, thus speeding operation through elimination of S1 states. ADSTB8 is active for DMA channels 0-3.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
TC	67	O	TERMINAL COUNT Terminal Count (TC) is an active high signal. Information concerning the completion of DMA services is available at the TC output pin. A pulse is generated by the DMA Controller when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers TC will be output when the TC for channel 1 occurs. When a TC pulse occurs, the DMA Controller will terminate the service, and if auto-initialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel unless the channel is programmed for auto-initialize. In that case, the mask bit remains clear.
IOCHRDY	68	I/O	I/O CHANNEL READY In the input mode, a low on IOCHRDY causes the internal DMA ready signal to go low asynchronously. When IOCHRDY goes high, one DMA clock cycle will elapse before internal DMA Ready goes up. This signal is used to extend memory read and write pulses for the DMA controllers to accommodate slow memories or I/O devices. IOCHRDY must satisfy set-up and hold times with respect to SCLK in order to work reliably. In the output mode, this pin is an open drain output and provides an active low output whenever any SAB 82C206 register is addressed for read or write. This output will remain low for a programmed number of SCLK cycles (as configured by bits 6 and 7 of the SAB 82C206 configuration register) and then goes high if pulled up by an external resistor. IOCHRDY provides a means of introducing a programmed number of wait states (as counted by SCLK cycles) for I/O read/write cycles to SAB 82C206. In a PC/AT architecture based design this pin should be wire-ORed to PC/AT's IOCHRDY signal.
HRQ	69	O	HOLD REQUEST The Hold Request output is used to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the DMA Controller issues HRQ. The HLDA signal then informs the controller when access to the system buses is permitted. For stand-alone operation where the DMA Controller always controls the buses, HRQ may be tied to HLDA. This will result in one S0 state before the transfer.
INTR	70	O	INTERRUPT This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU and is usually connected to the CPU's interrupt pin.
AS	71	I	ADDRESS STROBE Address Strobe is a positive pulse whose falling edge latches the address from the XD bus.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
OSCI	72	I	OSCILLATOR INPUT The time base for the time functions is connected to this pin. External square waves of 32.768 KHz may be connected to this input.
HLDA	73	I	HOLD ACKNOWLEDGE The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system buses.
V_{CC}	32, 75	–	POWER SUPPLY (+5 V)
GND	12, 53, 74	–	GROUND (0 V)

Functional Description

The SAB 82C206 is an LSI implementation of the standard peripherals required to implement an IBM PC/AT system board. This device contains the equivalent of two 8237A DMA Controllers, a 74LS612 Mapper, two 8259A Interrupt Controllers, an 8254 Counter/Timer, and a 146818 Real Time Clock with RAM. The SAB 82C206 provides all of the standard peripherals required for a system board implementation except the keyboard interface controller. Figure 2 illustrates the subsystems contained within the SAB 82C206.

Two DMA controllers are connected in such a way as to provide the user with four DMA channels (DMA1) for 8-bit transfers and three DMA channels (DMA2) for 16-bit transfers (the first 16-bit DMA channel is used for cascading). Included as part of the DMA subsystem is the Page Register (DMAPAGE) device which is used to supplement the DMA and drive the upper address lines when required.

Sixteen interrupt channels are provided in the SAB 82C206. These channels are allocated to two cascaded controllers (INTC1, INTC2) with 8 inputs each. Of these 16 channels, three are connected internally to various devices, allowing 13 user-definable interrupt channels. The three internally connected channels are as follows:

Channel 0 – Counter/Timer Counter 0 Interrupt
Channel 2 – Cascade to Slave Interrupt Controller (INTC2)
Channel 8 – Real Time Clock Interrupt

The remaining 13 channels may be defined and utilized as necessary to meet the user-specific system requirements.

A Counter/Timer (CTC) subsystem contains three independent counters. All three counters are driven from a clock input pin which is independent from the other clock inputs to the device. Counter 0 is connected to Interrupt 0 of INTC1. It is intended to be used as a multi-level interrupt to the system for such tasks as time keeping and task-switching. Counter 1 may be programmed to generate pulses or square waves for use by external devices. The third channel (Counter 2) is a full function Counter/Timer which has a gate input for controlling the internal counter. This channel can be used as an interval counter, a timer, or as a gated rate/pulse generator.

A Real Time Clock (RTC) is included in the SAB 82C206 for maintaining the time and date. This subsystem also contains 114 bytes of RAM in addition to the Clock/Calendar. The Clock/Calendar information and RAM are kept active by connecting the device to an external battery when system power is turned off.

To interconnect and control all of these major subsystems a top level control section is employed which is divided into subsystems for purposes of discussion.

The first section is the Clock and Wait State Control section. This subsystem controls the generation of DMA wait states and the negation of IOCHRDY (if programmed to do so) during CPU access of the device. The last subsystem is the Top Level Decode.

In order to accommodate over 200 registers in the SAB 82C206 and maintain I/O decode compatibility with the IBM PC/AT, a multilevel decode scheme is employed. The Top Level Decode subsystem performs the function of generating enables to the various subsystems. Control and direction of the XD0-XD7 data bus buffers are also handled by this subsystem.

Top Level Decoder

The SAB 82C206 Top Level Decoder provides 8 separate enables to various subsystems of the device. Table 1 contains a truth table for the Top Level Decoder. Enabling of the SAB 82C206 XD0-XD7 output buffers is also controlled by this section. The output buffers are enabled whenever an enable is generated to an internal subsystem and the $\overline{\text{XIOR}}$ signal is asserted.

Table 1
Top Level Decoder

$\overline{ACK}$	XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	Address Range (Hex)	Selected Device
1	0	0	0	0	0	0	X	X	X	X	000-00F	DMA1
1	0	0	0	0	1	0	0	0	0	X	020-021	INTC1
1	0	0	0	0	1	0	0	0	1	X	022-023	CONFIG
1	0	0	0	1	0	0	0	0	X	X	040-043	CTC
1	0	0	0	1	1	1	0	0	0	X	070-071	RTC
1	0	0	1	0	0	0	X	X	X	X	080-08F	DMAPAGE
1	0	0	1	0	1	0	0	0	0	X	0A0-0A1	INTC2
1	0	0	1	1	0	X	X	X	X	X	0C0-0DF	DMA2
0	X	X	X	X	X	X	X	X	X	X	Disabled	
X	1	X	X	X	X	X	X	X	X	X	Disabled	
X	X	1	X	X	X	X	X	X	X	X	Disabled	

The decoder is enabled by three signals. These three signals are $\overline{ACK}$, XA9 and XA8. To enable any internal device $\overline{ACK}$ must be "1" and both XA9 and XA8 must be "0".

The decode scheme employed in the SAB 82C206 is designed to comply with the IBM PC/AT requirements and is more fully decoded. If the user wishes to take advantage of the areas which are unused by inserting additional peripherals in the I/O map, he may do so since the subsystems in the SAB 82C206 will not respond to the unused address spaces established by the Top Level Decoder. The extra peripherals may be tied directly to the XD0-XD7 data lines since the SAB 82C206 output buffers are not enabled unless an internal subsystem is enabled.

Clock and Wait State Control

The Clock and Wait State Control subsystem performs four functions, control of the DMA command width, control of the CPU read or write cycle length, and selection of the DMA clock rate. All of these functions are user selectable by writing to the Configuration Register located at address 023H.

Writing and reading this register is accomplished by first writing a 01H to location 022H to select the SAB 82C206 Configuration Register, and then performing either a read or write to location 023H.

Configuration Register (023H):

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
RW1	RW0	16W1	16W0	8W1	8W0	EMR	CLK

RW1-RW0 – When the higher speed CPU's are accessing the SAB 82C206, the cycle can be extended by programming up to four wait states into the Configuration Register. This will cause the SAB 82C206 to assert a not ready condition on IOCHRDY (low) whenever a valid decode from the Top Level Decoder is detected and either $\overline{XIOR}$ or $\overline{XIOW}$ is asserted. IOCHRDY will remain low for the number of wait states programmed into the Configuration Register bits 6 and 7.

RW1	RW0	Read/Write Cycle Wait States
0	0	1
0	1	2
1	0	3
1	1	4

Wait states programmed by RW0 and RW1 are in increments of one SCLK cycle and are not affected by the DMA Clock Divider.

16W1-16W0 – Wait states can be independently controlled for both 8-bit and 16-bit DMA cycles. This allows the user to tailor the DMA cycle more closely to the application.

16W1	16W0	16-Bit DMA Wait States
0	0	1
0	1	2
1	0	3
1	1	4

8W1-8W0 – Wait states may be inserted in 8-bit DMA cycles by programming these two bits in the Configuration Register.

8W1	8W0	8-Bit DMA Wait States
0	0	1
0	1	2
1	0	3
1	1	4

Further control of the cycle length is available through the use of the IOCHRDY pin on the SAB 82C206. During DMA this pin is used as an input to the wait state generation logic to extend the cycle if necessary. This input is driven low by the peripheral to extend the cycle. The cycle can then be completed by releasing IOCHRDY and allowing it to return high.

EMR – This bit enables the extended $\overline{\text{DMAMEMR}}$ function. Normally the assertion of $\overline{\text{DMAMEMR}}$ is delayed one clock cycle later than $\overline{\text{XIOR}}$ in the IBM PC/AT implementation. This may not be desirable in some systems. A "1" programmed into this bit position will start $\overline{\text{DMAMEMR}}$ at the same time as $\overline{\text{XIOR}}$.

CLK – This bit allows the user to insert a divider between the DMA Controller subsystems and the SCLK input in, or connect the two directly. When this bit position contains a "0", the SCLK input is divided by two and is used to drive both the 8-bit and 16-bit DMA subsystems. A "1" in this position bypasses the divider and uses the SCLK input directly. Whenever the state of this bit is changed, an internal synchronizer controls the actual switching of the clock to prevent a short clock pulse from causing a DMA malfunction.

DMA wait states are in increments of one DMA clock cycle, which is affected by the DMA clock divider.

The Configuration Register contents are preloaded by RESET to an initial value of 0C0H. This value establishes a default which is IBM PC/AT compatible and corresponds to:

Read/Write cycles – 4 wait states
16-bit DMA transfers – 1 wait state
8-bit DMA transfers – 1 wait state

$\overline{\text{DMAMEMR}}$ is delayed 1 DMA clock cycle later than $\overline{\text{XIOR}}$.

DMA clock is equal to SCLK/2.

DMA Functional Description

The equivalent of two 8237A DMA Controllers is implemented in the SAB 82C206. Each controller is a four channel DMA device which will generate the memory addresses and control signals necessary to transfer information between a peripheral device and memory directly. This allows high speed information transfers with less CPU intervention.

The two DMA controllers are internally cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1), and three channels for transfers to 16-bit peripherals (DMA2). DMA2 Channel 0 provides the cascade interconnection of the two DMA devices, thereby maintaining IBM PC/AT compatibility.

DMA cycle length control is provided internally in the SAB 82C206 allowing independent control for both 8-bit and 16-bit cycles. This is done through the programmable registers which can extend command signals or insert wait states.

Each DMA channel has a pair of 16-bit counters and a reload register for each counter. The 16-bit counters allow the DMA channel to transfer blocks as large as 64 K words. The register associated with each counter allows the channel to reinitialize without reprogramming.

From this point on, the description of the DMA subsystem pertains to both DMA1 and DMA2 unless otherwise noted.

DMA Operation

During normal operation of the SAB 82C206, the DMA subsystem will be in either the Idle condition, the Program condition or the Active condition. In the Idle condition the DMA controller will be executing cycles consisting of only one state. The Idle state SI is the default condition and the DMA will remain in this condition unless the device has been initialized and one of the DMA requests is active or the CPU attempts to access one of the internal registers.

When a DMA request becomes active the device enters the Active condition and issues a hold request to the system. Once in the Active condition the SAB 82C206 will generate the necessary memory addresses and command signals to accomplish a memory-to-I/O, I/O-to-memory, or a memory-to-memory transfer. Memory-to-I/O and I/O-to-memory transfers take place in one cycle while memory-to-memory transfers require two cycles. During transfers between memory and I/O, data is presented on the system bus by either memory or the requesting device and the transfer is completed in one cycle. Memory-to-memory transfers, however, require the DMA to store data from the read operation in an internal register. The contents of this register is then written to memory on the subsequent cycle.

During transfers between memory and I/O, two commands are activated during the same cycle. In the case of a memory-to-I/O transfer, the SAB 82C206 will assert both $\overline{\text{DMAMEMR}}$ and $\overline{\text{XIOW}}$ allowing data to be transferred directly to the requesting device from memory. Note that SAB 82C206 does not latch data from nor drive data out on this type of cycle.

The number of clock cycles required to transfer a word of data may be varied by programming the DMA or, optionally extended by the peripheral device. During an Active cycle the DMA will sequence through a series of states. Each state will be one DMA clock cycle in length and the number of states in a cycle will vary depending on how the device is programmed and what type of cycle is being performed. The states are labeled S0-S4 and will be explained in detail in the section entitled Active Condition.

Idle Condition

When no device is requesting service the DMA is in an Idle condition which maintains the state machine in the SI state. During this time the SAB 82C206 will sample the DREQ input pins every clock cycle. The internal select from the top level decoder and HLDA are also sampled at the same time to determine if the CPU is attempting to access the internal registers. When either of the above two situations occurs, the DMA will exit the Idle condition. Note that the Program condition has priority over the Active condition since a CPU cycle has already started.

Program Condition

The Program condition is entered whenever HLDA is inactive and an internal select is active. The internal select is derived from the top level decoder described previously. During this time address lines XA0-XA3 become inputs if DMA1 is selected, or XA1-XA4 become inputs if DMA2 is selected. Note, when DMA2 is selected XA0 is ignored. These address inputs are used to select the DMA controller registers which are to be read or written. Table 2 lists the register address assignment. Due to the large number of internal registers in the DMA subsystem, an internal flip-flop is used to supplement the addressing of the count and address registers. This bit is used to select between the high and low bytes of these registers. The flip-flop will toggle each time a read or write occurs to any of the word count or address registers in the DMA. This internal flip-flop will be cleared by hardware RESET or a Master Clear command and may be set or cleared by the CPU issuing the appropriate command.

Table 2
DMA Register Address Operations

DMA1	DMA2	$\overline{XIOR}$	$\overline{XIOW}$	Flip-Flop	Register Function
000H	0C0H	0	1	0	Read Channel 0 Current Addres Low Byte
		0	1	1	Read Channel 0 Current Address High Byte
		1	0	0	Write Channel 0 Base and Current Address Low Byte
		1	0	1	Write Channel 0 Base and Current Address High Byte
001H	0C2H	0	1	0	Read Channel 0 Current Word Count Low Byte
		0	1	1	Read Channel 0 Current Word Count High Byte
		1	0	0	Write Channel 0 Base and Current Word Count Low Byte
		1	0	1	Write Channel 0 Base and Current Word Count High Byte
002H	0C4H	0	1	0	Read Channel 1 Current Address Low Byte
		0	1	1	Read Channel 1 Current Address High Byte
		1	0	0	Write Channel 1 Base and Current Address Low Byte
		1	0	1	Write Channel 1 Base and Current Address High Byte
003H	0C6H	0	1	0	Read Channel 1 Current Word Count Low Byte
		0	1	1	Read Channel 1 Current Word Count High Byte
		1	0	0	Write Channel 1 Base and Current Word Count Low Byte
		1	0	1	Write Channel 1 Base and Current Word Count High Byte
004H	0C8H	0	1	0	Read Channel 2 Current Address Low Byte
		0	1	1	Read Channel 2 Current Address High Byte
		1	0	0	Write Channel 2 Base and Current Address Low Byte
		1	0	1	Write Channel 2 Base and Current Address High Byte
005H	0CAH	0	1	0	Read Channel 2 Current Word Count Low Byte
		0	1	1	Read Channel 2 Current Word Count High Byte
		1	0	0	Write Channel 2 Base and Current Word Count Low Byte
		1	0	1	Write Channel 2 Base and Current Word Count High Byte
006H	0CCH	0	1	0	Read Channel 3 Current Address Low Byte
		0	1	1	Read Channel 3 Current Address High Byte
		1	0	0	Write Channel 3 Base and Current Address Low Byte
		1	0	1	Write Channel 3 Base and Current Address High Byte
007H	0CEH	0	1	0	Read Channel 3 Current Word Count Low Byte
		0	1	1	Read Channel 3 Current Word Count High Byte
		1	0	0	Write Channel 3 Base and Current Word Count Low Byte
		1	0	1	Write Channel 3 Base and Current Word Count High Byte
008H	0D0H	0	1	X	Read Status Register
		1	0	X	Write Command Register
009H	0D2H	0	1	X	Read DMA Request Register
		1	0	X	Write DMA Request Register
00AH	0D4H	0	1	X	Read Command Register
		1	0	X	Write Single Bit DMA Request Mask Register

Table 2
DMA Register Address Operations (cont'd)

DMA1	DMA2	$\overline{XIOR}$	$\overline{XIOW}$	Flip-Flop	Register Function
00BH	0D6H	0	1	X	Read Mode Register
		1	0		Write Mode Register
00CH	0D8H	0	1	X	Set Byte Pointer Flip-Flop
		1	0	X	Clear Byte Pointer Flip-Flop
00DH	0DAH	0	1	X	Read Temporary Register
		1	0	X	Master Clear
00EH	0DCH	0	1	X	Clear Mode Register Counter
		1	0	X	Clear All DMA Request Mask Register Bits
00FH	0DEH	0	1	X	Read All DMA Request Mask Register Bits
		1	0	X	Write All DMA Request Mask Register Bits

Special commands are supported by the DMA subsystem in the Program condition to control the device. These commands do not make use of the data bus but are derived from a set of addresses, the internal select and $\overline{XIOW}$ or $\overline{XIOR}$. These commands are Master Clear, Clear Mask Register, Clear Mode Register Counter, Set and Clear Byte Pointer Flip-Flop.

The SAB 82C206 will enable programming whenever HLDA has been inactive for one DMA clock cycle. It is the responsibility of the system to ensure that programming and HLDA are mutually exclusive. Erratic operation of the SAB 82C206 can occur if a request for service occurs on an unmasked channel which is being programmed. The channel should be masked or the DMA disabled to prevent the SAB 82C206 from attempting to service a device with a channel which is partially programmed.

Active Condition

The SAB 82C206 DMA subsystem enters the Active condition whenever a software request or a DMA request on an unmasked channel occurs and the device is not in the Program condition. The SAB 82C206 will then begin a DMA transfer cycle.

In a read cycle for example, after receiving a DREQ, the SAB 82C206 will issue a HRQ to the system. Until a HLDA is returned the DMA will remain in an idle condition. On the next clock cycle the DMA will exit Idle and enter state S0. During S0 the device will resolve priority and issue DACK on the highest priority channel requesting service. The DMA will then proceed to state S1 where the multiplexed addresses are output and latched. State S2 is then entered, at which time the SAB 82C206 will assert $\overline{DMAMEMR}$. The device then transitions into S3 where the $\overline{XIOW}$ command is asserted. The SAB 82C206 DMA will then remain in S3 until the Wait State Counter has decremented to zero and IOCHRDY is true. Note that at least one additional S3 will occur unless Compressed Timing is selected. Once a ready condition is detected, the DMA will enter S4 where both command lines are deasserted. In Burst Mode and Demand Mode, subsequent cycles will begin in S2 unless the intermediate addresses require updating. In these subsequent cycles the lower addresses are changed in S2.

The DMA can be programmed on a channel by channel basis to operate in one of four modes. The four modes are listed in the following.

Single Transfer Mode – This mode directs the DMA to execute only one transfer cycle at a time. DREQ must be held active until DACK becomes active. If DREQ is held active throughout the cycle, the SAB 82C206 will deassert HRQ and release the bus once the transfer is complete. After HLDA has gone inactive the SAB 82C206 will again assert HRQ and execute another cycle on the same channel unless a request from a higher priority channel has been received. In this mode the CPU is ensured of being allowed to execute at least one bus cycle between transfers.

Following each transfer the word count is decremented and the address is incremented or decremented. When the word count decrements from 0000H to FFFFH the terminal count bit in the status register is set and a TC pulse is generated. If the autoinitialization option has been enabled, the channel will reinitialize itself. If Autoinitialize is not selected the DMA will set the DMA request bit mask and suspend transferring on that channel.

Block Transfer Mode – When Block Transfer Mode is selected, the SAB 82C206 will begin transfers in response to either a DREQ or a software request and will continue until a terminal count (FFFFH) is reached, at which time TC is pulsed and the status register terminal count bit is set. In this mode DREQ need only be held active until DACK is asserted. Autoinitialization is optional in this mode also.

Demand Transfer Mode – In Demand Transfer mode the DMA will start transfers in response to the assertion of DREQ and will continue until either terminal count is reached or DREQ becomes inactive. This mode is normally used for peripherals which have limited buffering capability. The peripheral can initiate a transfer and continue until its buffer capacity is exhausted. The peripheral may then re-establish service by again asserting DREQ. During idle periods between transfers the CPU is released to operate and can monitor the operation by reading intermediate values from the address and word count registers. Once DREQ has been deasserted, higher priority channels are allowed to intervene. Reaching terminal count will result in the generation of a TC pulse, the setting of the terminal count bit in the status register and autoinitialization (if enabled).

Cascade Mode – This mode is used to interconnect more than one DMA controller, to extend the number of DMA channels while preserving the priority chain. In Cascade mode the master DMA controller does not generate address or control signals. The DREQ and DACK signals of the master are used to interface the HRQ and HLDA signals of the slave DMA devices. Once the master has received a HLDA from the CPU in response to a DREQ caused by the HRQ from a slave DMA controller, the master DMA controller will ignore all inputs except HLDA from the CPU and DREQ on the active channel. This prevents conflicts between the DMA devices.

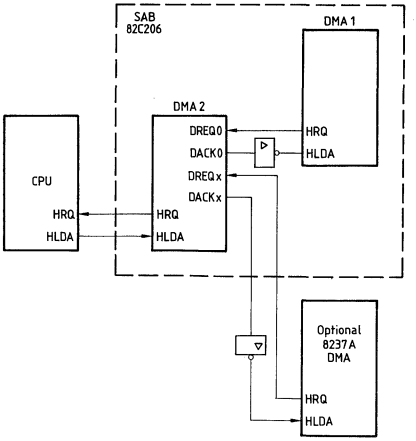
Figure 3 shows the cascade interconnection for two levels of DMA devices. Note that Channel 0 of DMA2 is internally connected for Cascade mode to DMA1. Additional devices can be cascaded to the available channels in either DMA1 or DMA2 since cascade is not limited to two levels of DMA controllers.

When programming cascaded controllers, begin with the device which is actually generating HRQ to the system (first level device) and then proceed to the second level devices. RESET causes the DACK outputs to become active low and are placed in the inactive state. To allow the internal cascade between DMA1 and DMA2 to function correctly, the active low state of DACK should not be modified. This is because the SAB 82C206 has an inverter between DACK0 of DMA2 and HLDA of DMA1. The first level device's DMA request mask bits will prevent second level cascaded devices from generating unwanted hold requests during the initialization process.

DMA Transfers

Four types of transfer modes are provided in the SAB 82C206 DMA subsystem. These transfer types are:

Figure 3
Cascade Mode Interconnections



Read Transfer – Read transfers move data from memory to an I/O device by generating the memory address and asserting $\overline{\text{DMAMEMR}}$ and $\overline{\text{XIOW}}$ during the same cycle.

Write Transfer – Write transfers move data from an I/O device to memory by generating the memory address and asserting $\overline{\text{XIOR}}$ and $\overline{\text{DMAMEMW}}$.

Memory-to-Memory Transfer – The memory-to-memory transfer is used to move a block of memory from one location in memory to another. DMA channels 0 and 1 may be programmed to operate as memory-to-memory channels by setting a bit in the Command Register. Once programmed to perform a memory-to-memory transfer the process can be started by generating either a software or an external request to channel 0. Once the transfer is initiated, Channel 0 provides the address for the source block during the memory read portion of the cycle. Channel 1 generates the address for the memory write cycle. During the read cycle, a byte of data is latched in the internal Temporary Register of the SAB 82C206. The contents of this register are then output on the XD0-7 data lines during the write portion of the cycle and subsequently written to memory. Channel 0 may be programmed to maintain the same source address on every cycle. This allows the CPU to initialize large blocks of memory with the same value. The SAB 82C206 will continue performing transfer cycles until Channel 1 reaches terminal count.

Verify Transfer – The verify transfer is a pseudo-transfer which is useful for diagnostics. In this type of transfer the DMA will operate as if it is performing a Read or Write Transfer by generating HRQ, addresses and DACK but will do so without asserting a command signal. Since no transfer actually takes place IOCHRDY is ignored during Verify transfer cycles.

Autoinitialization

Each of the four DMA channel Mode Registers contains a bit which will cause the channel to reinitialize after reaching terminal count. During this process, referred to an Autoinitialization, the Base Address and Base Word Count Registers, which were originally written to by the CPU, are reloaded into the Current Address and Current Word Count Registers (both the base and current registers are loaded during a CPU write cycle). The base registers remain unchanged during DMA Active cycles and can only be changed by the CPU. If the channel has been programmed to autoinitialize, the request mask bit will not be set upon reaching terminal count. This allows the DMA to continue operation without CPU intervention.

During memory-to-memory transfers the Word Count Registers of both Channel 0 and Channel 1 must be programmed with the same starting value for full autoinitialization. If Channel 0 reaches terminal count before Channel 1, then Channel 0 will reload the starting address and word count and continue transferring data from the beginning of the source block.

Should Channel 1 reach terminal count first, it will reload the current registers and Channel 0 will remain uninitialized.

DREQ Priority

The SAB 82C206 supports two schemes for establishing DREQ priority. The first is fixed priority which assigns priority based on channel position. In this method Channel 0 is assigned the highest priority. Priority assignment then progresses downward through the channels in order with Channel 3 receiving the lowest priority.

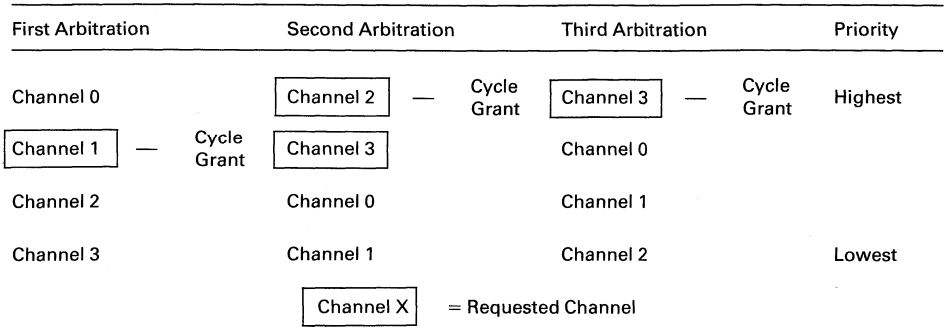
The second type of priority assignment is rotating priority. In this scheme the order of priority from Channel 0 to Channel 3 is maintained but the actual assignment of priority changes. The channel most recently serviced will be assigned the lowest priority and, since the order of priority assignment remains fixed, the remaining three channels rotate accordingly. The rotating priority assignment is illustrated in Figure 4.

In instances where multiple requests occur at the same time the SAB 82C206 will issue a HRQ but will not freeze the priority logic until HLDA is returned. Once HDLA becomes active the priority logic is frozen and DACK is asserted on the highest requesting channel. Priority will not be re-evaluated until HLDA has been deactivated.

Address Generation

Eight intermediate bits of the address are multiplexed onto the data lines during Active cycles of the DMA. This reduces the number of pins required by the DMA subsystem. During state S1, the intermediate addresses are output on data lines XD0-XD7. These addresses must be externally latched and used to drive the system address bus. Since DMA1 is used to transfer 8-bit data and DMA2 is used to transfer 16-bit data, a one-bit skew occurs in the intermediate address fields. DMA1 will therefore output addresses A8-A15 on the data bus at this time whereas DMA2 will output A9-A16. A separate set of latch and enable signals are provided for both DMA1 and DMA2 to accommodate the address skew.

Figure 4
Rotating Priority Scheme



During 8-bit DMA cycles, in which DMA1 is active, the SAB 82C206 will output the lower 8 bits of address on XA0-XA7. The intermediate 8 bits of address will be output on XD0-XD7 and ADSTB8 will be asserted for one DMA clock cycle. The falling edge of ADSTB8 is used to latch the intermediate addresses A8-A15. Enable signal $\overline{AEN8}$ is used to control the output drivers of the external latch. A16-A23 are also generated at this time from a DMA Page Register in the SAB 82C206. Note that A16 is output on the XA16 pin of the device.

16-bit DMA cycles from DMA2 require the SAB 82C206 to output the lower 8-bits of the address on XA1-XA8. The intermediate addresses A9-A16 are output on XD0-XD7. Control for a separate latch is provided by signals ADSTB16 and $\overline{AEN16}$. The DMA Page Register now generates A17-A23. During 16-bit DMA transfers XA0 and XA16 remain inactive.

The DMA Page Register is a set of 16 8-bit registers in the SAB 82C206 which are used to generate the high-order addresses during DMA cycles. Only 8 of the registers are actually used but all 16 were included to maintain IBM PC/AT compatibility. Each DMA channel has a register associated with it with the exception of Channel 0 of DMA2 which is used for internal cascading to DMA1. Assignment of each of these registers is shown in Table 3 along with its Read/Write address.

Table 3
DMA Address Extension Register Map

Address	Register Function
080H	Unused
081H	8-bit DMA Channel 2 (DACK2)
082H	8-bit DMA Channel 3 (DACK3)
083H	8-bit DMA Channel 1 (DACK1)
084H	Unused
085H	Unused
086H	Unused
087H	8-bit DMA Channel 0 (DACK0)
088H	Unused
089H	16-bit DMA Channel 2 (DACK6)
08AH	16-bit DMA Channel 3 (DACK7)
08BH	16-bit DMA Channel 1 (DACK5)
08CH	Unused
08DH	Unused
08EH	Unused
08FH	Refresh Cycle

During Demand and Block Transfers, the SAB 82C206 generates multiple sequential transfers. For most of these transfers the information in the external address latches will remain the same, eliminating the need to be relatched. Since the need to update the latches occurs only when a carry of borrow from the lower 8-bits of the Address Counter exists, the SAB 82C206 will only update the latch contents when necessary. The SAB 82C206 will therefore only execute S1 cycles when necessary, resulting in an overall throughput improvement.

Compressed Timing

The DMA subsystem in the SAB 82C206 can be programmed to transfer a word in as few as 3 DMA clock cycles. The normal DMA cycle consists of three states: S2, S3 and S4 (this assumes Demand or Block Transfer Mode). Normal transfers require 4 DMA clock cycles since S3 is executed twice due to the 1 wait state insertion. In systems capable of supporting higher throughput, the SAB 82C206 can be programmed to omit one S3 and assert both commands in S2. S2 begins the cycle by generating the address and asserting both commands. One S3 cycle is executed and the cycle terminates in S4. If Compressed Timing is selected, TC will be output in S2 and S1 cycles will be executed as necessary to update the address latch. Note that Compressed Timing is not allowed for memory-to-memory transfers.

Register Description
Current Address Register

Each DMA channel has a 16-bit Current Address Register which holds the address used during transfers. Each channel can be programmed to increment or decrement this register whenever a transfer is completed. This register can be read or written by the CPU in consecutive 8-bit bytes. If Autoinitialization is selected, this register will be reloaded from the Base Address Register upon reaching terminal count in the Current Word Count Register. Channel 0 can be prevented from incrementing or decrementing by setting the Address Hold Bit in the Command Register.

Current Word Count Register

Each channel has a Current Word Count Register which determines the number of transfers to perform. The actual number of transfers performed will be one greater than the value programmed into the register. The register is decremented after each transfer until it goes from zero to FFFFH. When this roll-over occurs the SAB 82C206 will generate and either suspend operation on that channel and set the appropriate Request Mask Bit or Autoinitialize and continue.

Base Address Register

Associated with each Current Address Register is a Base Address Register. This is a write only register which is loaded by the CPU when writing to the Current Address Register. The purpose of this register is to store the initial value of the Current Address Register for Autoinitialization. The contents of this register are loaded into the Current Address Register whenever terminal count is reached and the Autoinitialize Bit is set.

Base Word Count Register

This register preserves the initial value of the Current Word Count Register. It is also a write only register which is loaded by writing to the Current Word Count Register. This register is loaded into the Current Word Count Register during Autoinitialization.

Command Register

This register controls the overall operation of a DMA subsystem. The register can be read or written by the CPU and is cleared by either RESET or a Master Clear command.

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
DAK	DRQ	EW	RP	CT	CD	AH	M-M

DAK – DACK active level is determined by bit 7. Programming a 1 in this bit position makes DACK an active high signal.

DRQ – DREQ active level is determined by bit 6. Writing a 1 in this bit position causes DREQ to become active low.

EW – Extended Write is enabled by writing a 1 to bit 5, causing the write commands to be asserted one DMA cycle earlier during a transfer. The read and write commands both begin in state S2 when enabled.

RP – Writing a 1 to bit 4 causes the SAB 82C206 to utilize a rotating priority scheme for honoring DMA requests. The default condition is fixed priority.

CT – Compressed timing is enabled by writing a 1 to bit 3 of this register. The default 0 condition causes the DMA to operate with normal timing.

CD – Bit 2 is the master disable for the DMA controller. Writing a 1 to this location disables the DMA subsystem (DMA1 or DMA2). This function is normally used whenever the CPU needs to reprogram one of the channels to prevent DMA cycles.

AH – Writing a 1 to bit 1 enables the address hold feature in Channel 0 when performing memory-to-memory transfers.

M-M – A 1 in the bit 0 position enables Channel 0 and Channel 1 to be used for memory-to-memory transfers.

Mode Register

Each DMA channel has a Mode Register associated with it. All four Mode Registers reside at the same I/O address. Bits 0 and 1 of the Write Mode Register command determine which channel's Mode Register will be written to. The remaining six bits control the mode of the selected channel. Each channel's Mode Register can be read by sequentially reading the Mode Register location. A Clear Mode Register Counter command is provided to allow the CPU to restart the mode read process at a known point. During mode read operations, bits 0 and 1 will both be undefined.

Msb **Lsb**

b7	b6	b5	b4	b3	b2	b1	b0
M1	M0	DEC	AI	TT1	TT0	CS1	CS0

(Read/Write Register)

M1-M0 – Mode selection for each channel is accomplished by bits 6 and 7.

M1	M0	MODE
0	0	Demand Mode
0	1	Single Cycle Mode
1	0	Block Mode
1	1	Cascade Mode

DEC – Determines direction of the address counter. A one in bit 5 decrements the address after each transfer.

AI – The Autoinitialization function is enabled by writing a 1 in bit 4 of the Mode Register.

TT1-TT0 – Bits 2 and 3 control the type of transfer which is to be performed.

TT1	TT0	TYPE
0	0	Verify Transfer
0	1	Write Transfer
1	0	Read Transfer
1	1	Illegal

CS1-CS0 – Channel Select bits 1 and 0 determine which channel's Mode Register will be written to. Read back of a mode register will result in bits 1 and 0 both being undefined.

CS1	CS0	Channel
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Request Register

This is a 4-bit register used to generate software requests (DMA service can be requested either externally or under software control). Request Register bits can be set or reset independently by the CPU. The Request Mask has no effect on software-generated requests.

All four bits are read in one operation and appear in the lower four bits of the byte. Bits 4 through 7 are read as ones. All four request bits are cleared to zero by RESET.

Msb **Lsb**

b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	RB	RS1	RS0

(Write Operation)

RB – The request bit is set by writing a 1 to bit 2. RS1-RS0 select which bit (channel) is to be manipulated.

RS1-RS0 – Channel Select 0 and 1 determine which channel's Request Register will be written.

RS1	RS0	Channel
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

The format for the Request Register read operation is shown below.

Msb **Lsb**

b7	b6	b5	b4	b3	b2	b1	b0
1	1	1	1	RC3	RC2	RC1	RC0

(Read Operation)

RC3-RC0 – During a Request Register read, the state of the request bit associated with each channel is returned in bits 0 through 3 of the byte. The bit position corresponds to the channel number.

Request Mask Register

The Request mask register is a set of four bits which are used to inhibit external DMA requests from generating transfer cycles.

This register can be programmed in two ways. Each channel can be independently masked by writing to the Write Single Mask Bit location. The data format for this operation is shown below.

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	X	MB	MS1	MS0

(Set/Reset Operation)

MB – Bit 2 sets or resets the request mask bit for the channel selected by MS1 and MS0. Writing a 1 in this bit position sets the mask-bit, inhibiting external requests.

MS1-MS0 – These two bits select the specific mask bit which is to be set or reset.

MS1	MS0	Channel
0	0	Channel 0 select
0	1	Channel 1 select
1	0	Channel 2 select
1	1	Channel 3 select

Alternatively all four mask bits can be programmed in one operation by writing to the Write All Mask Bits address. Data format for this and the Read All Mask Bits function is shown below.

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	X	MB3	MB2	MB1	MB0

(Read/Write Operation)

MB3-MB0 – Each bit position in the field represents the mask bit of a channel. The mask bit number corresponds to the channel number associated with the mask bit.

All four mask bits are set following a RESET or a Master Clear command. Individual channel mask bits will be set as a result of terminal count being reached, if Autoinitialize is disabled. The entire register can be cleared, enabling all four channels, by performing a Clear Mask Register operation.

Status Register

The status of all four channels can be determined by reading the Status Register. Information is available to determine if a channel has reached terminal count and whether an external service request is pending. Bits 0-3 of this register are cleared by RESET, Master Clear or each time a Status Read takes place. Bits 4-7 are cleared by RESET, Master Clear or the pending request being deasserted. Bits 4-7 are not affected by the state of the Mask Register Bits. The channel number corresponds to the bit position.

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
DRQ3	DRQ2	DRQ1	DRQ0	TC3	TC2	TC1	TC0

(Read Only Register)

Temporary Register

The Temporary Register is used as a temporary holding register for data during memory-to-memory transfers. The register is loaded during the first cycle of a memory-to-memory transfer from XD0-XD7. During the second cycle of the transfer, the data in the Temporary Register is output on the XD0-XD7 pins. Data from the last memory-to-memory transfer will remain in the register unless a RESET or Master Clear occurs.

Special Commands

Five Special Commands are provided to make the task of programming the device easier. These commands are activated as a result of a specific address and assertion of either a $\overline{\text{XIOR}}$ or $\overline{\text{XIOW}}$. Information on the data lines is ignored by the SAB 82C206 whenever an $\overline{\text{XIOW}}$ activated command is issued, thus data returned on $\overline{\text{XIOR}}$ activated commands is invalid.

Clear Byte Pointer Flip-Flop – This command is normally executed prior to reading or writing to the address or word count registers. This initializes the flip-flop to point to the low byte of the register and allows the CPU to read or write register bytes in correct sequence.

Set Byte Pointer Flip-Flop – Setting the Byte Pointer Flip-Flop allows the CPU to adjust the pointer to the high byte of an address or word count register.

Master Clear – This command has the same effect as a hardware RESET. The Command Register, Status Register, Request Register, Temporary Register, Mode Register Counter and Byte Pointer Flip-Flop are cleared and the Request Mask Register is set. Immediately following Master Clear or RESET, the DMA will be in the Idle Condition.

Clear Request Mask Register – This command enables all four DMA channels to accept requests by clearing the mask bits in the Register.

Clear Mode Register Counter – In order to allow access to four Mode Registers while only using one address, an additional counter is used. After clearing the counter all four Mode Registers may be read by doing successive reads to the Read Mode Register address. The order in which the registers will be read is Channel 0 first, Channel 3 last.

Interrupt Controller Functional Description

The programmable interrupt controllers in the SAB 82C206 function as a system wide interrupt manager. They accept requests from peripherals, resolve priority on pending interrupts and interrupts in service, issue an interrupt request to the CPU, and provide a vector which is used as an index by the CPU to determine which interrupt service routine to execute.

A variety of priority assignment modes are provided, which can be reconfigured at any time during system operation, allowing the complete interrupt subsystem to be restructured based on the system environment.

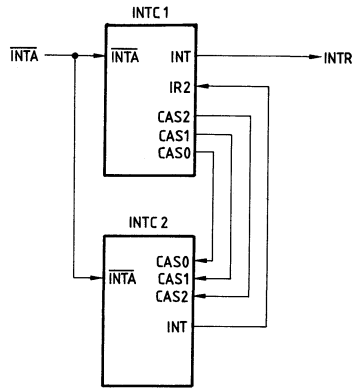
Overview

Two interrupt controllers, INTC1 and INTC2, are included in the SAB 82C206. Each of the interrupt controllers is equivalent to an 8259A device operating in the 86-Mode. The two controllers are interconnected and must be programmed to operate in Cascade Mode (see figure 5) for proper operation of all 16 interrupt channels. INTC1 is located at addresses 020H-021H and is configured for master operation (defined below) in Cascade Mode. INTC2 is a slave device (defined below) and is located at 0A0H-0A1H. The Interrupt Request output signal from INTC2 (INT) is internally connected to the interrupt request input Channel 2 (IR2) of INTC1. The address decoding and cascade interconnection matches that of the IBM PC/AT.

Two additional interconnections are made to the interrupt request inputs of the interrupt controllers. The output of Timer 0 in the Counter/Timer subsystem is connected to Channel 0 (IR0) of INTC1. Interrupt request from the Real Time Clock is connected to Channel 0 (IR0) of INTC2. Figure 5 lists the 16 interrupt channels and their interrupt request source.

The description of the Interrupt Subsystem will pertain to both INTC1 and INTC2 unless otherwise noted. Wherever register addresses are used, the address for the INTC1 register will be listed first and the address for the INTC2 register will follow in parenthesis. Example: 020H (0A0H).

Figure 5
Internal Cascade Interconnections



Controller Operation

Figure 6 shows a block diagram of the major elements in the interrupt controller. The Interrupt Request Register (IRR) is used to store requests from all of the channels which are requesting service. Interrupt Request Register bits are labeled using the Channel Name IR7-IR0. The In-Service Register (ISR) contains all the channels which are currently being serviced (more than one channel can be serviced at a time). In-Service Register bits are labeled IS7-IS0 and correspond to IR7-IR0. The Interrupt Mask Register (IMR) allows the CPU to disable any or all of the interrupt channels. The Priority Resolver evaluates inputs from the above three registers, issues an interrupt request, and latches the corresponding bit into the In-Service Register. During interrupt acknowledge cycles, a master controller outputs a code to the slave device which is compared in the Cascade Buffer/ Comparator with a 3-bit ID code previously written. If a match occurs in the slave controller, it will generate an interrupt vector. The contents of the Vector Register are used to provide the CPU with an interrupt vector during Interrupt Acknowledge ($\overline{\text{INTA}}$) cycles.

Interrupt Sequence

The SAB 82C206 allows the CPU to perform an indirect jump to a service routine in response to a request for service from a peripheral device. The indirect jump is based on a vector which is provided by the SAB 82C206 on the second of two CPU-generated $\overline{\text{INTA}}$ cycles (the first $\overline{\text{INTA}}$ cycle is used for resolving priority and the second cycle is for transferring the vector to the CPU). The events which occur during an interrupt sequence are as follows:

Table 4
Interrupt Request Sources

Controller Number	Channel Name	Interrupt Request Source
INTC1	IR0	Counter/Timer Out0
INTC1	IR1	IRQ1 Input Pin
INTC1	IR2	INTC2 Cascade Interrupt
INTC1	IR3	IRQ3 Input Pin
INTC1	IR4	IRQ4 Input Pin
INTC1	IR5	IRQ5 Input Pin
INTC1	IR6	IRQ6 Input Pin
INTC1	IR7	IRQ7 Input Pin
INTC2	IR0	Real Time Clock IRQ
INTC2	IR1	IRQ9 Input Pin
INTC2	IR2	IRQ10 Input Pin
INTC2	IR3	IRQ11 Input Pin
INTC2	IR4	IRQ12 Input Pin
INTC2	IR5	IRQ13 Input Pin
INTC2	IR6	IRQ14 Input Pin
INTC2	IR7	IRQ15 Input Pin

1 – One or more of the interrupt requests (IR7-IR0) becomes active, setting the corresponding IRR bit(s).

2 – The interrupt controller resolves priority based on the state of the IRR, IMR and ISR and asserts the INTR output if appropriate.

3 – The CPU accepts the interrupt and responds with an $\overline{\text{INTA}}$ cycle.

4 – During the first $\overline{\text{INTA}}$ cycle, the highest priority ISR bit is set and the corresponding IRR bit is reset. The internal Cascade address is generated and the XD7-XD0 outputs remain tristated.

5 – The CPU will excecute a second $\overline{\text{INTA}}$ cycle, during which the SAB 82C206 will drive an 8-bit vector onto the data pins XD7-XD0, which is in turn latched by the CPU. The format of this vector is shown in table 5. Note that V7-V3 in table 5 are programmable by writing to Initialization Control Word 2 (see Initialization Command Words section below).

6 – At the end of the second $\overline{\text{INTA}}$ cycle, the ISR bit will be cleared if the Automatic End Of Interrupt mode is selected (see End Of Interrupt section). Otherwise, the ISR bit must be cleared by an End Of Interrupt (EOI) command from the CPU at the end of the interrupt service routine.

If no interrupt request is present at the beginning of the first $\overline{\text{INTA}}$ cycle (i.e. a spurious interrupt) INTC1 will issue an interrupt level 7 vector during the second $\overline{\text{INTA}}$ cycle.

End of Interrupt

EOI is defined as the condition which causes an ISR bit to be reset. Determination of which ISR bit is to be reset can be done by a CPU command (specific EOI) or, the Priority Resolver can be instructed to clear the highest priority ISR bit (non-specific EOI).

Figure 6
Interrupt Controller Block Diagram

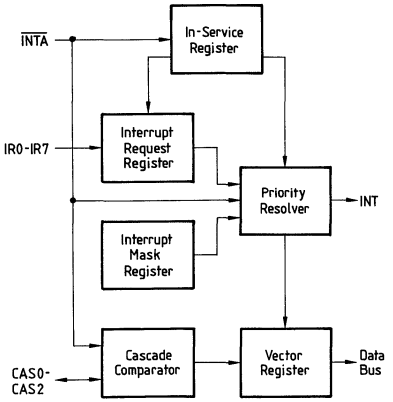
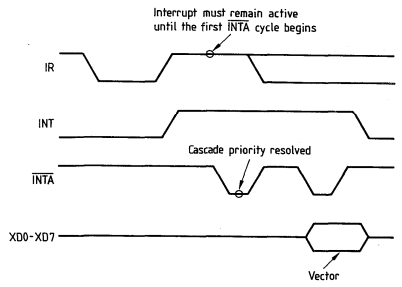


Figure 7
Interrupt Sequence



The SAB 82C206 can determine the correct ISR bit to reset when operated in modes which do not alter the fully nested structure, since the current highest priority ISR bit is necessarily the last level acknowledged and serviced. In conditions where the fully nested structure is not preserved, a specific EOI must be generated at the end of the interrupt service routine. An ISR bit that is masked, in Special Mask Mode by an IMR bit, will not be cleared by a non-specific EOI command. The interrupt controller can optionally generate an Automatic End Of Interrupt (AEOI) on the trailing edge of the second $\overline{INTA}$ cycle.

Priority Assignment

Assignment of priority is based on an interrupt channel's position relative to the other channels in the interrupt controller. After the initialization sequence, IR0 has the highest priority, IR7 has the lowest, and priority assignment is fixed (Fixed Priority Mode). Priority assignment can be rotated either manually (Specific Rotation Mode) or automatically (Automatic Rotation Mode) by programming Operational Command Word 2 (OCW2).

Fixed Priority Mode – This is the default condition which exists unless rotation (either manual or automatic) is enabled, or the controller is programmed for Polled Mode. In Fixed Priority Mode, interrupts are fully nested with priority assigned as shown:

	Lowest						Highest
Priority Status	7	6	5	4	3	2	1	0

Nesting allows interrupts of a higher priority to generate interrupt requests prior to the completion of the interrupt in service. When an interrupt is acknowledged, priority is resolved, the highest priority request's vector is placed on the bus and the ISR bit for that channel is set. This bit remains set until an EOI (automatic or CPU generated) is issued to that channel. While the ISR bit is set, all interrupts of equal or lower priority are inhibited. Note that a higher priority interrupt which occurs during an interrupt service routine, will only be acknowledged if the CPU has internally re-enabled interrupts.

Specific Rotation Mode – Specific Rotation allows the system softare to reassign priority levels by issuing a command which redefines the highest priority channel.

Before Rotation

	Lowest							Highest
Priority Status	7	6	5	4	3	2	1	0

(Specific Rotation command issued with Channel 5 specified).

After Rotation

	Lowest						Highest	
Priority Status	5	4	3	2	1	0	7	6

Automatic Rotation Mode – In applications where a number of equal priority peripherals are requesting interrupts, Automatic Rotation may be used to equalize the priority assignment. In this mode a peripheral, after being serviced, is assigned the lowest priority. All peripherals connected to the controller will be serviced at least once in 8 interrupt requests to the CPU from the controller. Automatic rotation will occur, if enabled, due to the occurrance of EOI (automatic or CPU-generated).

Before Rotation (IR4 highest priority request being serviced)

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	1	0	0	0	0

	Lowest						Highest	
Priority Status	7	6	5	4	3	2	1	0

After Rotation (IR4 service completed)

ISR Status Bit	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	0	0	0	0	0

	Lowest						Highest	
Priority Status	4	3	2	1	0	7	6	5

Programming the Interrupt Controller

Two types of commands are used to control the SAB 82C206 interrupt controllers, Initialization Command Words (ICWs) and Operational Command Words (OCWs).

Initialization Command Words

The Initialization process consists of writing a sequence of 4 bytes to each Interrupt Controller. The initialization sequence is started by writing the first Initialization Command Word (ICW1) to address 020H (0A0H) with a 1 on bit 4 of the data byte. The Interrupt Controller interprets this as the start of an initialization sequence and does the following:

1 – The Initialization Command Word Counter is reset to zero.
2 – ICW1 is latched into the device
3 – Fixed Priority Mode is selected
4 – IR7 is assigned the highest priority
5 – The Interrupt Mask Register is cleared
6 – The Slave Mode Address is set to 7
7 – Special Mask Mode is disabled
8 – The IRR is selected for Status Read operations

The next three I/O writes to address 021H (0A1H) will load ICW2-ICW4. See figure 8 for a flow chart of the initialization sequence. The initialization sequence can be terminated at any point (all 4 bytes must be written for the controller to be properly initialized) by writing to address 020H (0A0H) with a 0 in data bit 4. Note, this will cause OCW2 or OCW3 to be written.

Figure 8
Initialization Sequence

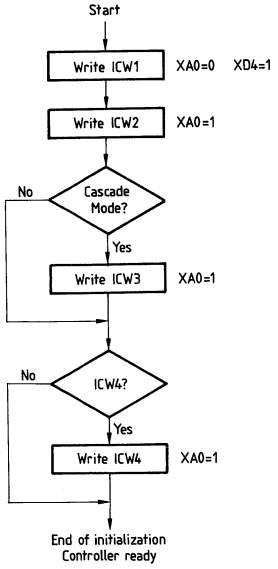


Table 5
Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	V7	V6	V5	V4	V3	1	1	1
IR6	V7	V6	V5	V4	V3	1	1	0
IR5	V7	V6	V5	V4	V3	1	0	1
IR4	V7	V6	V5	V4	V3	1	0	0
IR3	V7	V6	V5	V4	V3	0	1	1
IR2	V7	V6	V5	V4	V3	0	1	0
IR1	V7	V6	V5	V4	V3	0	0	1
IR0	V7	V6	V5	V4	V3	0	0	0

ICW1 – Address 020H (0A0H)

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	SI	LTM	X	SM	X

(Write Only Register)

SI – Bit 4 indicates to the interrupt controller that an Initialization Sequence is starting and must be a 1 to write ICW1.

LTM – Bit 3 selects level or edge triggered inputs to the IRR. If a 1 is written to LTM, a "high" level on the IRR input will generate an interrupt request. The IR must be active until the first $\overline{\text{INTA}}$ cycle is started to generate the proper interrupt vector (an IR7 vector will be generated if the IRR input is deasserted earlier) and the IR must be removed prior to EOI to prevent a second interrupt from occuring.

SM – Bit 1 selects between Single Mode and Cascade Mode. Single Mode is used whenever only one interrupt controller (INTC1) is used and is not recommended for this device. Cascade Mode allows the two interrupt controllers to be connected through IR2 of INTC1. INTC1 will allow INTC2 to generate its own interrupt vectors if Cascade Mode is selected and the highest priority IR pending is from an INTC2 input. INTC1 and INTC2 must be programmed for Cascade Mode for both devices to operate.

ICW2 – Address 021H (0A1H)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
V7	V6	V5	V4	V3	X	X	X

(Write Only Register)

V7-V3 – These bits are the upper 5 bits of the interrupt vector and are programmable by the CPU. The lower three bits of the vector are generated by the Priority Resolver during $\overline{\text{INTA}}$ (see table 5). INTC1 and INTC2 need not be programmed with the same value in ICW2.

ICW3 Format for INTC1 – Address 021H

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
S7	S6	S5	S4	S3	S2	S1	S0

(Write Only Register)

S7-S0 – Select which IR inputs have Slave Mode controllers connected. ICW3 in INTC1 must be written with a 04H for INTC2 to function.

ICW3 Format for INTC2 – Address 0A1H

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	ID2	ID1	ID0

(Write Only Register)

ID2-ID0 – Determine the Slave Mode address the controller will respond to during the cascaded $\overline{\text{INTA}}$ sequence. ICW3 in INTC2 should be written with a 02H for Cascade Mode operation. Note, b7-b3 should be zero.

ICW4 – Address 021H (0A1H)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
X	X	X	EMI	X	X	AEOI	X

(Write Only Register)

EMI – Bit 4 will Enable Multiple Interrupts from the same channel in Fixed Priority Mode. This allows INTC2 to fully nested interrupts, when Cascade Mode with Fixed Priority Mode are both selected, without being blocked by INTC1. Correct handling of this mode requires the CPU to issue a non-specific EOI command to INTC2 and check its In-Service Register for zero, when exciting an interrupt service routine. If zero, a non-specific EOI command should be sent to INTC1. If non-zero, no command is issued.

AEOI – Auto End Of Interrupt is enabled when ICW4 is written with a zero in bit 1. The interrupt controller will perform a non-specific EOI on the trailing edge of the second $\overline{\text{INTA}}$ cycle. Note, this function should not be used in a device with fully nested interrupts unless the device is a cascade Master.

Operational Command Words

Operational Command Words (OCWs) allow the SAB 82C206 Interrupt Controllers to be controlled or reconfigured at any time while operating. Each interrupt has 3 OCWs which can be programmed to effect the proper operating configuration and a Status Register to monitor controller operation.

Operational Command Word 1 (OCW1) is located at address 021H (0A1H) and may be written any time the controller is not in Initialization Mode. Operational Command Words 2 and 3 (OCW2, OCW3) are located at address 020H (0A0H). Writing to address 020H (0A0H) with a 0 in bit 4 will place the controller in operational mode and load OCW2 (if data bit 3 = 0) or OCW3 (if data bit 3 = 1).

OCW1 – Address 021H (0A1H)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
M7	M6	M5	M4	M3	M2	M1	M0

(Read/Write Register)

M7-M0 – These bits control the state of the Interrupt Mask Register. Each Interrupt Request can be masked by writing a 1 in the appropriate bit position (M0 controls IR0 etc.). Setting an IMR bit has no affect on lower priority requests. All IMR bits are cleared by writing ICW1.

OCW2 – Address 020H (0A0H)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
R	SL	EOI	SI	2/3	L2	L1	L0

(Write Only Register)

R – This bit in conjunction with SL and EOI selects operational function. Writing a 1 in bit 7 causes one of the rotate functions to be selected.

R	SL	EOI	Function
0	0	0	Rotate on auto EOI disable
0	0	1	Non-specific EOI Command
0	1	0	No operation
0	1	1	Specific EOI Command
1	0	0	Rotate on auto EOI enable
1	0	1	Rotate on non-specific EOI
1	1	0	Specific Rotate Command
1	1	1	Rotate on specific EOI

SL – This bit in conjunction with R and EOI selects operational function. Writing a 1 in this bit position causes a specific or immediate function to occur. All specific commands require L2-L0 to be valid except no operation.

EOI – This bit in conjunction with R and SL selects operational function. Writing a 1 in this bit position causes a function related to EOI to occur.

SI – Writing a 0 in this bit position takes the interrupt controller out of initialize mode and writes OCW2 or OCW3.

2/3 – If the I/O write places a 0 in bit 4 (SI), then writing a 0 in bit 3 (2/3) selects OCW2 and writing a 1 will select OCW3.

L2-L0 – These three bits are internally decoded to select which interrupt channel is to be affected by the Specific Command. L2-L0 must be valid during three of the four specific cycles (see SL).

OCW3 – Address 020H (0A0H)

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
0	ESMM	SMM	SI	2/3	PM	RR	RIS

(Write Only Register)

ESMM – Writing a 1 in this bit position enables the Set/Reset Special Mask Mode function controlled by bit 5 (SMM). ESMM allows the other functions in OCW3 to be accessed and manipulated without affecting the Special Mask Mode state.

SMM – If ESMM and SMM both are written with a 1 the Special Mask Mode is enabled. Writing a 1 to ESMM and a 0 to SMM disables Special Mask Mode. During Special Mask Mode, writing a 1 to any bit position inhibits interrupts and a 0 enables interrupts on the associated channel by causing the Priority Resolver to ignore the condition of the ISR.

SI – See SI on the left.

2/3 – See 2/3 on the left.

PM – Polled Mode is enabled by writing a 1 to bit 2 of OCW3, causing the SAB 82C206 to perform the equivalent of an $\overline{\text{INTA}}$ cycle during the next I/O read operation to the controller. The byte read during this cycle will have bit 7 set if an interrupt is pending. If bit 7 of the byte is set, the level of the highest pending request will be encoded on bits 2-0. The IRR will remain frozen until the read cycle is completed at which time the PM bit is reset.

RR – When the RR bit (bit 1) is 1, reading the Status Port at address 020h (0A0h) will cause the contents of IRR or ISR (determined by RIS) to be placed on XD7-XD0. Asserting PM forces RR to be reset.

RIS – This bit selects between the IRR and the ISR during Status Read operations if RR = 1.

Counter/Timer

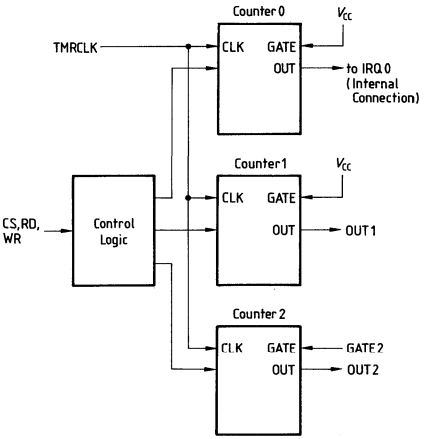
The Counter/Timer (CTC) in the SAB 82C206 is general purpose, and can be used to generate accurate time delays under software control. The CTC contains three 16-bit counters (Counter 0-3) which can be programmed to count in binary or binary coded decimal (BCD). Each counter operates independently of the other two and can be programmed for operation as a timer or a counter.

All three of the counters shown in Figure 9 are controlled from a common set of Control Logic. The Control Logic decodes control information written to the CTC and provides the controls necessary to load, read, configure and control each counter. Counter 0 and Counter 1 can be programmed for all six modes, but Mode 1 and Mode 5 have limited usefulness due to the absence of an external hardware trigger signal. Counter 2 can be operated in any of the six modes listed in the following.

Mode 0 Interrupt on terminal count
Mode 1 Hardware retriggerable one-shot
Mode 2 Rate generator
Mode 3 Square wave generator
Mode 4 Software triggered strobe
Mode 5 Hardware retriggerable strobe

All three counters in the CTC are driven from a common clock input pin (TMRCLK) which is independent from other clock inputs to the SAB 82C206. Counter 0's output (OUT0) is connected to IR0 of INTC1 (see Interrupt Controller, Functional Description) and may be used as an interrupt to the system for time keeping and task switching. Counter 1 may be programmed to generate pulses or square waves for use by external devices. The third counter (Counter 2) is a full function Counter/Timer. This channel can be used as an interval timer, a counter, or as a gated rate/pulse generator.

Figure 9
Counter/Timer Block Diagram



Counter Description

Each counter in the CTC contains a Control Register, a Status Register, a 16-bit Counting Element (CE), a pair of 8-bit Counter Input Latches (CIL, CIH), and a pair of 8-bit Counter Output Latches (COL, COH). Each counter also has a clock input for loading and decrementing the CE, a mode defined GATE input for controlling the counter (only GATE2 is externally accessible), and an OUT signal (OUT0 is not externally accessible). The OUT signal's state and function are controlled by the Counter Mode and condition of the CE (see Mode Definitions).

The Control Register stores the mode and command information used to control the counter. The Control Register may be loaded by writing a byte, containing a pointer to the desired counter, to the Write Control Word address (043H). The remaining bits in the byte contain the mode, the type of command, and count format information.

The Status Register allows the software to monitor counter condition and read back the contents of the Control Register.

The Counting Element is a loadable 16-bit synchronous down counter. The CE is loaded or decremented on the falling edge of TMRCLK. The CE contains the maximum count when a 0 is loaded, which is equivalent to 65536 in binary operation or 10000 in BCD. The CE does not stop when it reaches 0. In Modes 2 and 3 the CE will be reloaded and in all other modes it will wrap around to FFFF in binary operation or to 9999 in BCD operation.

The CE is indirectly loaded by writing one or two bytes (optional) to the Counter Input Latches, which are in turn loaded into the CE. This allows the CE to be loaded or reloaded in one TMRCLK cycle.

The CE is also read indirectly by reading the contents of the Counter Output Latches. COL and COH are transparent latches which can be read while transparent or latched (see Latch Counter Command).

Programming the CTC

After power-up the condition of CTC Control Registers, Counter Registers, CE, and the output of all counters is undefined. Each counter must be programmed before it can be used.

Counters are programmed by writing a Control Word and then read/write an initial count. The Control Register of a counter is written by writing to the Control Word address (see table 10). The Control Register is a write only location.

Control Word – (043H)

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
F3	F2	F1	F0	M2	M1	M0	BCD

(Write Only Register)

F3-F0 – Bits 7-4 determine the command to be performed.

M2-M0 – Bits 3-1 determine the counter's mode during Read/Write Counter Commands (see Read/Write Counter Command) or select the counter during a Read-Back Command (see Read Back Command). Bits 3-1 become "don't cares" during Latch Counter Commands.

BCD – Bit 0 selects binary coded decimal counting format during Read/Write Counter Commands. Note, during Read Back Command this bit must be 0.

Table 10
Counter/Timer Address Map

Address	Function
040H	Counter 0 Read/Write
041H	Counter 1 Read/Write
042H	Counter 2 Read/Write
043H	Control Register Write Only

Read/Write Counter Command

When writing to a counter, two conventions must be observed:

1 – Each counter's Control Word must be written before the initial count is written.

2 – Writing the initial count must follow the format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

A new initial count can be written into the counter at any time after programming without rewriting the Control Word providing the programmed format is observed.

During Read/Write Counter Commands M3-M0 are defined as follows:

M2	M1	M0	Function
0	0	0	Select Mode 0
0	0	1	Select Mode 1
X	1	0	Select Mode 2
X	1	1	Select Mode 3
1	0	0	Select Mode 4
1	0	1	Select Mode 5

Latch Counter Command

When a Latch Counter Command is issued, the counter's output latches (COL, COH) latch the current state of the CE. COL and COH remain latched until read by the CPU, or the counter is reprogrammed. The output latches then return to a "transparent" condition. In this condition the latches are enabled and the contents of the CE may be read directly.

F3	F2	F1	F0	Command
0	0	0	0	Latch Counter 0 (see Counter Latch Command)
0	0	0	1	Read/Write Counter 0 Lsb Only
0	0	1	0	Read/Write Counter 0 Msb Only
0	0	1	1	Read/Write Counter 0 Lsb then Msb
0	1	0	0	Latch Counter 1 (see Counter Latch Command)
0	1	0	1	Read/Write Counter 1 Lsb Only
0	1	1	0	Read/Write Counter 1 Msb Only
0	1	1	1	Read/Write Counter 1 Lsb then Msb
1	0	0	0	Latch Counter 2 (see Counter Latch Command) 2
1	0	0	1	Read/Write Counter 2 Lsb Only
1	0	1	0	Read/Write Counter 2 Msb Only
1	0	1	1	Read/Write Counter 2 Lsb then Msb
1	1	X	X	Read Back Command (see Counter Read Back Command)

Latch Counter Commands may be issued to more than one counter before reading the first counter to which the command was issued. Also, multiple Latch Counter Commands issued to the same counter without reading the counter will cause all but the first command to be ignored.

Read Back Command

The Read Back Command allows the user to check the count value, Mode, and state of the OUT signal and Null Count Flag of the selected counter(s).

The format of the Read-Back Command is:

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
1	1	LC	LS	C2	C1	C0	0

LC – Writing a 0 in bit 5 causes the selected counter(s) to latch the state of the CE in COL and COH.

LS – Writing a 0 in bit 4 causes the selected counter(s) to latch the current condition of its Control Register, Null Count and Output into the Status Register. The next read of the Counter will result in the contents of the Status Register being read (see Status Read).

C2-C0 – Writing a 1 in bit 3 causes Counter 3 to latch one or both of the registers specified by LC and LS. The same is true for bits 2 and 1 except that they enable Counters 1 and 0 respectively.

Each counter's latches remain latched until either the latch is read or the counter is reprogrammed.

If LS=LC=0, status will be returned on the next read from the counter. The next one or two reads (depending on whether the counter is programmed to transfer one or two bytes) from the counter result in the count being returned.

Status Byte

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
OUT	NC	F1	F0	M2	M1	M0	BCD

OUT – Bit 7 contains the state of the OUT signal of the counter.

NC – Bit 6 contains the condition of the Null Count Flag. This flag is used to indicate that the contents of the CE are valid. NC will be set to a 1 during a write to the Control Register or the counter. NC is cleared to a 0 whenever the counter is loaded from the counter input registers.

F1-F0 – Bits 5-4 contain the F1 and F0 Command bits which were written to the Command Register of the counter during initialization. This information is useful in determining whether the high byte, the low byte or both must be transferred during counter read/write operations.

M2-M0 – These bits reflect the mode of the counter and are interpreted in the same manner as in Write Command operations.

BCD – Bit 0 indicates that the CE is operating in BCD format.

Counter Operation

Due to the previously stated restrictions in Counter 0 and Counter 1, Counter 2 will be used as in the example describing counter operation, but the description of Mode 0, 2, 3 and 4 is relevant to all counters.

The following terms are defined for describing CTC operation.

TMRCLK pulse – A rising edge followed by a falling edge of the SAB 82C206 TMRCLK input.

Trigger – The rising edge of the GATE2 input.

Counter load – The transfer of the 16-bit value in CIL and CIH to the CE.

Initialized – A Control Word written and the Counter Input Latches loaded.

Counter 2 operates in one of the following modes.

Mode 0 – Interrupt on terminal count

Writing the Control Word causes OUT2 to go low and remain low until the CE reaches 0, at which time it goes back high and remains high until a new count or Control Word is written. Counting is enabled when GATE2=1. Disabling the count has no effect on OUT2.

The CE is loaded with the first TMRCLK pulse after the Control Word and initial count are loaded. When both CIL and CIH are written, the CE is loaded after CIH is written (see Write Operations). This TMRCLK pulse does not decrement the count, so for an initial count of N, OUT2 does not go high until N+1 TMRCLK pulses after initialization. Writing a new initial count to the counter reloads the CE on the next TMRCLK pulse and counting continues from the new count.

If an initial count is written with GATE2=0, it will still be loaded on the next TMRCLK pulse but counting does not begin until GATE2=1. OUT2, therefore, goes high N TMRCLK pulses after GATE2=1.

Mode 1 – Hardware retriggerable one-shot

Writing the Control Word causes OUT2 to go high initially. Once initialized the counter is armed and a trigger causes OUT2 to go low on the next TMRCLK pulse. OUT2 then remains low until the counter reaches 0. An initial count of N results in a one-shot pulse N TMRCLK cycles long.

Any subsequent triggers while OUT2 is low cause the CE to be reloaded, extending the length of the pulse. Writing a new count to CIL and CIH will not affect the current one-shot unless the counter is retriggered.

Mode 2 – Rate generator

Mode 2 functions as a divide-by-N counter, with OUT2 as the carry. Writing the Control Word during initialization sets OUT2 high.

When the initial count is decremented to 1, OUT2 goes low on the next TMRCLK pulse. The following TMRCLK pulse returns OUT2 high, reloads the CE and the process is repeated. In Mode 2 the counter continues counting (if GATE2=1) and will generate an OUT2 pulse every N TMRCLK cycles. Note that a count of 1 is illegal in Mode 2.

GATE2=0 disables counting and forces OUT2 high immediately. A trigger reloads the CE on the next TMRCLK pulse. Thus GATE2 can be used to synchronize the counter to external events.

Writing a new count while counting does not affect the current operation unless a trigger is received. Otherwise, the new count will be loaded at the end of the current counting cycle.

Mode 3 – Square wave generator

Mode 3 is similar to Mode 2 in every respect except for the duty cycle of OUT2. OUT2 is set high initially and remains high for the first half of the count. When the first half of the initial count expires, OUT2 goes low for the remainder of the count.

If the counter is loaded with an even count, the duty cycle of OUT2 will be 50% (high=low=N/2). For odd count values. OUT2 is high one TMRCLK cycle longer than it is low. Therefore, high = (N+1)/2 and low=(n-1)/2.

Mode 4 – Software triggered strobe

Writing the Control Word causes OUT2 to go high initially. Expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2=0 disables counting but has no effect on OUT2. Also, a trigger will not reload the CE.

The counting sequence is started by writing the initial count. The CE is loaded on the TMRCLK pulse after initialization. The CE begins decrementing one TMRCLK pulse later. OUT2 will go low for one TMRCLK cycle, (N+1) cycles after the initial count is written.

If a new initial count is written during a counting sequence, it is loaded into the CE on the next TMRCLK pulse and the sequence continues from the new count. This allows the sequence to be "retriggerable" by software.

Mode 5 – Hardware triggered strobe

Writing the Control Word causes OUT2 to go high initially. Counting is started by trigger. The expiration of the initial count causes OUT2 to go low for one TMRCLK cycle. GATE2 = 0 disables counting.

The CE is loaded on the TMRCLK pulse after a trigger. Since loading the CE inhibits decrementing, OUT2 will go low for one TMRCLK cycle (N+1) TMRCLK cycles after the trigger.

If a new count is loaded during counting, the current counting sequence will not be affected unless a trigger occurs. A trigger causes the counter to be reloaded from CIL and CIH, making the counter "retriggerable".

GATE2

In Modes 0, 2, 3 and 4 GATE2 is level sensitive and is sampled on the rising edge of TMRCLK. In Modes 1, 2, 3 and 5 the GATE2 input is rising-edge sensitive. This rising edge sets an internal flip-flop whose output is sampled on the next rising edge of TMRCLK. The flip-flop resets immediately after being sampled. Note that in Modes 2 and 3 the GATE2 input is both edge and level sensitive.

Table 11
Gate Pin Functions

Mode	Condition		
	Low	Rising	High
0	Disables Counting	–	Enables Counting
1	–	a) Initiates Counting b) Resets Out Pin	–
2	a) Disables Counting b) Forces Out Pin High	Initiates Counting	Enables Counting
3	a) Disables Counting b) Forces Out Pin High	Initiates Counting	Enables Counting
4	Disables Counting	–	Enables Counting
5	–	Initiates Counting	–

Real Time Clock

Functional Description

This section of the SAB 82C206 combines a complete time-of-day clock with alarm facility, one-hundred-year calendar, a programmable periodic interrupt, and 114 bytes of low-power static RAM. Provisions are made to enable the device to operate in a low power (battery powered) mode and protect the contents of both the RAM and clock during system power-up and power-down.

Register Access

Reading and writing to the 128 locations in the Real Time Clock is accomplished by first placing the Index Address of the location you wish to access on the data input pins XD0-XD6 and then strobing the AS input pin. The address will then be latched into the Index Address Register on the falling edge of AS. The Index Address Register is then used as a pointer to the specific byte in the Real Time Clock, which may be read or written to by asserting $\overline{\text{XIOR}}$ or $\overline{\text{XIOW}}$ with an address on the XA9-XA0 inputs of 071H.

Since AS will most likely be generated by an I/O operation which will result in the assertion of $\overline{\text{XIOW}}$, it is recommended that an address of 070H be applied to the XA9-XA0 inputs during this time. This will prevent the modification of other registers in the SAB 82C206.

Address Map

Table 12 illustrates the internal register RAM organization of the Real Time Clock portion of the SAB 82C206. The 128 addressable locations in the Real Time Clock are divided into 10 bytes which normally contain the time, calendar, and alarm data, four control and status bytes and 114 general purpose RAM bytes. All 128 bytes are readable by the CPU. The CPU may also write to all locations except Registers C, D, Bit 7 of Register A and Bit 7 of the Seconds Byte which is always 0.

Table 12
Address Map for Real Time Clock

Index	Function
00	SECONDS
01	SECONDS ALARM
02	MINUTES
03	MINUTES ALARM
04	HOURS
05	HOURS ALARM
06	DAY OF WEEK
07	DATE OF MONTH
08	MONTH
09	YEAR
0A	REGISTER A
0B	REGISTER B
0C	REGISTER C
0D	REGISTER D
0E	USER RAM
0F . . . 7E	USER RAM USER RAM
7F	USER RAM

Time Calendar and Alarm Bytes

The CPU can obtain the time and calendar information by reading the appropriate locations in the Real Time Clock. Initialization of the time, calendar and alarm information is accomplished by writing to these locations. Information is stored in these locations in binary-coded decimal (BCD) format.

Before initialization of the internal registers can be performed, the SET bit in Register B should be set to a "1" to prevent Real Time Clock updates from occuring. The CPU then initializes the first 10 locations in BCD format. The SET bit should then be cleared to allow updates. Once initialized and enabled, the Real Time Clock will perform Clock/Calendar updates at a 1 Hz rate.

Table 13
Time, Calendar, Alarm Data Format

Index Register Address	Function	BCD Range
0	Seconds	00-59
1	Seconds Alarm	00-59
2	Minutes	00-59
3	Minutes Alarm	00-59
4	Hours (12-hour mode) Hours (24-hour mode)	01-12 (AM) 81-92 (PM) 00-23
5	Hours Alarm (12-hour mode) Hours Alarm (24-hour-mode)	01-12 (AM) 81-92 (PM) 00-23
6	Day of Week	01-07
7	Day of Month	01-31
8	Month	01-12
9	Year	00-99

Table 13 shows the format for the ten clock, calendar and alarm locations. The 24/12 bit in Register B determines whether the hour locations will be updated using a 1-12 or 0-23 format. After initialization the 24/12 bit cannot be changed without reinitializing the hour locations. In 12-hour format the high-order bit of the hours byte in both the time and alarm bytes will indicate PM when it is a "1".

During updates, which occur once per second, the 10 bytes of time, calendar and alarm information are unavailable to be read or written by the CPU for a period of 2 ms. These 10 locations cannot be written during this time. Information read while the Real Time Clock is performing an update will be undefined. The Update Cycle section shows how to avoid Update Cycle/CPU contention problems.

The alarm bytes can be programmed to generate an interrupt at a specific time or a periodic interrupt. To generate an interrupt at a specific time, the user only needs to program the time at which the interrupt is to occur into the 3 alarm bytes. Alternatively, a periodic interrupt can be generated by setting the two high-order bits in an alarm register to a "1", which turns that byte into a "don't care". For instance, an interrupt can be generated every hour by programming a C0H into Register 5, or an interrupt can be generated once a second by programming the same value into all three alarm registers.

Static RAM

The 114 bytes of RAM from Index Address 0EH to 7FH are not affected by the Real Time Clock. These bytes are accessable during the update cycle and may be used for whatever the designer wishes. Typical applications will use this as nonvolatile storage for configuration and calibration parameters since this device is normally battery powered when the system is turned off.

Control and Status Registers

The SAB 82C206 contains four registers used to control the operation and monitor the status of the Real Time Clock. These registers are located at Index Address 0AH-0DH and are accessable by the CPU at all times.

REGISTER A (0AH)

Msb							**Lsb**
b7	b6	b5	b4	b3	b2	b1	b0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

(Read/Write register except UIP)

UIP – Update In Progress flag is a status bit used to indicate when an update cycle is about to take place. A "1" indicates that an update cycle is taking place or is imminent. UIP will go active (High) 224 µs prior to the start of an update cycle and will remain active for an additional 2 ms while the update is taking place. The UIP bit is read only and is not affected by Reset. Writing a "1" to the SET bit in Register B will clear the UIP status bit.

DV2-DV0 – These three bits are used to control the Divider/Prescaler on the Real Time Clock. While the SAB 82C206 can operate at frequencies higher than 32.768 kHz, this is not recommended for battery powered operation due to the increased power consumption at these higher frequencies.

Divider Options

DV2	DV1	DV0	OSC Freq.	Mode
0	0	0	4.194304 MHz	Operate
0	0	1	1.048576 MHz	Operate
0	1	0	32.768 KHz	Operate
1	1	X	Reset Divider	

RS3-RS0 – These four bits control the Periodic Interrupt rate. The Periodic Interrupt is derived from the Divider/Prescaler in the Real Time Clock and is separate from the Alarm Interrupt. Both the Alarm and Periodic Interrupts do, however, use the same interrupt channel in the Interrupt Controller. Use of the Periodic Interrupt allows the generation of interrupts at rates higher than once per second. Below are the interrupt rates for which the Real Time Clock can be programmed.

Periodic Interrupt Rate

Rate Selection				Time Base	
RS3	RS2	RS1	RS0	4.194304 MHz 1.048576 MHz	32.768 KHz
0	0	0	0	None	None
0	0	0	1	30.517 µs	3.90526 ms
0	0	1	0	61.035 µs	7.8125 ms
0	0	1	1	122.070 µs	122.070 µs
0	1	0	0	244.141 µs	244.141 µs
0	1	0	1	488.281 µs	488.281 µs
0	1	1	0	976.562 µs	976.562 µs
0	1	1	1	1.953125 ms	1.953125 ms
1	0	0	0	3.90625 ms	3.90625 ms
1	0	0	1	7.8125 ms	7.8125 ms
1	0	1	0	15.625 ms	15.625 ms
1	0	1	1	31.25 ms	31.25 ms
1	1	0	0	62.5 ms	62.5 ms
1	1	0	1	125 ms	125 ms
1	1	1	0	250 ms	250 ms
1	1	1	1	500 ms	500 ms

REGISTER B (0BH)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	0	0	24/12	DSE

(Read/Write Register)

SET – Writing a "0" to this bit enables the Update Cycle and allows the Real Time Clock to function normally. When set to a "1" the Update Cycle is inhibited and any cycle in progress is aborted. The SET bit is not affected by the RESET input pin.

PIE – The Periodic Interrupt Enable Bit controls the generation of interrupts based on the value programmed into the RS3-RS0 bits of Register A. This allows the user to disable this function without affecting the programmed rate. Writing a "1" to this bit enables the generation of periodic interrupts. This bit is cleared to a "0" by RESET.

AIE – The generation of alarm interrupts is enabled by setting this bit to a "1". Once this bit is enabled the Real Time Clock will generate an alarm whenever a match occurs between the programmed alarm and clock information. If the don't care condition is programmed into one or more of the Alarm Registers, this will enable the generation of periodic interrupts at rates of one second or greater. This bit is cleared by RESET.

UIE – The UIE (Update-Ended Interrupt Enable) bit is a read/write bit which enables the update-end flag (UF) bit in Register C to assert an interrupt. This bit is cleared by SET = 1 or RESET.

24/12 – The 24/12 control bit is used to establish the format of both the Hours and Hours Alarm bytes. If this bit is a "1", the Real Time Clock will interpret and update the information in these two bytes using the 24 hour mode. This bit can be read or written by the CPU and is not affected by RESET.

DSE – The Real Time Clock can be instructed to handle daylight saving time changes by setting this bit to a "1". This enables two exceptions to the normal time keeping sequence to occur on the last Sunday in April a.m. Setting this bit to a "0" disables the execution of these two exceptions. $\overline{\text{PSRSTB}}$ has no affect on this bit.

REGISTER C (0CH)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

(Read only register)

IRQF – The Interrupt Request Flag bit is set to a "1" when any of the conditions which can cause an interrupt is true and the interrupt enable for that condition is true. The condition which causes this bit to be set, also generates an interrupt. The logic expression for this flag is:

IRQF = PF & PIE
+ AF & AIE
+ UF & UIE

This bit and all other active bits in this register are cleared by reading the register or by activating the PSRSTB input pin. Writing to this register has no affect on the contents.

PF – The Periodic Interrupt Flag is set to a "1" when a transition, which is selected by RS3-RS0, occurs in the divider chain. This bit will become active, independent of the condition of the PIE control bit. The PF bit will then generate an interrupt and set IRQF if PIE is a "1".

AF – A "1" appears in the AF bit whenever a match has occurred between the time registers and alarm registers during an update cycle. This flag is also independent of its enable (AIE) and will generate an interrupt if AIE is true.

UF – The Update-Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to "1" the "1" in UF causes the IRQF bit to be a "1", generating an interrupt. UF is cleared by a Register C read or a RESET.

REGISTER D (0DH)

Msb							Lsb
b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

(Read only register)

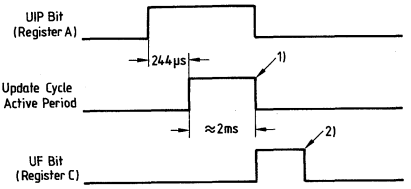
VRT – The Valid RAM and Time bit indicates the condition of the contents of the Real Time Clock. This bit is cleared to a "0" whenever the $\overline{\text{PSRSTB}}$ input pin is low. This pin is normally derived from the power supply which supplies V_{CC} to the device and will allow the user to determine whether the registers have been initialized since power was applied to the device. VRT has no affect on this bit and it can only be set by reading Register D. All unused register bits will be "0" when read and are not writable.

Update Cycle

During normal operation the Real Time Clock will perform an update cycle once every second. The performance of an update cycle is contingent upon the divider bits DV2-DV0 not being cleared, and the SET bit in Register B cleared. The function of the update cycle is to increment the Clock/Calendar registers and compare them to the Alarm Registers. If a match occurs between the two sets of registers, an alarm is generated and an interrupt will be issued if the alarm and interrupt control bits are enabled.

During the time that an update is taking place, the lower 10 registers are unavailable to the CPU. This is done to prevent the possible corruption of data in the registers or the reading of incorrect data. To avoid contention problems between the Real Time Clock and the CPU, a flag is provided in Register A to alert the user of an impending update cycle. This Update In Process Bit (UIP) is asserted 244 µs before the actual start of the cycle and is maintained until the cycle is complete. Once the cycle is complete the UIP bit will be cleared and the Update Flag (UF) in Register C will be set. Figure 10 illustrates the update cycle. CPU access is always allowed to Registers A through D during update cycles.

Figure 10
Update Cycle



Note:
1. Register 0-9 are unavailable to be read or written during this time.
2. If bit cleared by CPU read of Register C.

Two methods for reading and writing to the Real Time Clock are recommended. Both of these methods will allow the user to avoid contention between the CPU and the Real Time Clock for access to the time and date information.

The first method is to read Register A, determine the state of the UIP bit and if it is "0", perform the read or write operation. For this method to work successfully the entire read or write operation (including any interrupt service routines which might occur) must not require more than 244 µs to complete from the beginning of the read of Register A to the completion of the last read or write operation to the Clock Calendar Registers.

The second method of accessing the lower 10 registers is to read Register C once and disregard the contents. Then subsequently continue reading this register until the UF bit is a "1". This bit will become true immediately after an update has been completed. The user then has to complete a read or write operation until the start of the next update cycle.

Power-Up/Down

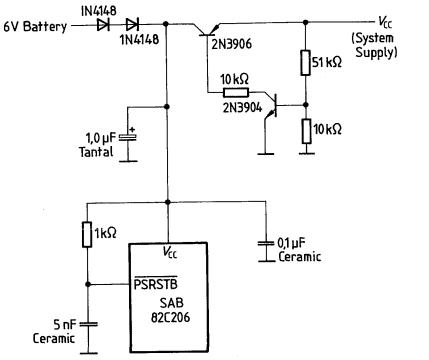
Most applications will require the Real Time Clock to remain active whenever the system power is turned off. To accomplish this the user must provide an alternative source of power to the SAB 82C206. This alternative source of power is normally provided by connecting a battery to the V_{CC} supply pin of the device. A means should be provided to switch from the system power supply to the battery. A circuit such as the one shown in Figure 11 may be used to eliminate power drain on the battery when the entire SAB 82C206 is active. The circuit shown here will allow for reliable transitions between system and battery power without undue battery power drain.

The user should also ensure that the V_{IN} maximum specification is never exceeded when powering the system up or down. Failure to observe this specification may result in damage to the device.

A pin is provided on the device to protect the contents of the Real Time Clock and reduce power consumption whenever the system is powered down. This pin (PWRGD) should be low whenever the system power supply is not within specifications for proper operation of the system. This signal may be generated by circuitry in either the power supply or on the system board. The PWRGD input will disable all unnecessary inputs during the time the system is powered down to prevent noise on the inactive pins from causing increased I_{CC}. This pin must therefore be inactive for the remainder of the device to operate properly when system power is applied.

One pin is provided to initialize the device whenever power is applied to the SAB 82C206. This pin ($\overline{\text{PSRSTB}}$) will not alter the RAM or Clock/Calendar contents but it will initialize the necessary control register bits. (See Pin Description for a list of the control register bits affected by $\overline{\text{PSRSTB}}$). Assertion of $\overline{\text{PSRSTB}}$ disables the generation of interrupts and sets a flag indicating that the contents of the device may not be valid. A recommended circuit for controlling the $\overline{\text{PSRSTB}}$ input is also shown in figure 11.

Figure 11
Power Conversion and Reset Circuitry



Absolute Maximum Ratings

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Supply voltage	−0.5 V to + 7.0 V
Voltage on any pin with respect to ground	−0.5 V to V_{CC} + 0.5 V
Power dissipation	1 W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ±10%; GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	–
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	–
V_{OL}	Output Low Voltage	–	0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	−2.0	–	V	I_{OH} = 2.0 mA
I_{IL}	Input Leakage Current	−10	10	µA	V_{IN} = V_{CC} to 0 V
I_{OL}	Output Leakage Current	−10	10	µA	V_{OUT} = V_{CC} to 0.45
I_{CC}	V_{CC} Supply Current	–	30	mA	SCLK Freq. = 8 MHz
I_{CCSB}	V_{CC} Standard Supply Current	–	10	µA	SCLK Freq. = DC

Capacitance [1)]

T_A = 25°C, V_{CC} = GND = 0 V

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{IN}	Input capacitance	–	10	pF	f_C = 1 MHz Unmeasured pins returned to GND
C_{IO}	I/O capacitance	–	20	pF	
C_{OUT}	Output capacitance	–	20	pF	

[1)] This parameter is periodically sampled and not 100% tested.

AC Characteristics

T_A = 0°C to 70°C; V_{CC} = +5 V ±10%; GND = 0 V

Symbol	Parameter	Limit values		Unit
		min.	max.	
t_1	Address Setup to Command Active	25	–	ns
t_2	Command Active Period	200	–	ns
t_3	Address Hold Time from Command Inactive	0	–	ns
t_4	Data Valid Delay	160	–	ns
t_5	Data Hold Time from $\overline{\text{XIOR}}$/$\overline{\text{INTA}}$ Inactive	10	–	ns
t_6	XD0-XD7 Active from $\overline{\text{XIOR}}$/$\overline{\text{INTA}}$	5	40	ns
t_7	Data Setup to $\overline{\text{XIOW}}$ Inactive	160	–	ns
t_8	Data Hold Time from $\overline{\text{XIOW}}$ Inactive	0	–	ns
t_9	Command Recovery Time	120	–	ns
t_{10}	Interrupt Request width (Low)	100	–	ns
t_{11}	Interrupt Request width (High)	200	–	ns
t_{12}	INT Output Delay	–	300	ns
t_{13}	IOCHRDY Delay from $\overline{\text{XIOR}}$/$\overline{\text{XIOW}}$ Active	–	TBD	ns
t_{14}	IOCHRDY Delay from SCLK	–	TBD	ns
t_{20}	Real Time Clock Cycle Time	–	500	ns
t_{21}	AS Pulse Width	160	–	ns
t_{22}	Data Valid Setup to AS Inactive	160	–	ns
t_{23}	Data Hold Time from AS Inactive	0	–	ns
t_{24}	OSCI Period	500	–	ns
t_{25}	OSCI High Time	200	–	ns
t_{26}	OSCI Low Time	200	–	ns
t_{27}	$\overline{\text{PSRSTB}}$ High Delay from V_{CC}	5	–	µs
t_{28}	$\overline{\text{PSRSTB}}$ Low Pulse Width	5	–	µs
t_{29}	VRT Bit Valid Delay	–	2	µs
t_{40}	TMRCLK Period	125	DC	ns
t_{41}	TMRCLK Low Time	50	–	ns
t_{42}	TMRCLK High Time	50	–	ns
t_{43}	GATE2 Setup to TMRCLK	50	–	ns
t_{44}	GATE2 Hold Time from TMRCLK	50	–	ns

AC Characteristics (cont'd)

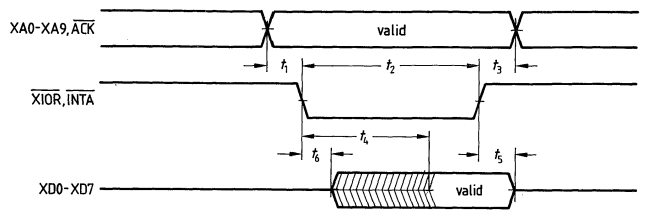
Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{45}	GATE2 Low Time	50	–	ns
t_{46}	GATE2 High Time	50	–	ns
t_{47}	OUT2 Delay from TMRCLK	–	120	ns
t_{48}	OUT2 Delay from GATE2	–	120	ns
t_{50}	SCLK Period (DMA clock = SCLK)	125	–	ns
t_{50A}	SCLK Period (DMA clock = SCLK/2	62	–	ns
t_{51}	SCLK Low Time (DMA clock = SCLK)	43	–	ns
t_{51A}	SCLK Low Time (DMA clock = SCLK/2)	22	–	ns
t_{52}	SCLK High Time (DMA clock = SCLK)	55	–	ns
t_{52A}	SCLK High Time (DMA clock = SCLK/2)	27	–	ns
t_{53}	DREQx Setup to SCLK	0	–	ns
t_{54}	HRQ Valid from SCLK	–	75	ns
t_{55}	HLDA Setup to SCLK	45	–	ns
t_{56}	$\overline{\text{AENx}}$ Valid Delay from SCLK	–	105	ns
t_{57}	$\overline{\text{AENx}}$ Invalid Delay from SCLK	TBD	80	ns
t_{58}	ADSTBx Valid Delay from SCLK	–	70	ns
t_{59}	ADSTBx Invalid Delay from SCLK	–	70	ns
t_{60}	XD0-XD7 Active Delay from SCLK	–	60	ns
t_{61}	XD0-XD7 Valid Setup to ADSTBx Low	65	–	ns
t_{62}	XD0-XD7 Hold Time from ADSTBx Low	25	–	ns
t_{63}	XD0-XD7 Tristate Delay from SCLK	–	135	ns
t_{64}	Address Valid Delay from SCLK	–	60	ns
t_{65}	Address Hold Time from $\overline{\text{DMAMEMR}}$ High	50	–	ns
t_{66}	Address Tristate Delay from SCLK	–	55	ns
t_{67}	DACKx Delay from SCLK	–	105	ns
t_{68}	Command Enable Delay from SCLK	–	90	ns
t_{69}	Command Active Delay from SCLK	–	120	ns
t_{70}	Write Command Inactive Delay from SCLK	–	80	ns
t_{71}	Address Hold Time from Write High	75	–	ns
t_{72}	Command Tristate Delay from SCLK	–	75	ns

AC Characteristics (cont'd)

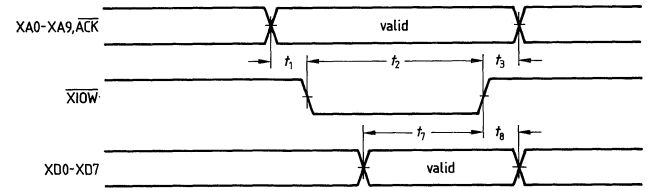
Symbol	Parameter	Limit values		Unit
		min.	max.	
t_{73}	Read Command Inactive Delay from SCLK	–	115	ns
t_{74}	TC Delay from SCLK	–	60	ns
t_{75}	XD0-XD7	90	–	ns
t_{76}	XD0-XD7 Hold from Read Command Inactive	0	–	ns
t_{77}	XD0-XD7 Valid Delay from SCLK	–	120	ns
t_{78}	XD0-XD7 Hold from Write Inactive	15	–	ns
t_{79}	IOCHRDY Input Setup to SCLK	35	–	ns
t_{80}	IOCHRDY Input Hold Time from SCLK	20	–	ns
t_{81}	RESET Pulse Width	TBD	–	ns
t_{82}	First $\overline{\text{XIOR}}$/$\overline{\text{XIOW}}$ Active after RESET	TBD	–	ns

Waveforms

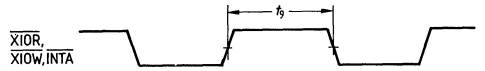
Peripheral Read/$\overline{\text{INTA}}$Cycle



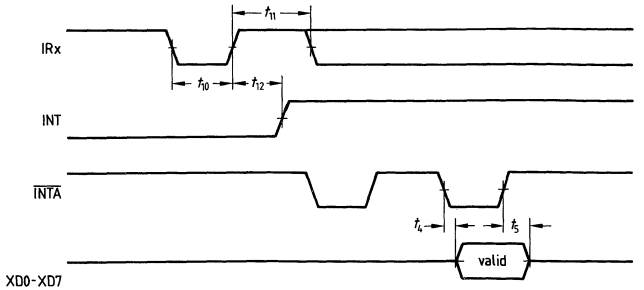
Peripheral Write Cycle



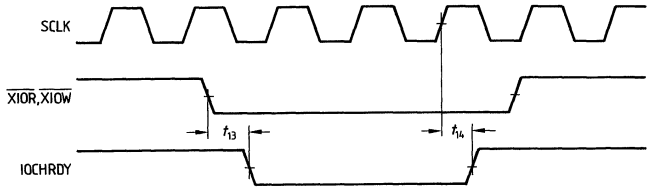
Command Recovery



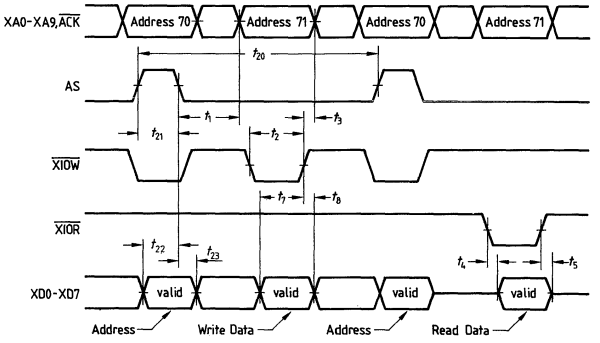
$\overline{\text{INTA}}$ Sequence



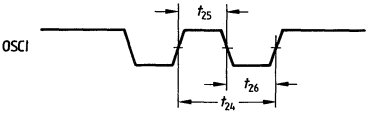
IOCHRDY OUTPUT



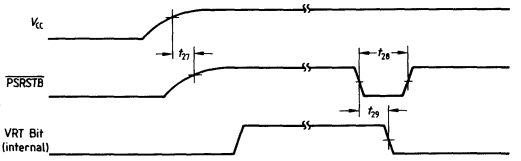
Real Time Clock Access Cycle



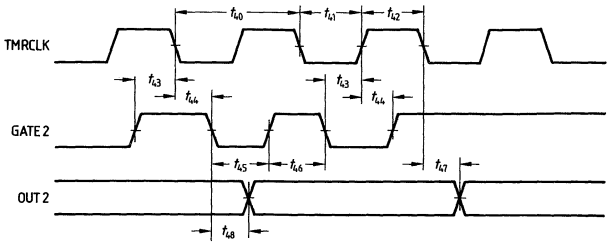
Real Time Clock Input



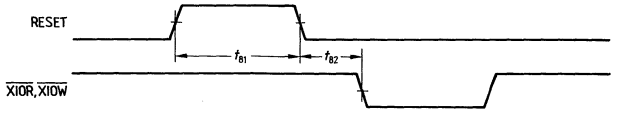
Real Time Clock Power-up Sequence



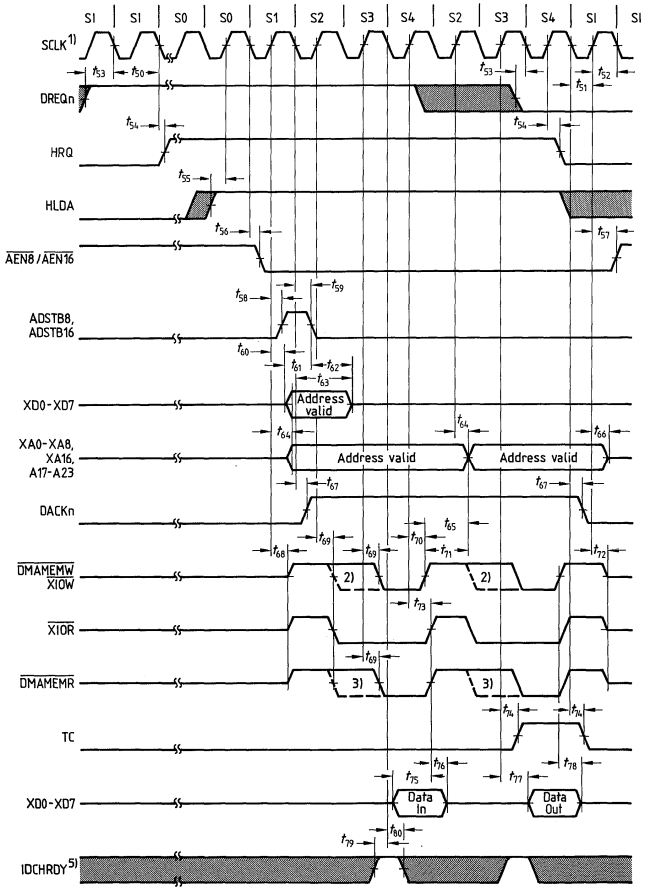
Counter/Timer Parameters



DMA Reset

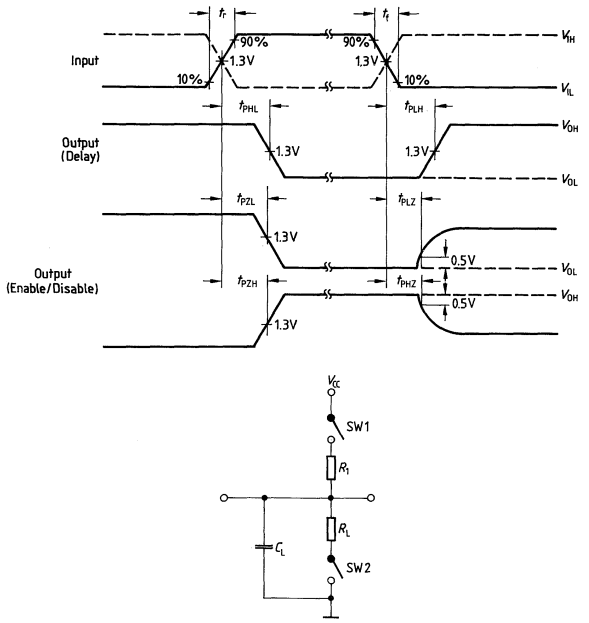


DMA Transfer Timing



1) All timings referenced to SCLK are independent of the state of the clock select bit in the configuration register. SCLK shown in this diagram is the undivided clock directly from the input.
2) Extended Write mode selected
3) Extended Read mode selected
4) Data Bus during Memory to Memory Transfer
5) IOCHRDY Input Timing

Load Circuit and AC Characteristics Measurement Waveform



Load Circuit Measurement Conditions

Parameter	Output Type	Symbol	C_L (pF)	R_1 (kΩ)	R_L (kΩ)	SW_1	SW_2
Propagation Delay Time	Totem Pole Tristate Bidirectional	 t_{PLH} t_{PHL}	 50 50	 – –	 1.0 1.0	OFF	ON
Propagation Delay Time	Open Drain or Open Collector	t_{PLH} t_{PHL}	50 50	0.5 0.5	– –	ON	OFF
Disable Time	Tristate Bidirectional	t_{PLZ} t_{PHZ}	5 5	0.5 0.5	1.0 1.0	ON OFF	 ON
Enable Time	Tristate Bidirectional	t_{PZL} t_{PZH}	50 50	0.5 0.5	1.0 1.0	ON OFF	ON ON

Package Outlines

In preparation

Ordering Information

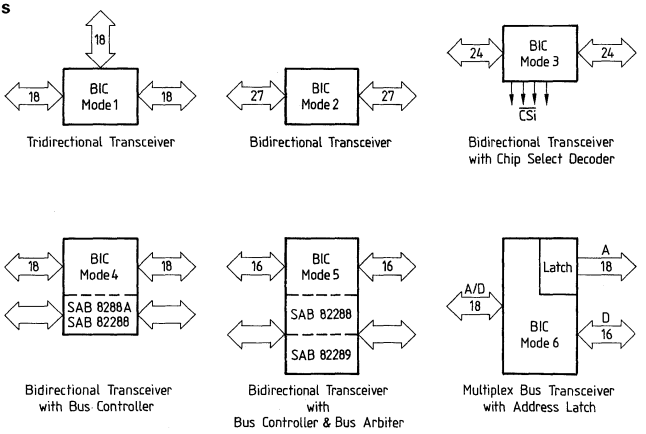
Type	Ordering code	Description
SAB 82C206-N	Q67120-P286	Integrated Peripheral Controller (PL-CC-84)

Preliminary

SAB 82220
Bus Interface Controller (BIC)

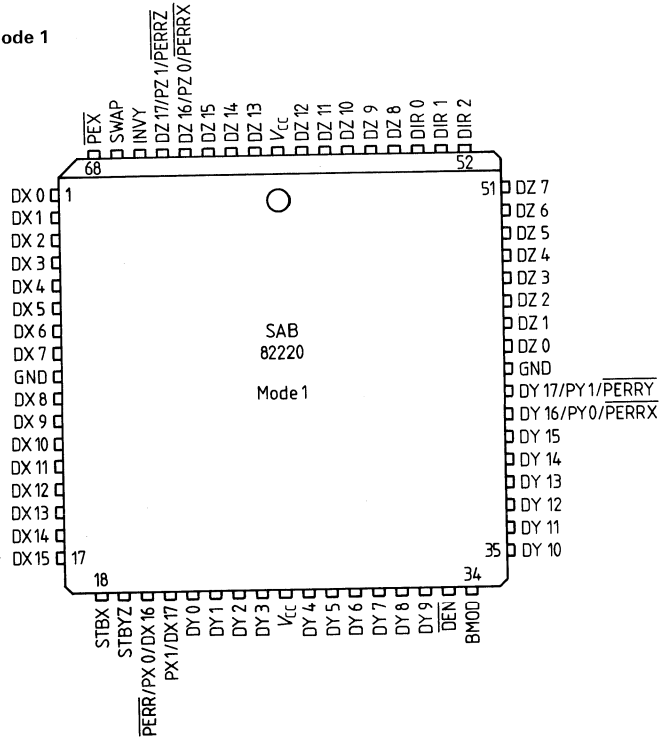
- Highly integrated microprocessor system support component
- Integrates into one package microprocessor interface logic, like bus drivers, bus control logic, etc.
- Reduction of
  - chip count up to 80%
  - board space up to 60%
  - power consumption up to 60%
  - design and test effort
  - cost
- Six modes of operation for flexible adaption to different applications
- Support of parity-protected bus systems
- Bus control and arbitration support for Siemens/ Intel 8/ 16-bit microprocessors SAB 8086/8088/ 80186/80188/80286
- Multibus I compatible bus drivers
- Low power consumption due to CMOS technology

Figure 1
Block Diagrams

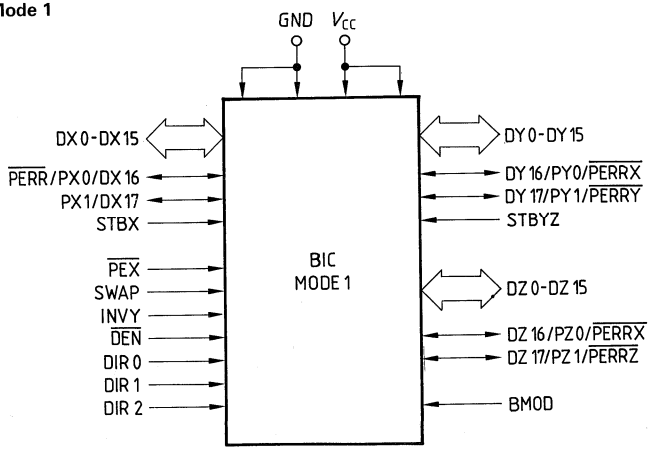


Designing modern high-performance microcomputer systems leads to multiprocessor architectures with multiple buses and/or dual-port memories. Those types of architecture require an increasing amount of interface logic. Designed with standard components, however, that logic would need many packages with a great number of interconnections and consume a lot of board space and power.
The SAB 82220 Bus Interface Controller (BIC) solves those problems by integrating many interface functions into one package, thus providing easy interface design. Flexible adaption to different systems and applications is supported by its six different modes of operation. The selection of the operating modes and the respective programming is done via strapping pins thus avoiding processor programming and control overhead. The BIC is housed in a 68-pin plastic leaded chip carrier package and fabricated in Siemens Advanced CMOS Technology.

Figure 2
Pin Configuration Mode 1



Logic Symbol Mode 1



Pin Definitions and Functions Mode 1

Symbol	Pin	Input (I) Output (O)	Function
DX0–DX15	1–8, 10–17	I/O	DATA PORT X: Bidirectional I/O lines of port X. The state of these lines (input, output or tristate) depends on the direction control input lines DIR0, DIR1 and DIR2 and the $\overline{DEN}$ input.
DX16/PX0/$\overline{PERR}$	20	I/O	DATA PORT X LINE 16: DX16 is an additional bidirectional I/O line of data port X. This feature is enabled if $\overline{PEX}$ = high (parity mode A).
		I	PARITY MODE SELECT 0: In parity mode C and D this input is used to select one of these two parity modes. If PX0 = low parity mode C is selected. Parity mode D is programmed with PX0 = high.
		O	$\overline{PARITY\ ERROR}$: $\overline{PERR}$ is an open-drain parity error output in parity mode B. In this parity mode, $\overline{PERR}$ must be tied to V_{CC} via a pullup resistor. If a parity error occurs, $\overline{PERR}$ goes low, $\overline{PERR}$ is enabled with $\overline{DEN}$ = low and deactivated by $\overline{DEN}$ = high.
DX17/PX1	21	I/O	DATA PORT X LINE 17: DX17 is an additional bidirectional I/O line of data port X. This feature is enabled if $\overline{PEX}$ = high (parity mode A).
		I	PARITY MODE SELECT 1 In parity mode B, C and D ($\overline{PEX}$ = low) this input is used as a mode select input. If PX1 = high parity mode B is selected. In parity mode C and D, PX1 is tied to low. Parity Mode Selection **Mode** | $\overline{PEX}$ | PX0 | PX1 A | 1 | X | X B | 0 | X | 1 C | 0 | 0 | 0 D | 0 | 1 | 0 X: not used for the specific parity mode selection
STBX	18	I	PORT X INPUT STROBE: STBX is the strobe signal which controls the port X input latch. The latch is transparent if STBX = high and the data port X is latched at the high-to-low transition of STBX.

Pin Definitions and Functions Mode 1 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
STBYZ	19	I	PORT Y/Z INPUT STROBE: STBYZ is a common strobe signal which controls the port Y or port Z input latch. It depends on the transfer direction whether the input latch of port Y or Z is activated by STBYZ. The latch is transparent if STBX = high and the data at port Y or Z is latched at the high-to-low transition of STBYZ.
DY0-DY15	22-25 27-32 35-40	I/O	DATA PORT Y: Bidirectional I/O lines of port Y. The state of these lines (input, output or tristate) depends on the direction control input lines DIR0, DIR1 and DIR2 and the $\overline{DEN}$ input. Port Y may have inverted signal polarity (see INVY).
DY16/PY0/$\overline{PERRX}$	41	I/O	DATA PORT Y LINE 16: DY16 is an additional bidirectional I/O line of data port Y. This feature is enabled if $\overline{PEX}$ = high (parity mode A).
		I/O	PARITY BIT Y0: In parity mode B and C, PY0 is the parity input/output line which is related to DY0-7. During a data transfer from port Y, PY0 is an input to the parity checker. If the transfer is destinated to port Y, PY0 is an output of the parity generator.
		O	$\overline{PORT\ X\ PARITY\ ERROR}$: $\overline{PERRX}$ is an open-drain parity error output in parity mode D. In this parity mode, $\overline{PERRX}$ must be tied to V_{CC} via a pullup resistor. If a parity error occurs during a transfer from port Z to port X, $\overline{PERRX}$ goes low. $\overline{PERRX}$ is enabled with $\overline{DEN}$ = low and deactivated by $\overline{DEN}$ = high.
DY17/PY1/$\overline{PERRY}$	42	I/O	DATA PORT Y LINE 17: DY17 is an additional bidirectional I/O line of data port Y. This feature is enabled if $\overline{PEX}$ = low (parity mode A).
		I/O	PARITY BIT Y1: In parity mode B and C, PY1 is the parity input/output line which is related to DY8-15. During a data transfer from port Y, PY1 is an input to the parity checker. If the transfer is destinated to port Y, PY1 is an output of the parity generator.
		O	$\overline{PORT\ Y\ PARITY\ ERROR}$: $\overline{PERRY}$ is an open-drain parity error output in parity mode D. In this parity mode, $\overline{PERRY}$ must be tied to V_{CC} via a pullup resistor. If a parity error occurs during a transfer from port Z to port Y, $\overline{PERRY}$ goes low. $\overline{PERRY}$ is enabled with $\overline{DEN}$ = low and deactivated by $\overline{DEN}$ = high.

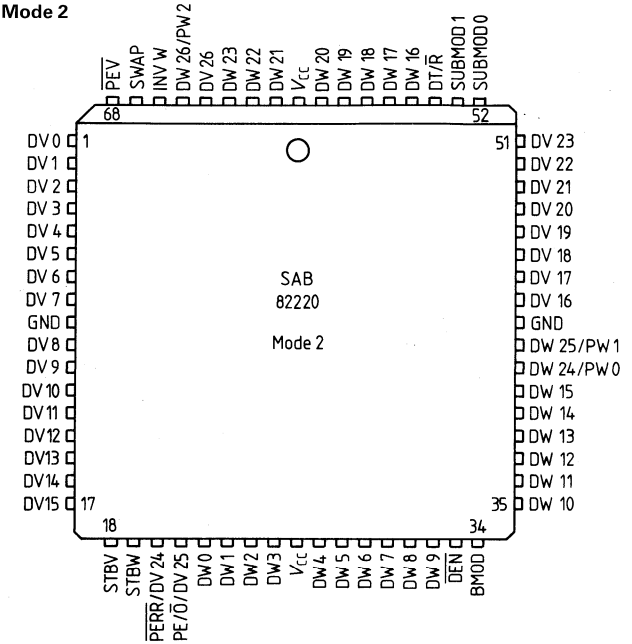
Pin Definitions and Functions Mode 1 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{DEN}$	33	I	$\overline{DATA\ ENABLE}$: $\overline{DEN}$ = low enables the output port lines and the parity outputs. If $\overline{DEN}$ = high the output port lines and the parity outputs are driven into the high-impedance state and the parity error outputs are driven inactive.
BMOD	34	I	BASE MODE: BMOD is an operating mode select input. For mode 1 BMOD must be tied to GND.
DZ0-DZ15	44-51 55-59 61-63	I/O	DATA PORT Z: Bidirectional I/O lines of port Z. The state of these lines (input, output or tristate) depends on the direction control input lines DIR0, DIR1 and DIR2 and the $\overline{DEN}$ input.
DZ16/PZ0/$\overline{PERRX}$	64	I/O I/O O	DATA PORT Z LINE 16: DZ16 is an additional bidirectional I/O line of data port Z. This feature is enabled if $\overline{PEX}$ = high (parity mode A). PARITY BIT Z0: In parity mode B and D, PZ0 is the parity input/output line which is related to DZ0-7. During a data transfer from port Z, PZ0 is an input to the parity checker. If the transfer is destinated to port Z, PZ0 is an output of the parity generator. $\overline{PORT\ X\ PARITY\ ERROR}$: $\overline{PERRX}$ is an open-drain parity error output in parity mode C. In this parity mode, $\overline{PERRX}$ must be tied to V_{CC} via a pullup resistor. If a parity error occurs during a transfer from port Y to port X, $\overline{PERRX}$ goes low. $\overline{PERRX}$ is enabled with $\overline{DEN}$ = low and deactivated by $\overline{DEN}$ = high.
DZ17/PZ1/$\overline{PERRZ}$	65	I/O I/O O	DATA PORT Z LINE 17: DZ17 is an additional bidirectional I/O line of data port Z. This feature is enabled if $\overline{PEX}$ = high (parity mode A). PARITY BIT Z1: In parity mode B and D, PZ1 is the parity input/output line which is related to DZ8-15. During a data transfer from port Z, PZ1 is an input to the parity checker. If the transfer is destinated to port Z, PZ1 is an output of the parity generator. $\overline{PORT\ Z\ PARITY\ ERROR}$: $\overline{PERRZ}$ is an open-drain parity error output in parity mode C. In this parity mode, $\overline{PERRZ}$ must be tied to V_{CC} via a pullup resistor. If a parity error occurs during a transfer from port Y to port Z, $\overline{PERRZ}$ goes low. $\overline{PERRZ}$ is enabled with $\overline{DEN}$ = low and deactivated by $\overline{DEN}$ = high.

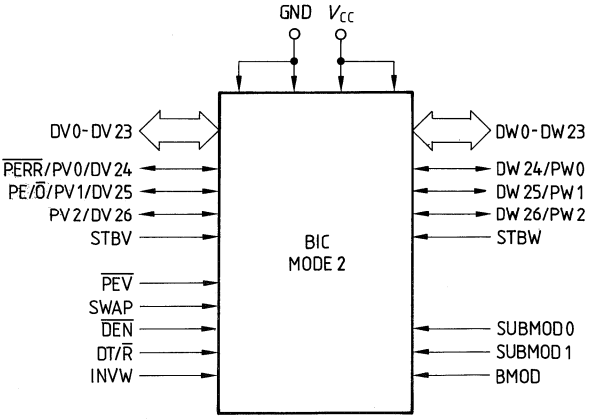
Pin Definitions and Functions Mode 1 (cont'd)

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>DIR2
DIR1
DIR0</td><td>52
53
54</td><td>I
I
I</td><td>DIRECTION CONTROL INPUT:
DIR0, DIR1 and DIR2 arbitrate the direction of the data transfer between the 3 bidirectional I/O ports of mode 1. The 3 direction lines are latched with STBX or STBYZ.
<table>
<tr><th rowspan="2">Transfer Direction</th><th colspan="3">Port Configuration</th><th colspan="3">Port Configuration</th></tr>
<tr><th>DIR2</th><th>DIR1</th><th>DIR0</th><th>Port X</th><th>Port Y</th><th>Port Z</th></tr>
<tr><td>Z → Y</td><td>0</td><td>0</td><td>0</td><td>X</td><td>Output</td><td>Input</td></tr>
<tr><td>Y → Z</td><td>0</td><td>0</td><td>1</td><td>X</td><td>Input</td><td>Output</td></tr>
<tr><td>X → Y</td><td>0</td><td>1</td><td>0</td><td>Input</td><td>Output</td><td>X</td></tr>
<tr><td>Y → X</td><td>0</td><td>1</td><td>1</td><td>Output</td><td>Input</td><td>X</td></tr>
<tr><td>Z → X</td><td>1</td><td>0</td><td>0</td><td>Output</td><td>X</td><td>Input</td></tr>
<tr><td>X → Z</td><td>1</td><td>0</td><td>1</td><td>Input</td><td>X</td><td>Output</td></tr>
<tr><td>Y → X</td><td>1</td><td>1</td><td>0</td><td>Output</td><td>Input</td><td>X</td></tr>
<tr><td>X → Y</td><td>1</td><td>1</td><td>1</td><td>Input</td><td>Output</td><td>X</td></tr>
</table>
X: Tristate</td></tr>
<tr><td>INVY</td><td>66</td><td>I</td><td>INVERT PORT Y:
The polarity of port Y may be inverted with INVY = high. In this case input and output data at port Y, including parity lines, is inverted.</td></tr>
<tr><td>SWAP</td><td>67</td><td>I</td><td>SWAP:
During a data transfer data at the input port is swapped bytewise to the output port by activating SWAP = high. In this case the input data lines 0-7 (8-15) are transferred to the output data lines 8-15 (0-7). SWAP is latched with STBX or STBYZ. If a parity mode B-D is enabled, the parity inputs/outputs are also swapped.</td></tr>
<tr><td>$\overline{PEX}$</td><td>68</td><td>I</td><td>$\overline{PARITY\ ENABLE}$:
If $\overline{PEX}$ = low, parity mode B, C or D is selected and the parity checker and parity generator is active. With $\overline{PEX}$ = high, the parity logic are disabled and the data ports have a width of 18 bits (parity mode A).</td></tr>
<tr><td>V_{CC}</td><td>26, 60</td><td>–</td><td>POWER SUPPLY (+5V)</td></tr>
<tr><td>GND</td><td>9, 43</td><td>–</td><td>GROUND (0V)</td></tr>
</table>

Figure 3
Pin Configuration Mode 2



Logic Symbol Mode 2



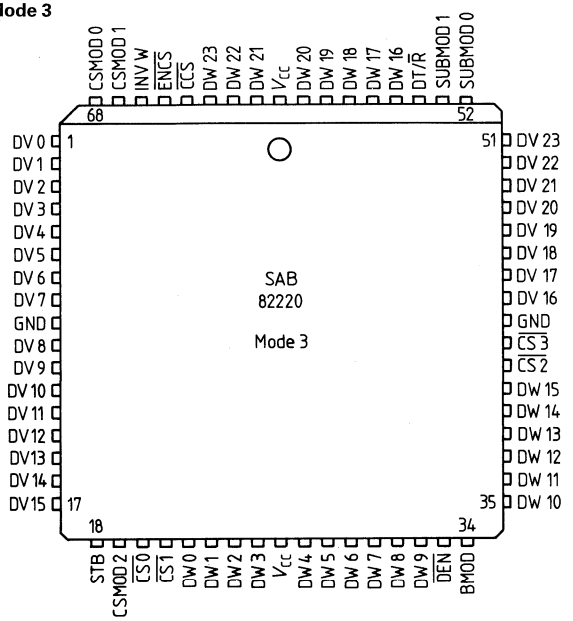
Pin Definitions and Functions Mode 2

Symbol	Pin	Input (I) Output (O)	Function
DV0-DV23	1-8 10-17 44-51	I/O	DATA PORT V: Bidirectional I/O lines of port V. The state of these lines (input, output or tristate) depends on the direction control input DT/$\overline{R}$ and the $\overline{DEN}$ input.
DV24/$\overline{PERR}$	20	I/O O	DATA PORT V LINE 24: DV24 is an additional bidirectional I/O line of data port V if $\overline{PEV}$ = high. $\overline{PARITY\ ERROR}$: $\overline{PERR}$ is an open drain parity error output in parity mode B ($\overline{PEV}$ = low). In this parity mode, $\overline{PERR}$ must be tied to V_{CC} via a pullup resistor. If a parity error occurs during a transfer from port W to port V, $\overline{PERR}$ goes low. $\overline{PERR}$ is enabled with $\overline{DEN}$ = low and deactivated by $\overline{DEN}$ = high.
DV25/PE/$\overline{O}$	21	I/O I	DATA PORT V LINE 25: DV25 is an additional bidirectional I/O line of data port V if $\overline{PEV}$ = high. PARITY EVEN/$\overline{ODD}$: PE/$\overline{O}$ is a select signal for even or odd parity generating and checking. This input is available only in parity mode B ($\overline{PEV}$ = low).
DV26	64	I/O	DATA PORT V LINE 26: DV26 is an additional bidirectional I/O line of data port V if $\overline{PEV}$ = high. In parity mode B ($\overline{PEV}$ = low) DV26 is an unused pin.
STBV	18	I	PORT V INPUT STROBE: STBV is the strobe signal which controls the port V input latch. The latch is transparent if STBV = high and the data at port V is latched at the high-to-low transition of STBV.
STBW	19	I	PORT W INPUT STROBE: STBW is the strobe signal which controls the port W input latch. The latch is transparent if STBW = high and the data at port W is latched at the high-to-low transition of STBW.
DW0-DW23	22-25 27-32 35-40 55-59 61-63	I/O	DATA PORT W: Bidirectional I/O lines of port W. The state of these lines (input, output or tristate) depends on the direction control input DT/$\overline{R}$ and the $\overline{DEN}$ input. Port W may have inverted signal polarity (see INVW).

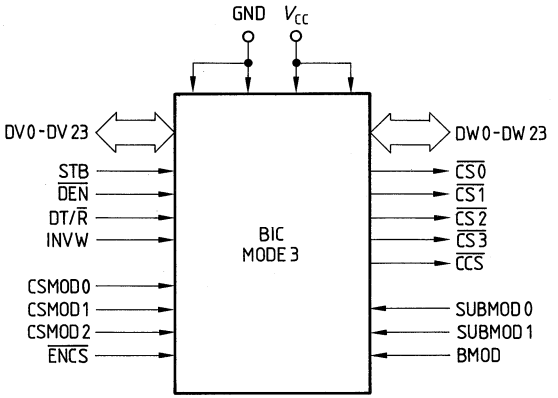
Pin Definitions and Functions Mode 2 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
DW24/PW0 DW25/PW1 DW26/PW2	41 42 65	I/O	DATA PORT W LINE 24-26: DW 24-26 are additional bidirectional I/O lines of data port W if $\overline{PEV}$ = high.
		I/O	PARIT BIT W0-2: In parity mode B ($\overline{PEV}$ = low) PW0-2 are parity input/output lines. PW0 is related to DW0-7, PW1 to DW8-15 and PW2 to DW16-23. During a data transfer from port W, PW0-2 are inputs to the parity checker. If the transfer is designated to port W, PW0-2 are outputs of the parity generator.
$\overline{DEN}$	33	I	$\overline{DATA\ ENABLE}$: $\overline{DEN}$ = low enables the output port lines and the parity outputs. If $\overline{DEN}$ = high the output port lines and the parity outputs are driven into the high-impedance state and the parity error output is driven inactive.
BMOD	34	I	BASE MODE: BMOD is an operating mode select input. For operating mode 2, BMOD must be tied to V_{CC}.
SUBMOD0 SUBMOD1	52 53	I	SUBMODE CONTROL: SUBMOD0 and SUBMOD1 are mode select inputs. For operating mode 2, both select inputs must be tied to GND.
DT/$\overline{R}$	54	I	DATA TRANSMIT/$\overline{RECEIVE}$: DT/$\overline{R}$ determines the transfer direction of a data transfer. With DT/$\overline{R}$ = low (high) a transfer is achieved from port W(V) to V(W). DT/$\overline{R}$ is latched with STBV or STBW.
INVW	66	I	INVERT PORT W: The polarity of port W may be inverted with INVW = high. In this case input and output data at port W, including parity lines, is inverted.
SWAP	67	I	SWAP: During a data transfer data at the input port is swapped bytewise to the output port by activating SWAP = high. In this case the input data lines 0-7 (8-15) are transferred to the output data lines 8-15 (0-7). SWAP is latched with STBV or STBW. The port lines 16-26 are not affected by SWAP.
$\overline{PEV}$	68	I	$\overline{PARITY\ ENABLE}$: If $\overline{PEV}$ = low, parity mode B is selected and the parity checker and parity generator are active. With $\overline{PEV}$ = high, the parity logic is disabled and the data ports have a width of 27 bits (parity mode A).
V_{CC}	26, 60	–	POWER SUPPLY (+5V)
GND	9, 43	–	GROUND (0V)

Figure 4
Pin Configuration Mode 3



Logic Symbol Mode 3



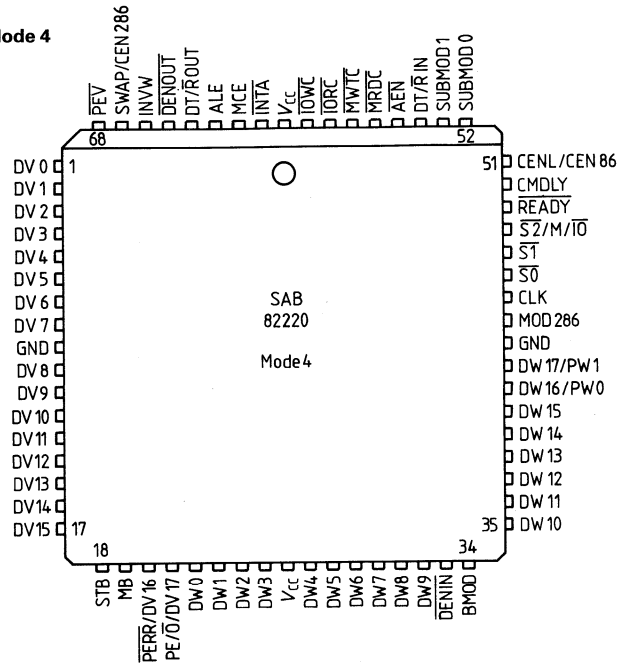
Pin Definitions and Functions Mode 3

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>DV0-DV23</td><td>1-8
10-17
44-51</td><td>I/O</td><td>DATA PORT V:
Bidirectional I/O lines of port V. The state of these lines (input, output or tristate) depends on the direction control input DT/$\overline{R}$ and the $\overline{DEN}$ input.</td></tr>
<tr><td>STB</td><td>18</td><td>I</td><td>INPUT STROBE:
STB is a common strobe signal which controls the port V or port W input latch. With DT/$\overline{R}$ = low (high) the input latch of port W (V) is selected. The latch is transparent if STB = high and the data at the input port is latched at the high-to-low transition of STB.</td></tr>
<tr><td>CSMOD0
CSMOD1
CSMOD2</td><td>67
68
19</td><td>I</td><td>CHIP SELECT MODE 0-2:
CSMOD0-2 are used to select the address ranges (sub-modes) of the chip select decoder. In the submodes with CSMOD2 = low, all 4 chip select outputs may go active. In a submode with CSMOD2 = high, either $\overline{CS0}$ and $\overline{CS1}$ or $\overline{CS2}$ and $\overline{CS3}$ are deactivated.
<table>
<tr><th colspan="3">CSMOD</th><th colspan="2">Chip Select Outputs</th></tr>
<tr><th>2</th><th>1</th><th>0</th><th>Address Range</th><th>Active Lines</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>256 Byte</td><td>$\overline{CS0}$-$\overline{3}$</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>128 Kbyte</td><td>$\overline{CS0}$-$\overline{3}$</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>16 Kbyte</td><td>$\overline{CS0}$-$\overline{3}$</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>512 Kbyte</td><td>$\overline{CS0}$-$\overline{3}$</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>256 Byte</td><td>$\overline{CS0}$, $\overline{CS1}$</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>128 Kbyte</td><td>$\overline{CS2}$, $\overline{CS3}$</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>256 Byte</td><td>$\overline{CS0}$, $\overline{CS1}$</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>512 Kbyte</td><td>$\overline{CS2}$, $\overline{CS3}$</td></tr>
</table>
The address ranges in the table above are related to a single chip select output.</td></tr>
<tr><td>$\overline{CS0}$-$\overline{CS3}$</td><td>20, 21
41, 42</td><td>O</td><td>$\overline{CHIP\ SELECT\ 0\text{-}3}$:
Chip select outputs of the chip select decoder. If the input data at port V or port W is inside a specific range, programmed via CSMOD0-2, one of the chip select outputs goes active (low). $\overline{CS0}$-$\overline{CS3}$ may go active only if $\overline{ENCS}$ = low and $\overline{DEN}$ = low.</td></tr>
<tr><td>DW0-DW23</td><td>22-25
27-32
35-40
55-59
61-63</td><td>I/O</td><td>DATA PORT W:
Bidirectional I/O lines of port W. The state of these lines (input, output or tristate) depends on the direction control input DT/$\overline{R}$ and the $\overline{DEN}$ input.</td></tr>
<tr><td>$\overline{DEN}$</td><td>33</td><td>I</td><td>$\overline{DATA\ ENABLE}$:
$\overline{DEN}$ = low enables the output port lines and the 5 chip select outputs. With $\overline{DEN}$ = high the output port lines and the 5 chip select outputs are tristated.</td></tr>
</table>

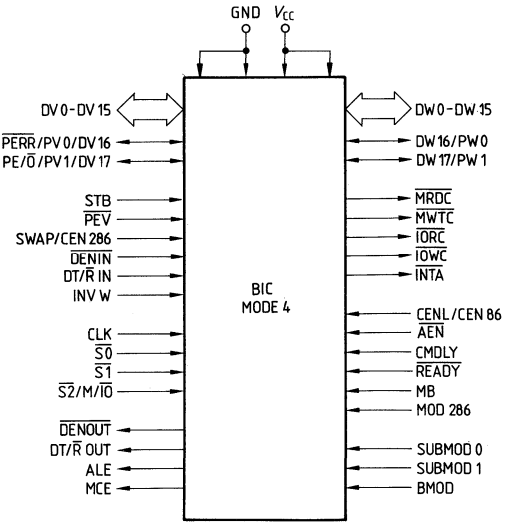
Pin Definitions and Functions Mode 3 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
BMOD	34	I	BASE MODE: BMOD is an operating mode select input. In operating mode 3, BMOD must be tied to V_{CC}.
SUBMOD0 SUBMOD1	52 53	I	SUBMODE CONTROL: SUBMOD0 and SUBMOD1 are mode select inputs. For operating mode 3 SUBMOD0 must be tied to V_{CC} and SUBMOD1 to GND.
DT/$\overline{R}$	54	I	DATA TRANSMIT/$\overline{\text{RECEIVE}}$: DT/$\overline{R}$ determines the transfer direction of a data transfer. With DT/$\overline{R}$ = low (high) a transfer is achieved from port W (V) to port V (W). DT/$\overline{R}$ is latched with STB.
$\overline{CCS}$	64	I	$\overline{\text{COMMON CHIP SELECT}}$: If one of the 4 chip select outputs is activated also $\overline{CCS}$ becomes active (low). $\overline{CCS}$ is affected by $\overline{ENCS}$ and $\overline{DEN}$.
$\overline{ENCS}$	65	I	$\overline{\text{ENABLE CHIP SELECT}}$: $\overline{ENCS}$ = high forces the chip select outputs $\overline{CS0\text{-}3}$ and $\overline{CCS}$ to the inactive state (high). With $\overline{ENCS}$ = low all 5 chip select outputs are enabled.
INVW	66	I	INVERT PORT W: The polarity of port W may be inverted with INVW = high. In this case input and output data at port W is inverted.
V_{CC}	26, 60	–	POWER SUPPLY (+5V)
GND	9, 43	–	GROUND (0V)

Figure 5
Pin Configuration Mode 4



Logic Symbol Mode 4



Pin Definitions and Functions Mode 4

Symbol	Pin	Input (I) Output (O)	Function
DV0-DV15	1-8 10-17	I/O	DATA PORT V: Bidirectional I/O lines of port V. The state of these lines (input, output or tristate) depends on the direction control input DT/$\overline{R}$IN and the $\overline{DENIN}$ input.
STB	18	I	INPUT STROBE: STB is a common strobe signal which controls the port V or port W input latch. With DT/$\overline{R}$IN = low (high) the input latch of port W (V) is selected. The latch is transparent if STB = high and the data at the input port is latched at the high-to-low transition of STB.
MB	19	I	MULTIBUS SELECT: If MOD286 = low (SAB 8288 mode), MB = low enables advanced I/O write and memory write command cycles at the $\overline{MWTC}$ and $\overline{IOWC}$ command outputs. In this case $\overline{MWTC}$ and $\overline{IOWC}$ go active 1 clock period earlier than in a bus cycle with MB = high. If MOD286 = high (SAB 82288 mode) MB determines the timing of the command and control outputs. This input is intended to be a strapping option tied to V_{CC} or GND. If MB = low, short optimized bus cycles will be performed. If MB = high, the bus controller operates in Multibus mode and generates longer bus cycles to meet the IEEE-796 (Multibus) specification.
DV16/$\overline{PERR}$	20	I/O O	DATA PORT V LINE 16: DV16 is an additional bidirectional I/O line of data port V if $\overline{PEV}$ = high. $\overline{PARITY\ ERROR}$: $\overline{PERR}$ is an open-drain parity error output in parity mode B ($\overline{PEV}$ = low). In this parity mode, $\overline{PERR}$ must be tied to V_{CC} via a pullup resistor. If a parity error occurs during a transfer from port W to port V, $\overline{PERR}$ goes low. $\overline{PERR}$ is enabled with $\overline{DENIN}$ = low and deactivated by $\overline{DENIN}$ = high.
DV17/PE/$\overline{O}$	21	I/O I	DATA PORT V LINE 17: DV17 is an additional bidirectional I/O line of data port V if $\overline{PEV}$ = high. PARITY EVEN/$\overline{ODD}$: PE/$\overline{O}$ is a select signal for even or odd parity generating and checking. This input is available only in parity mode B ($\overline{PEV}$ = low).
DW0-DW15	22-25 27-32 35-40	I/O	DATA PORT W: Bidirectional I/O lines of port W. The state of these lines (input, output or tristate) depends on the direction control input DT/$\overline{R}$IN and the $\overline{DENIN}$ input.

Pin Definitions and Functions Mode 4 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{DENIN}}$	33	I	$\overline{\text{DATA ENABLE IN}}$: $\overline{\text{DENIN}}$ = low enables the output port lines and the parity outputs. If $\overline{\text{DENIN}}$ = high the output port lines and the parity outputs are driven into the high-impedance state and the parity error output is driven inactive.
BMOD	34	I	BASE MODE: BMOD is an operating mode select input. For operating mode 4, BMOD must be tied to V_{CC}.
DW16/PW0 DW17/PW1	41 42	I/O I/O	DATA PORT W LINE 16, 17: DW16 and DW17 are additional bidirectional I/O lines of data port W if $\overline{\text{PEV}}$ = high. PARITY BIT W0, W1: In parity mode B ($\overline{\text{PEV}}$ = low) PW0 and PW1 are parity input/output lines. PW0 is related to DW0-7 and PW1 to DW8-15. During a transfer from port W, PW0 and PW1 are inputs to the parity checker. If a transfer is destinated to port W, PW0 and PW1 are outputs of the parity generator.
MOD286	44	I	BUS CONTROLLER MODE: If MOD286 is connected to GND, the bus controller part works in the SAB 8288 compatible mode. The SAB 82288 compatible bus controller mode is selected by strapping MOD286 to V_{CC}.
CLK	45	I	SYSTEM CLOCK: CLK is the system clock input to the bus controller part. The falling edge of CLK occurs when inputs are sampled and control outputs change. In the SAB 8288 compatible bus controller mode CLK is connected either to a SAB 8284B CLK output or to an SAB 80186/80188 CLKOUT output. In the SAB 82288 compatible bus controller mode CLK is tied to a SAB 82284 CLK output.

Pin Definitions and Functions Mode 4 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{S0}$ $\overline{S1}$ $\overline{S2}$/M/$\overline{IO}$	46 47 48	I	STATUS INPUTS: These pins are the status input pins of the BIC bus controller part. The command logic of the bus controller decodes these inputs to generate command and control signals at the appropriate time. The decoding of the status inputs depends on the selected bus controller mode (MOD286). In the SAB 8288 compatible bus controller mode (MOD286 = low) the following decoding of the status inputs is used:

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Processor State	Active Command Output Line
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$
0	1	1	Halt	None
1	0	0	Code Fetch	$\overline{MRDC}$
1	0	1	Read Memory Data	$\overline{MRDC}$
1	1	0	Write Memory Data	$\overline{MWTC}$
1	1	1	Passive	None

In the SAB 82288 compatible bus controller mode (MOD286 = high) the following decoding of the status inputs is used:

M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Processor State	Active Command Output Line
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$
0	1	1	Idle	None
1	0	0	Halt, Shutdown	None
1	0	1	Memory Read	$\overline{MRDC}$
1	1	0	Memory Write	$\overline{MWTC}$
1	1	1	Idle	None

$\overline{READY}$	49	I	$\overline{READY}$ INPUT: The $\overline{READY}$ input is only used in the SAB 82288 compatible bus controller mode (MOD286 = high). $\overline{READY}$ indicates the end of the current bus cycle and is an active low input.

Pin Definitions and Functions Mode 4 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CMDLY	50	I	COMMAND DELAY: CMDLY allows delaying the start of a command in the SAB 82288 bus controller mode. If CMDLY is sampled high at the end of a TS state, the command output is not activated and CMDLY is again sampled at the next falling edge of CLK. Once sampled low the proper command output becomes active. $\overline{\text{READY}}$ = low may terminate a bus cycle before CMLDY allows a command to be issued.
CENL/CEN86	51	I	COMMAND ENABLE 8288 MODE: In the SAB 8288 bus controller mode, CEN86 = high enables the command output lines. All command lines are forced into the inactive state (high) with CEN86 = low.
		I	COMMAND ENABLE 82288 MODE: In the SAB 82288 bus controller mode, CENL enables the bus controller to control the current bus cycle. CENL is latched at the end of each TS state. If CENL is sampled low, the command outputs $\overline{\text{DENOUT}}$ and DT/$\overline{\text{R}}$OUT will not go active. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus.
SUBMOD0 SUBMOD1	52 53	I	SUBMODE CONTROL: SUBMOD0 and SUBMOD1 are mode select inputs. For operating mode 4, SUBMOD0 must be tied to GND and SUBMOD1 to V_{CC}.
DT/$\overline{\text{R}}$IN	54	I	DATA TRANSMIT/$\overline{\text{RECEIVE}}$ IN: DT/$\overline{\text{R}}$IN determines the transfer direction of a data transfer. With DT/$\overline{\text{R}}$IN = low (high) a transfer is achieved from port W (V) to port V (W). DT/$\overline{\text{R}}$IN is latched with STB.
$\overline{\text{AEN}}$	55	I	$\overline{\text{ADDRESS ENABLE}}$: $\overline{\text{AEN}}$ = low enables the command outputs of the mode 4 bus controller part. $\overline{\text{AEN}}$ = high puts all command outputs into the high-impedance state and $\overline{\text{DENOUT}}$ to high level. $\overline{\text{AEN}}$ would normally be controlled by a bus arbiter (SAB 8289 or SAB 82289) which activates $\overline{\text{AEN}}$ when the arbiter owns the bus to which the bus controller is attached.
$\overline{\text{MRDC}}$	56	O	$\overline{\text{MEMORY READ COMMAND}}$: $\overline{\text{MRDC}}$ = low instructs the memory device to place data onto the data bus. The MB and CMDLY inputs control whether this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive (only if MOD286 = high).

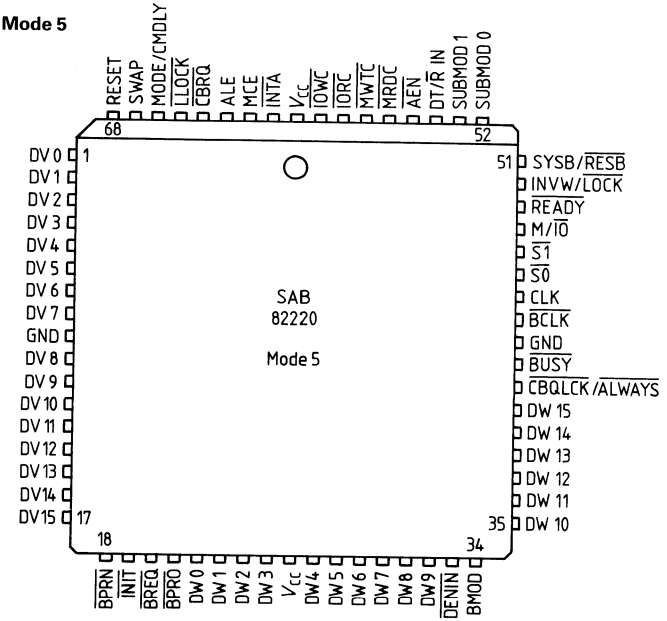
Pin Definitions and Functions Mode 4 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{MWTC}$	57	O	$\overline{MEMORY\ WRITE\ COMMAND}$: $\overline{MWTC}$ = low instructs the memory to read the data from the data bus. The MB and CMDLY inputs take over control when this output becomes active. $\overline{READY}$ controls when it becomes inactive (only if MOD286 = high).
$\overline{IORC}$	58	O	$\overline{I/O\ READ\ COMMAND}$: $\overline{IORC}$ = low instructs an I/O device to place data onto the data bus. The MB and CMDLY inputs take over control when this output becomes active. $\overline{READY}$ takes over control when it becomes inactive (only if MOD286 = high).
$\overline{IOWC}$	59	O	$\overline{I/O\ WRITE\ COMMAND}$: $\overline{IOWC}$ = low instructs an I/O device to read the data from the data bus. The MB and CMDLY inputs take over control when this output becomes active. $\overline{READY}$ controls when it becomes inactive (only if MOD286 = high).
$\overline{INTA}$	61	O	$\overline{INTERRUPT\ ACKNOWLEDGE}$: $\overline{INTA}$ = low tells an interrupting device that its interrupt request is being acknowledged. The state of the MB and CMDLY inputs determines whether this output becomes active. $\overline{READY}$ takes over control when it becomes inactive (only if MOD286 = high).
MCE	62	O	MASTER CASCADE ENABLE: MCE signals that a cascade address from a master SAB 8259A interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU address bus may then be used to send the cascade address to slave interrupt controllers. So only one of them will respond to the interrupt acknowledge cycle. MCE is only active during interrupt acknowledge cycles. A cascade address must be latched with the falling edge of ALE during MCE active (high).
ALE	63	O	ADDRESS LATCH ENABLE: ALE controls the address latches used to hold an address stable during a bus cycle. This signal is active high and latching occurs on the high-to-low transition. ALE will not be issued for the HALT bus cycle and is not affected by any of the control inputs.
DT/$\overline{ROUT}$	64	O	DATA TRANSMIT/$\overline{RECEIVE}$ OUT: The DT/$\overline{ROUT}$ output signal of the bus controller establishes the direction of data flow through the data bus transceivers. When high, this control output indicates that a write bus cycle is being performed. A low indicates a read bus cycle. This output is high when no bus cycle is active. DT/$\overline{ROUT}$ may be directly connected with DT/$\overline{RIN}$ to control the mode 4 bus transceiver part.

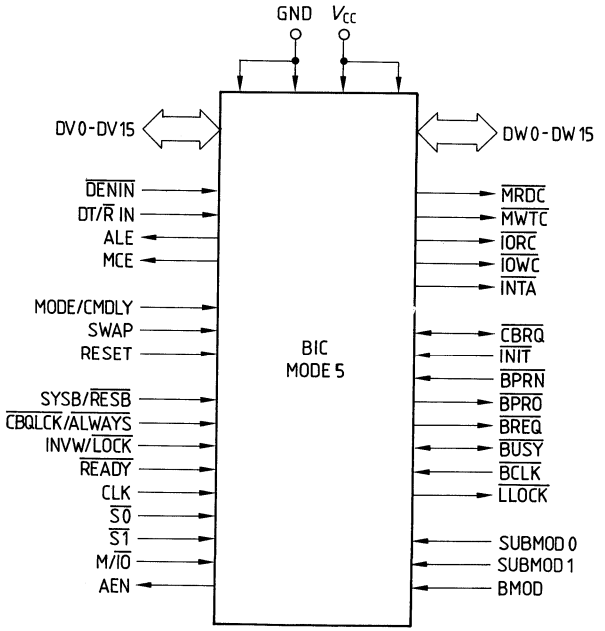
Pin Definitions and Functions Mode 4 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{DENOUT}}$	65	O	$\overline{\text{DATA ENABLE OUT}}$: This signal serves to enable data transceivers onto either the local or system data bus. $\overline{\text{DENOUT}}$ is an active low output. The timing of $\overline{\text{DENOUT}}$ is also controlled in the SAB 82288 compatible bus controller mode by the MB input.
INVW	66	I	INVERT PORT W: The polarity of port W may be inverted with INVW = high. In this case input and output data at port W, including parity lines, is inverted.
SWAP/CEN286	67	I	SWAP: If MOD286 = low, the swap feature of this input is enabled. SWAP is latched with ALE if $\overline{\text{AEN}}$ = low. If $\overline{\text{AEN}}$ = high SWAP directly affects the bus transceiver. During a data transfer, data at the input port is swapped bytewise to the output port by activating SWAP = high. In this case the input data lines 0-7 (8-15) are transferred to the output data lines 8-15 (0-7). COMMAND ENABLE 286 MODE: If MOD286 = high and MB = low, the swap feature is disabled and SWAP/CEN286 has the meaning of a command enable input. In this case the command outputs and $\overline{\text{DENOUT}}$ are immediately forced inactive (high) if CEN286 = low. If CEN286 goes high the command output and $\overline{\text{DENOUT}}$ go to the appropriate state. $\overline{\text{READY}}$ must still become active to terminate a bus cycle if CEN286 remains low.
$\overline{\text{PEV}}$	68	I	$\overline{\text{PARITY ENABLE}}$: If $\overline{\text{PEV}}$ = low, parity mode B is selected and the parity checker and parity generator are active. With $\overline{\text{PEV}}$ = high, the parity logic is disabled and the data ports have a width of 18 bits (parity mode A).
V_{CC}	26, 60	–	POWER SUPPLY (+5V)
GND	9, 43	–	GROUND (0V)

Figure 6
Pin Configuration Mode 5



Logic Symbol Mode 5



Pin Definitions and Functions Mode 5

Symbol	Pin	Input (I) Output (O)	Function
DV0–DV15	1–8, 10–17	I/O	DATA PORT V: Bidirectional I/O lines of port V. The state of these lines (input, output or tristate) depends on the direction control input DT/$\overline{R}$IN and the $\overline{DENIN}$ input or the bus controller activity. If $\overline{AEN}$ = low, the bus transceiver control is achieved by the bus controller internally.
$\overline{BPRN}$	18	I	$\overline{BUS\ PRIORITY\ IN}$: $\overline{BPRN}$ = low indicates that this arbiter has the highest priority of any arbiter requesting the system bus. $\overline{BPRN}$ = high signals the arbiter that a higher priority arbiter is requesting or has possession of the system bus.
$\overline{INIT}$	19	I	$\overline{INITIALIZE}$: This active-low Multibus signal is used to reset all arbiters on the system bus. It will cause the release of the multimaster bus, but will not clear the pending bus master request so that the arbiter can again request the multimaster bus. No arbiters have the use of the multimaster bus immediately after initialization.
$\overline{BREQ}$	20	O	$\overline{BUS\ REQUEST}$: $\overline{BREQ}$ is used in the parallel and rotating priority resolving schemes. The arbiter activates $\overline{BREQ}$ = low to request the use of the multimaster system bus. The arbiter holds $\overline{BREQ}$ active as long as it is requesting or has possession of the system bus.
$\overline{BPRO}$	21	O	$\overline{BUS\ PRIORITY\ OUT}$: $\overline{BPRO}$ is used in serial priority resolving schemes. It is connected to $\overline{BPRN}$ of the next lower priority arbiter to grant or revoke priority from that arbiter.
DW0–DW15	22–25 27–32 35–40	I/O	DATA PORT W: Bidirectional I/O lines of port W. The state of these lines (input, output or tristate) depends either on the direction control input DT/$\overline{R}$IN and the $\overline{DENIN}$ input or the bus controller activity. If $\overline{AEN}$ = low, the bus transceiver control is achieved by the bus controller internally.
$\overline{DENIN}$	33	I	$\overline{DATA\ ENABLE\ IN}$: If the bus arbiter has no access right to the system bus ($\overline{AEN}$ = high), the output port lines are enabled with $\overline{DENIN}$ = low and driven into the high-impedance state by $\overline{DENIN}$ = high. In case of Multibus access ($\overline{AEN}$ = low) the outputs of the bus transceiver are controlled internally by the bus controller.
BMOD	34	I	BASE MODE: BMOD is an operating mode select input. For operating mode 5, BMOD must be tied to V_{CC}.

Pin Definitions and Functions Mode 5 (cont.)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{CBQLCK/ALWAYS}}$	41	I	$\overline{\text{COMMON BUS REQUEST LOCK/ALWAYS RELEASE}}$: At processor reset this input is programmed to be either the $\overline{\text{ALWAYS RELEASE}}$ strapping option or the $\overline{\text{COMMON BUS REQUEST LOCK}}$ input. When this pin is low during the falling edge of RESET ($\overline{\text{ALWAYS}}$ option) the arbiter is programmed to surrender the multimaster system bus after each bus transfer cycle. This function is established until the next reset operation. When this pin is high during the falling edge of RESET the arbiter is programmed to support the $\overline{\text{COMMON BUS REQUEST LOCK}}$ function. $\overline{\text{CBQLCK}}$ is an active low input that prevents the arbiter from surrendering the multimaster system bus to a common bus request through the $\overline{\text{CBRQ}}$ input pin.
$\overline{\text{BUSY}}$	42	I/O	$\overline{\text{BUSY}}$: $\overline{\text{BUSY}}$ is a Multibus signal which is asserted when the system bus is in use. As an input $\overline{\text{BUSY}}$ = low indicates when the Multibus is in use. As an output $\overline{\text{BUSY}}$ is asserted to signal when this arbiter has taken control of the Multibus. $\overline{\text{BUSY}}$ is an open-drain input/output which requires an external pullup resistor.
$\overline{\text{BCLK}}$	44	I	$\overline{\text{BUS CLOCK}}$: $\overline{\text{BCLK}}$ is the multimaster system bus clock to which the multimaster bus interface signals are synchronized. $\overline{\text{BCLK}}$ can be asynchronous to CLK.
CLK	45	I	SYSTEM CLOCK: CLK is the clock signal from the SAB 82284 clock generator as the timing reference for bus controller, bus arbiter and processor interface signals. Sampling of all inputs is done with the falling edge of CLK. Its frequency is twice the internal processor frequency of the SAB 80286.
$\overline{\text{S0}}$ $\overline{\text{S1}}$ M/$\overline{\text{IO}}$	46 47 48	I	STATUS INPUTS: $\overline{\text{S0}}$, $\overline{\text{S1}}$ and M/$\overline{\text{IO}}$ are the status input signal pins from the SAB 80286 processor. A bus cycle is started when either $\overline{\text{S1}}$ or $\overline{\text{S0}}$ is sampled low at the falling edge of CLK. These inputs have pullup resistors to generate an input high level if the status lines from the CPU are floating. The M/$\overline{\text{IO}}$ pin is also used for ADMA mode initialization.

Pin Definitions and Functions Mode 5 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
			The following decoding of the status inputs is used:

M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Processor State	Active Command Output Line
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$
0	1	1	Idle	None
1	0	0	Halt, Shutdown	None
1	0	1	Memory Read	$\overline{MRDC}$
1	1	0	Memory Write	$\overline{MWTC}$
1	1	1	Idle	None

$\overline{READY}$	49	I	$\overline{READY}$ INPUT: $\overline{READY}$ is an active low signal which indicates the end of the bus cycle. The SAB 80286 halt or shutdown cycles do not require $\overline{READY}$ to terminate the bus cycle.
INVW/$\overline{LOCK}$	50	I	INVERT PORT W/$\overline{LOCK}$: The invert option of the port W data inputs/outputs is enabled if INVW/$\overline{LOCK}$ = high during RESET active (high). Normal polarity of the W port is selected if INVW/$\overline{LOCK}$ = low during RESET. After RESET, INVW/$\overline{LOCK}$ operates as a $\overline{LOCK}$ input, which serves to prevent the arbiter from surrendering the system bus to any other bus arbiter, regardless of its priority. $\overline{LOCK}$ is sampled at the end of the TS state.
SYSB/$\overline{RESB}$	51	I	SYSTEM BUS/$\overline{RESIDENT\ BUS}$: This signal determines whether the multimaster system bus is required for the current bus cycle or the resident bus. The signal can be generated from an address decoder attached to the processors address pins. The arbiter will request or retain control of the multimaster system bus when the SYSB/$\overline{RESB}$ pin is sampled high at the end of the TS bus state (not in the ADMA mode). During an interrupt acknowledge cycle, this input is sampled on every falling edge of CLK, starting at the end of the TS state, until either SYSB/$\overline{RESB}$ is sampled high or the bus cycle is terminated by the $\overline{READY}$ signal.
SUBMOD0 SUBMOD1	52 53	I	SUBMODE CONTROL: SUBMOD0 and SUBMOD1 are mode select inputs. In operating mode 5, both must be tied to V_{CC}.

Pin Definitions and Functions Mode 5 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
DT/$\overline{R}$IN	54	I	DATA TRANSMIT/$\overline{\text{RECEIVE}}$ IN: If the bus arbiter has no access right to the system bus ($\overline{\text{AEN}}$ = high), the transfer direction of data transfer via the bus transceiver is determined by DT/$\overline{R}$IN. With DT/$\overline{R}$IN = low (high) a transfer is achieved from port W (V) to port V (W). In case of Multibus access ($\overline{\text{AEN}}$ = low), the transfer direction of the bus transceiver is controlled internally by the bus controller.
$\overline{\text{AEN}}$	55	O	$\overline{\text{ADDRESS ENABLE}}$: $\overline{\text{AEN}}$ is an output of the bus arbiter which serves as an output enable control to the address latches and the command outputs of the bus controller. The ready logic of an SAB 82284 is also controlled by $\overline{\text{AEN}}$. $\overline{\text{AEN}}$ goes active relative to $\overline{\text{BCLK}}$ and inactive relative to CLK.
$\overline{\text{MRDC}}$	56	O	$\overline{\text{MEMORY READ COMMAND}}$: $\overline{\text{MRDC}}$ = low instructs the memory device to place data onto the data bus. The CMDLY input takes over control when this output becomes active. $\overline{\text{READY}}$ takes over control when it becomes inactive.
$\overline{\text{MWTC}}$	57	O	$\overline{\text{MEMORY WRITE COMMAND}}$: $\overline{\text{MWTC}}$ = low instructs the memory to read the data from the data bus. The CMDLY input takes over control when this output becomes active. $\overline{\text{READY}}$ takes over control when it becomes inactive.
$\overline{\text{IORC}}$	58	O	$\overline{\text{I/O READ COMMAND}}$: $\overline{\text{IORC}}$ = low instructs an I/O device to place data onto the data bus. The CMDLY input takes over control when this output becomes active. $\overline{\text{READY}}$ takes over control when it becomes inactive.
$\overline{\text{IOWC}}$	59	O	$\overline{\text{I/O WRITE COMMAND}}$: $\overline{\text{IOWC}}$ = low instructs an I/O device to read the data from the data bus. The CMDLY input takes over control when this output becomes active. $\overline{\text{READY}}$ takes over control when it becomes inactive.
$\overline{\text{INTA}}$	61	O	$\overline{\text{INTERRUPT ACKNOWLEDGE}}$: $\overline{\text{INTA}}$ = low tells an interrupting device that its interrupt request is being acknowledged. The CMDLY input takes over control when this output becomes active. $\overline{\text{READY}}$ takes over control when it becomes inactive.

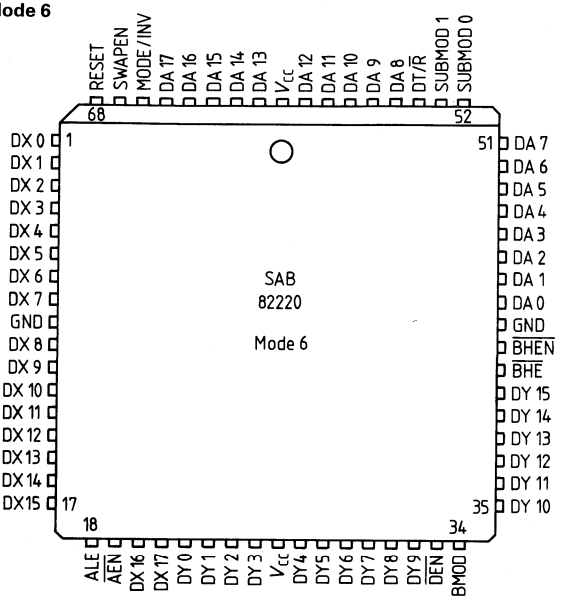
Pin Definitions and Functions Mode 5 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
MCE	62	O	MASTER CASCADE ENABLE: MCE = high signals that a cascade address from an SAB 8259A master interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The address bus of the CPU is then used to send the cascade address to slave interrupt controllers. Only one of them will respond to the interrupt acknowledge cycle. MCE is only active during interrupt acknowledge cycles. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.
ALE	63	O	ADDRESS LATCH ENABLE: ALE controls the address latches used to hold an address stable during a bus cycle. This signal is active high and latching occurs on the high-to-low transition. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.
$\overline{\text{CBRQ}}$	64	I/O	$\overline{\text{COMMON BUS REQUEST}}$: $\overline{\text{CBRQ}}$ is a Multibus signal that indicates when an arbiter is requesting the Multibus. The input function of this pin is enabled by the $\overline{\text{CBQLCK}}$ signal. As an input $\overline{\text{CBRQ}}$ = low indicates that another arbiter is requesting the multimaster system bus. As an output $\overline{\text{CBRQ}}$ is asserted to indicate that this arbiter is requesting the Multibus. The arbiter pulls $\overline{\text{CBRQ}}$ low when it issues $\overline{\text{BREQ}}$. The arbiter releases $\overline{\text{CBRQ}}$ when it obtains the Multibus. $\overline{\text{CBRQ}}$ is an open-drain input/output requiring an external pullup resistor.
$\overline{\text{LLOCK}}$	65	O	$\overline{\text{LEVEL LOCK}}$: $\overline{\text{LLOCK}}$ is an active-low output signal decoded from the processor $\overline{\text{LOCK}}$ signal. $\overline{\text{LLOCK}}$ can be used as Multibus $\overline{\text{LOCK}}$ when buffered with a tristate buffer, which is enabled by the $\overline{\text{AEN}}$ signal. $\overline{\text{LLOCK}}$ will be cleared by RESET but not by $\overline{\text{INIT}}$. In the "ADMA mode" of operating mode 5 of the BIC, this pin is used to generate the HLDA for the SAB 82258 advanced DMA controller.

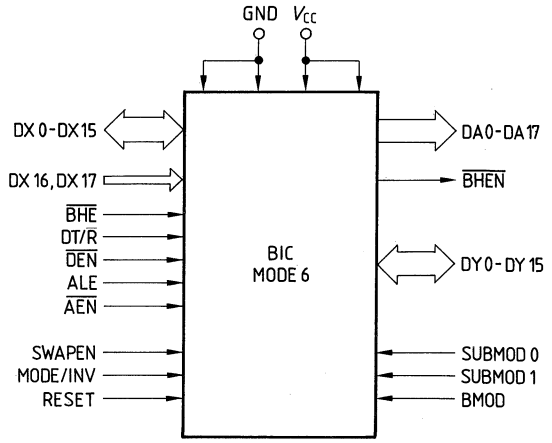
Pin Definitions and Functions Mode 5 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
MODE/CMDLY	66	I	MODE/COMMAND DELAY: During RESET active (high) this pin must be at low level to select the operating mode 5. After an active RESET, MODE/CMDLY is used to delay the start of a command. If sampled high, the command output is not activated and MODE/CMLDY is again sampled at the next CLK cycle. When sampled low the selected command output is enabled. If $\overline{\text{READY}}$ is detected low before the command output is activated, the BIC will terminate the bus cycle, even if no command was issued.
SWAP	67	I	SWAP: During a data transfer data at the input port is swapped bytewise to the output port by activating SWAP = high. In this case the input data lines 0-7 (8-15) are transferred to the output data lines 8-15 (0-7). SWAP is latched with ALE, which is generated by the bus controller.
RESET	68	I	RESET: The active high RESET signal is used for operating mode selection via MODE/CMDLY. It also resets the bus arbiter logic, clears any pending requests and releases the multimaster system bus.
V_{CC}	26, 60	–	POWER SUPPLY (+5V)
GND	9, 43	–	GROUND (0V)

Figure 7
Pin Configuration Mode 6



Logic Symbol Mode 6



Pin Definitions and Functions Mode 6

Symbol	Pin	Input (I) Output (O)	Function
DX0-DX15	1-8 10-17	I/O	DATA PORT X: Bidirectional I/O lines of port X. These lines are dedicated to be used as a 16-bit time multiplexed address and data bus. The state of these lines (input, output or tristate) depends on the direction control input DT/$\overline{R}$ and the $\overline{DEN}$ input.
DX16, DX17	20, 21	I	DATA PORT X LINE 16, 17: DX16 and DX17 are inputs of port X which are, additionally to DX0-15, wired to the address latch of port A.
ALE	18	I	ADDRESS LATCH ENABLE: ALE controls the port A latch. The address latch is transparent if ALE = high and the data at the input port is latched at the high-to-low transition of ALE.
$\overline{AEN}$	19	I	$\overline{ADDRESS\ ENABLE}$: $\overline{AEN}$ = low enables the port A outputs and the $\overline{BHEN}$ output. These outputs are tristated if $\overline{AEN}$ = high.
DY0-DY15	22-25 27-32 35-40	I/O	DATA PORT Y: Bidirectional I/O lines of port Y. These lines are dedicated to be used as a buffered 16-bit data bus. The state of these lines (input, output or tristate) depends on the direction control input DT/$\overline{R}$ and the $\overline{DEN}$ input.
$\overline{DEN}$	33	I	$\overline{DATA\ ENABLE}$: $\overline{DEN}$ = low enables the output port lines of either port X or port Y. With $\overline{DEN}$ = high the output port lines are tristated.
BMOD	34	I	BASE MODE: BMOD is an operating mode select input. For operating mode 6, BMOD must be tied to V_{CC}.
$\overline{BHE}$	41	I	$\overline{BUS\ HIGH\ ENABLE\ IN}$: $\overline{BHE}$ is used to enable a data transfer on the upper half of data bus X and Y. $\overline{BHE}$ = low indicates a data transfer on DX8-15 and DY8-15. $\overline{BHE}$ is latched with ALE and sent to the $\overline{BHEN}$ output (not in automatic swap mode).
$\overline{BHEN}$	42	O	$\overline{BUS\ HIGH\ ENABLE\ OUT}$: In the manual swap mode $\overline{BHEN}$ is the latched output of the $\overline{BHE}$ input signal. $\overline{AEN}$ = low enables the $\overline{BHEN}$ output. $\overline{BHEN}$ is not affected by the invert option of port A and port Y. In the automatic swap mode $\overline{BHEN}$ is a modified $\overline{BHE}$ signal (see functional description).

Pin Definitions and Functions Mode 6 (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
DA0-DA17	44-51 55-59 61-65	O	ADDRESS PORT A: The address port A is the output port of the 18-bit address latch. The information at port X is latched with ALE and sent to DA0-17. Port A is enabled by $\overline{AEN}$ = low.
SUBMOD0 SUBMOD1	52 53	I	SUBMODE CONTROL: SUBMOD0 and SUBMOD1 are mode control inputs. For operating mode 6 both inputs must be tied to V_{CC}.
DT/$\overline{R}$	54	I	DATA TRANSMIT/$\overline{RECEIVE}$: DT/$\overline{R}$ determines the transfer direction of a data transfer. With DT/$\overline{R}$ = low (high) a transfer is achieved from port Y (X) to port X (Y). DT/$\overline{R}$ is latched with ALE.
MODE/INV	66	I I	MODE SELECT: MODE/INV is a mode select signal which serves to distinguish between operating mode 5 and 6. During RESET active (high) MODE/INV must be at high level. INVERT: After an active RESET signal (if RESET = low) MODE/INV controls the polarity of port A and port Y. Normal polarity is selected with MODE/INV = low and inverted polarity with MODE/INV = high.
SWAPEN	67	I	SWAP ENABLE: Two swap modes are available; automatic and manual swapping. If SWAPEN = low during RESET active (high), the manual swap mode is selected. In this mode SWAPEN is latched with ALE. If SWAPEN = high the input lines 0-7 (8-15) of port X or Y are transferred to the output data lines 8-15 (0-7) of port Y or X. In the automatic swap mode (SWAPEN = high during RESET active) the BIC performs an automatic swap between the lower and the higher part of the data bus port X and Y if a byte transfer occurs from or to an odd address on port X (DX0 = 1 and $\overline{BHE}$ = 0).
RESET	68	I	RESET: The active high RESET signal is used for operating mode selection (with MODE/INV) and for swap mode control (with SWAPEN).
V_{CC}	26, 60	–	POWER SUPPLY (+5V)
GND	9, 43	–	GROUND (0V)

General Description

Advanced microcomputer systems for high-performance applications require usually multiprocessing. Therefore they have more than one bus to execute several tasks in parallel in a most efficient way. Due to this demand, the chip count of the interface logic of a system, necessary for bus interconnections, increases. Different standard devices are used to design bus interfaces. If the bus width exceeds 8 bits, several of these devices are cascaded. It's a major goal for a bus interface design to reduce the chip count, the power consumption and the interconnections on the board.

A universal multifunctional bus interface device that combines all functional parts of a bus interface logic onto one chip having a high current drive capability at a high capacitive bus load would be the optimal solution.

The SAB 82220 BIC (Bus Interface Controller) is such a component which fits in many different bus interface applications by combining all typical bus interface functions at a multifunctional device. The SAB 82220 contains the following functional parts:

Bidirectional buffers with a high current driving capability for data bus lines (inverting and non-inverting) and an enable/disable output function.

Latches with high current driving capability for data bus lines (inverting and non-inverting) and an enable/disable output function.

Bus controller to generate bus control signals.

Bus arbiter to provide arbitration support for multiprocessor system configurations.

Parity logic to generate and check bytewise even or odd parity bits which are added to a data or address bus.

Swap logic to swap lower and higher 8-bit quantities of a data bus (e.g. transfers via Multibus I from/to 16-bit boards).

Chip select decoder to generate select signals from address information at the address bus (e.g. chip select for I/O devices, memory bank select, system/resident bus select).

The SAB 82220 is designed to be applied in most standard microcomputer systems. Two operating modes fit especially into SAB 8086/8088, SAB 80186/80188 or SAB 80286 microcomputer applications. The BIC can be used in a resident bus interface as well as in a multimaster system bus interface. Depending on the operating mode one BIC may replace several of the following standard SAB 828X or SAB 8228X devices:

SAB 8282A/8283A	8-bit address latch
SAB 8286A/8287A	8-bit bus transceiver
SAB 8288A/82288	Bus controller
SAB 82289	Bus arbiter

Beside these SAB 828X and SAB 8228X parts the BIC also substitutes standard TTL components. Especially the on-chip swap logic and the parity generator/checker will replace a lot of random logic.

Operating Modes

The SAB 82220 offers 6 different operating modes. These operating modes are not changed in a specific application. So the BIC operates always in one of these 6 operating modes. Each mode is initiated by connecting special pins to V_{CC} or GND. For operating mode 5 and 6 additionally the RESET input is sampled during mode selection.

Operating mode 1: Tridirectional transceiver with 18-bit bus width. In this mode three 18-bit buses may be interconnected. A data transfer is possible in every transfer direction between all buses. A byte swap feature and parity check and generation are available. One port optionally supports inverted signal polarity.

Operating mode 2: Bidirectional transceiver with 27-bit bus width. In this mode two 27-bit buses may be interconnected. Mode 2 is suitable for address latch applications. Byte swap and parity check/generate features are available. One port optionally supports inverted signal polarity.

Operating mode 3: Bidirectional transceiver with 24-bit bus width and chip select decoder. This mode is suitable for address latch applications. It provides in addition to mode 2 a chip select decoder with decoding options of several address ranges. One port optionally supports inverted signal polarity.

Operating mode 4: Bidirectional transceiver with 18-bit bus width and bus controller. In this mode the BIC contains a bus controller part, which is able to generate SAB 8288A or SAB 82288 compatible bus control signals. The transceiver part can be used as a data bus transceiver. Byte swap and parity check/generate features are available. One port optionally supports inverted signal polarity.

Operating mode 5: Bidirectional transceiver with 16-bit bus width and bus controller and bus arbiter. This mode fits into SAB 80286/82258 (ADMA) systems with a Multibus I or multiprocessor bus interface. It provides an SAB 82288 compatible bus controller and an SAB 82289 compatible bus arbiter. The transceiver part is used as a data bus transceiver. One port optionally supports inverted signal polarity.

Operating mode 6: Multiplex bus transceiver with address latch (16/18-bit bus width). This mode supports applications where a processor with multiplexed address/data bus has to interface a demultiplexed address/data bus configuration. A byte swap feature is available at the data bus. The address bus and the buffered data bus optionally support inverted signal polarity.

Programming

The programming of the 6 operating modes of the SAB 82220 is done via pin strapping (figure 8).

Up to four pins at maximum are used to select the modes: BMOD, SUBMOD0, SUBMOD1 and MODE/CMDLY respectively MODE/INV (pin 66).

Figure 8
Operating Mode Programming

Operating Mode	BMOD (pin 34)	SUBMOD0 (pin 52)	SUBMOD1 (pin 53)	Signal during RESET high (pin 66)
Mode 1	GND	–	–	–
Mode 2	V_{CC}	GND	GND	–
Mode 3	V_{CC}	V_{CC}	GND	–
Mode 4	V_{CC}	GND	V_{CC}	–
Mode 5	V_{CC}	V_{CC}	V_{CC}	MODE/CMDLY = 0
Mode 6	V_{CC}	V_{CC}	V_{CC}	MODE/INV = 1

The base mode pin BMOD and the two submode pins SUBMOD0 and SUBMOD1 are wired directly to either V_{CC} or GND. In case of mode 5 and mode 6 an additional signal is used to select the operating mode.

This input line (pin 66: MODE/CMDLY or MODE/INV) must be tied to the corresponding level during the active reset phase (RESET = high). It is latched with the falling edge of RESET. After that, pin 66 is used for other functions.

Functional Description

Operating Mode 1

Transceiver Operation

In operating mode 1 the BIC offers three 18-bit latches/buffers with its bidirectional input/output lines DX0-17, DY0-17 and DZ0-17. Data at an input port may be stored in a latch. STBX is the strobe signal which controls the port X latch. The port Z and Y latches are controlled with the common strobe signal STBYZ. If STBYZ is activated it depends on the transfer direction which latch is used. The latches are transparent if the strobe signal is high. The data at the inputs of the ports is latched at the high-to-low transition of STBX or STBYZ. If the latches are not used the strobe input must be set to high level.

Three control signals DIR0, DIR1 and DIR2 select the direction of the data transfer between input and output port. The 3 direction lines are latched at the falling edge of STBX or STBYZ. Figure 9 shows the possible buffer transfer directions depending on the buffer direction control signals.

Figure 9
Mode 1 Direction Control

Transfer Direction	DIR2	DIR1	DIR0	Port Configuration Port X	Port Y	Port Z
Z → Y	0	0	0	Tristate	Output	Input
Y → Z	0	0	1	Tristate	Input	Output
X → Y	0	1	0	Input	Output	Tristate
Y → X	0	1	1	Output	Input	Tristate
Z → X	1	0	0	Output	Tristate	Input
X → Z	1	0	1	Input	Tristate	Output
Y → X	1	1	0	Output	Input	Tristate
X → Y	1	1	1	Input	Output	Tristate

The data outputs and the parity outputs of a port may be enabled or disabled with $\overline{DEN}$. If $\overline{DEN}$ = high, data and parity outputs are driven into the high-impedance state and parity error outputs are driven inactive. The polarity of port Y may be inverted by INVY. Data from or to port Y is inverted if INVY = high. This also inverts the parity inputs/outputs.

During a data transfer the input data can be swapped bytewise to the output port. If swapping is enabled (SWAP = high), the input data lines 0-7 (8-15) are transferred to the output data lines 8-15 (0-7). SWAP is internally latched with STBX or STBYZ. The swap feature is available for every transfer direction. If parity modes B-D are enabled, the activating of SWAP also affects swapping of the parity inputs/outputs.

Parity Modes

In operating mode 1 the SAB 82220 supports 4 different parity modes (figure 10) with even parity generating and checking. They are enabled via pin strapping. An even parity bit is set if the data which must be protected has an odd number of 1's. In parity mode B-D the port width of the bidirectional transceiver is reduced from 18 to 16 bits. The two remaining port lines are used as inputs and outputs to the parity generators and checkers. The two parity generators produce two bytewise parity bits to the corresponding data on the port lines 0-7 and 8-15. The two parity checkers test the parity inputs for a parity error and generate a parity error output signal. During a byte transfer with parity logic enabled, the not concerned port part must have a well defined content and a proper parity bit. Otherwise undesired parity error conditions may occur.

Parity mode A

In parity mode A the parity logic is disabled. In this mode the ports have the full width of 18 bits. Parity mode A is enabled by strapping $\overline{PEX}$ to V_{CC}.

Parity mode B

Parity mode B is enabled by strapping $\overline{PEX}$ to GND and PX1 to V_{CC}. In this mode parity generators and checkers are available on port Y and Z. PY0 and PZ0 (PY1 and PZ1) are the corresponding parity input/output lines to DY0-7 and DZ0-7 (DY8-15 and DZ8-15). The parity generators are active during a transfer from port X to either port Y or port Z. The parity checkers are in use if a transfer is performed from port Y or port Z to port X. If a parity error occurs on the low and/or high portion of a transfer to port X, the parity error signal $\overline{PERR}$ will go low. $\overline{PERR}$ is an open-drain output and needs an external pullup resistor to V_{CC}.

Parity mode C

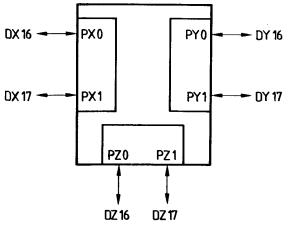
Parity mode C is enabled by strapping $\overline{PEX}$, PX0 and PX1 to GND. In this mode parity generators and checkers are available on port Y. If a transfer is executed to port Y, PY0 and PY1 are the corresponding outputs of the parity generators. PY0 (PY1) is related to DY0-7 (DY8-15). The parity checkers are active during a transfer from port Y to one of the other 2 ports. If a parity error occurs during a transfer from port Y to port X port $\overline{PERRX}$ ($\overline{PERRZ}$) will go low. $\overline{PERRX}$ and $\overline{PERRZ}$ are open-collector outputs and need an external pullup resistor to V_{CC}.

Parity mode D

Parity mode D is enabled by strapping $\overline{PEX}$ and PX1 to GND. PX0 must be tied to V_{CC}. In this mode parity generators and checkers are available on port Z. Every transfer to port Z is supported by the generation of two parity bits PZ0 (related to DZ0-7) and PZ1 (related to DZ8-DZ15). The parity checkers are active during a transfer from port Z to one of the other 2 ports. If a parity error occurs during a transfer from port X (port Y) to port Z, $\overline{PERRX}$ ($\overline{PERRY}$) will go low, $\overline{PERRX}$ and $\overline{PERRY}$ are open-collector outputs and need an external pullup resistor to V_{CC}.

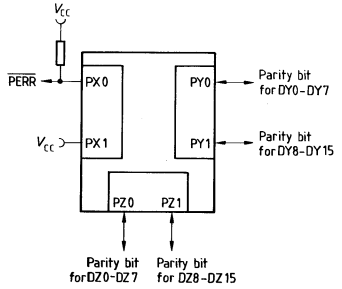
Figure 10
Parity Modes in Operating Mode 1

Parity Mode A: $\overline{PEX} = V_{CC}$



Parity generating/checking disabled
18-bit port width

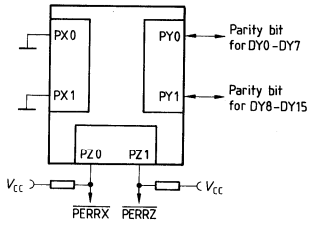
Parity Mode B: $\overline{PEX}$ = GND
PX1 = V_{CC}



Parity generating if transfer from
X → Y, X → Z

Parity checking if transfer from
Y → X, Z → X

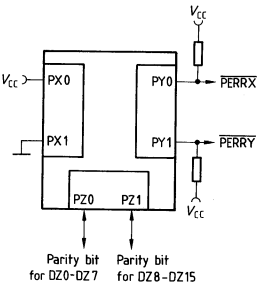
Parity Mode C: $\overline{PEX}$ = GND
PX0 = GND
PX1 = GND



Parity generating if transfer from
X → Y, Z → Y

Parity checking if transfer from
Y → X, Y → Z

Parity Mode D: $\overline{PEX}$ = GND
PX0 = V_{CC}
PX1 = GND



Parity generating if transfer from
X → Z, Y → Z

Parity checking if transfer from
Z → X, Z → Y

Operating Mode 2

Transceiver Operation

In operating mode 2 the BIC offers a 27-bit latch/buffer with the bidirectional input/output lines DV0-26 and DW0-26. The input port latches are controlled by strobe signals. STBV controls the latch of port V and STBW the latch of port W. The latches are transparent if the strobe signal is high. The data at the inputs of a port is latched at the high-to-low transition of STBV or STBW. If the latches are not used the strobe inputs must be set to high level.

The signal DT/$\overline{R}$ determines the buffer transfer direction. DT/$\overline{R}$ is latched at the falling edge of STBV or STBW. With DT/$\overline{R}$ = low (high), the transfer is performed from port W to port V (from port V to port W). The data outputs and the parity outputs of a port may be enabled or disabled with $\overline{DEN}$. If $\overline{DEN}$ = high, data and parity outputs are driven into the high impedance state and the parity error output is driven inactive. The polarity of the data at port W is inverted by INVW = high. This also inverts the parity inputs/outputs.

During a data transfer the input data can be swapped bytewise to the output port. If swapping is enabled (SWAP = high), the input data lines 0-7 (8-15) are transferred to the output data lines 8-15 (0-7). SWAP is internally latched with STBV or STBW. If parity generators/checkers are enabled the corresponding parity bits are also swapped.

Parity Modes

In operating mode 2 the SAB 82220 supports 2 parity modes (figure 11) with even or odd parity generating and checking. The selection of these modes is performed with pin strapping. An even (odd) parity bit is set if the data which must be protected has an odd (even) number of 1s. If parity lines are enabled the bus width of port V and W is reduced to 24 bit. The three parity generators/checkers produce and check 3 parity bits, one each for the lower, medium and higher byte of the 24-bit port. In case of a 8-bit or 16-bit data transfer with parity logic enabled the not concerned part of the ports must have well defined contents and a proper parity bit too. Otherwise, invalid parity error conditions may occur.

Parity mode A

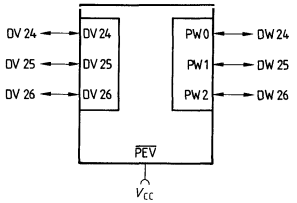
In parity mode A the parity logic is disabled. In this mode the ports have the full width of 27 bits. Parity mode A is selected by strapping $\overline{PEV}$ to V_{CC}.

Parity mode B

Parity mode B is enabled by connecting $\overline{PEV}$ to GND. In this mode 3 parity generators and checkers are available at port W. PW0, PW1 and PW2 are the corresponding parity input/output lines to DW0-7, DW8-15 and DW16-23. The parity generators are active during a transfer from port V to port W. The parity checkers are in use if a transfer is performed from port W to port V. If a parity error occurs at least at one of the parity inputs, the parity error signal $\overline{PERR}$ will go low. $\overline{PERR}$ is an open-drain output and needs an external pullup resistor to V_{CC}. If PE/$\overline{O}$ = low (high), odd (even) parity mode is selected.

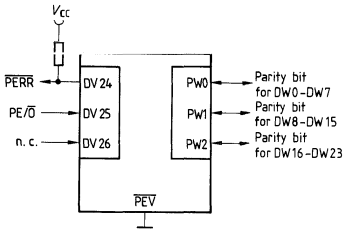
Figure 11
Parity Modes in Operating Mode 2

Parity Mode A: $\overline{PEV} = V_{CC}$



Parity generating/checking disabled
27-bit bus width

Parity Mode B: $\overline{PEV}$ = GND



Parity generating if transfer from V → W

Parity checking if transfer from W → V

Operating Mode 3

Transceiver Operation

In operating mode 3 the BIC provides a 24-bit latch/buffer with bidirectional input/output lines DV0-23 and DW0-23. If a port is used as an input port the strobe signal STB controls the input latch. The input latch is transparent if STB = high. The data at the inputs of a port is latched at the high-to-low transition of STB. If the latches are not used STB must be tied high.

The signal DT/$\overline{R}$ determines the buffer transfer direction. DT/$\overline{R}$ is latched at the falling edge of STB. With DT/$\overline{R}$ = low (high), the transfer is performed from port W to port V (from port V to port W). The data outputs of a port may be enabled or disabled with $\overline{DEN}$. $\overline{DEN}$ also affects the $\overline{CCS}$ and $\overline{CS0\text{-}3}$ chip select output lines. If $\overline{DEN}$ = high, the port output lines and the chip select lines are driven into the high-impedance state. The polarity of the data at port W is inverted by INVW = high.

Chip Select Decoder

Depending on the information at the port lines 8 to 23 (e.g. the address bus of a microprocessor) the chip select logic of the SAB 82220 operating mode 3 provides 4 select outputs $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ with programmable address ranges and one common select output $\overline{CCS}$. If the data or address at the input port, which is specified by DT/$\overline{R}$, is inside a specific range, the corresponding $\overline{CSi}$ and $\overline{CCS}$ will go active (low).

Figure 12
Select Output Control of Operating Mode 3

$\overline{DEN}$	$\overline{ENCS}$	Address inside Base Address Range	$\overline{CSi}$ $\overline{CCS}$	Output Port
0	0	Yes	0	Active
0	0	No	1	Active
0	1	X	1	Active
1	X	X	Tristate	Tristate

The activation of the select outputs is also controlled by $\overline{ENCS}$. $\overline{ENCS}$ = high forces the select outputs $\overline{CS0\text{-}3}$ and $\overline{CCS}$ into the inactive state (high). All 5 select outputs are tristated by $\overline{DEN}$ = high.

The signals CSMOD2-0 are used to select the address ranges (submodes) of the chip select decoder. Figure 13 shows in detail the address ranges depending on the submode which is programmed via CSMOD2-0. INVW also affects the chip select logic.

Figure 13
Chip Select Address Range Table

Submode CSMOD2, 1, 0	Select Line	INVW = 0 Address Range	INVW = 1 Address Range
(0, 0, 0)	$\overline{CS0}$	000000–0000FF	FFFF00–FFFFFF
	$\overline{CS1}$	000100–0001FF	FFFE00–FFFEFF
	$\overline{CS2}$	000200–0002FF	FFFD00–FFFDFF
	$\overline{CS3}$	000300–0003FF	FFFC00–FFFCFF
(0, 0, 1)	$\overline{CS0}$	040000–05FFFF	FA0000–FBFFFF
	$\overline{CS1}$	020000–03FFFF	FC0000–FDFFFF
	$\overline{CS2}$	000000–01FFFF	FE0000–FFFFFF
	$\overline{CS3}$	FE0000–FFFFFF	000000–01FFFF
(0, 1, 0)	$\overline{CS0}$	000000–003FFF	FFC000–FFFFFF
	$\overline{CS1}$	004000–007FFF	FF8000–FFBFFF
	$\overline{CS2}$	008000–00BFFF	FF4000–FF7FFF
	$\overline{CS3}$	00C000–00FFFF	FF0000–FF3FFF
(0, 1, 1)	$\overline{CS0}$	100000–17FFFF	E80000–EFFFFF
	$\overline{CS1}$	080000–0FFFFF	F00000–F7FFFF
	$\overline{CS2}$	000000–07FFFF	F80000–FFFFFF
	$\overline{CS3}$	F80000–FFFFFF	000000–07FFFF
(1, 0, 0)	$\overline{CS0}$	000200–0002FF	FFFD00–FFFDFF
	$\overline{CS1}$	000300–0003FF	FFFC00–FFFCFF
	$\overline{CS2}$	Not Active	Not Active
	$\overline{CS3}$	Not Active	Not Active
(1, 0, 1)	$\overline{CS0}$	Not Active	Not Active
	$\overline{CS1}$	Not Active	Not Active
	$\overline{CS2}$	000000–01FFFF	FE0000–FFFFFF
	$\overline{CS3}$	FE0000–FFFFFF	000000–01FFFF
(1, 1, 0)	$\overline{CS0}$	000000–0000FF	FFFF00–FFFFFF
	$\overline{CS1}$	000100–0001FF	FFFE00–FFFEFF
	$\overline{CS2}$	Not Active	Not Active
	$\overline{CS3}$	Not Active	Not Active
(1, 1, 1)	$\overline{CS0}$	Not Active	Not Active
	$\overline{CS1}$	Not Active	Not Active
	$\overline{CS2}$	000000–07FFFF	F80000–FFFFFF
	$\overline{CS3}$	F80000–FFFFFF	000000–07FFFF

With CSMOD2-0 = (0,0,0) the select outputs decode four contiguous address ranges of 256 bytes each. This submode is provided for I/O device selection.
With CSMOD2-0 = (0,0,1) the select outputs decode four contiguous address ranges of 128 Kbytes each. Memory bank selection may be supported in this submode.
With CSMOD2-0 = (0,1,0) the select outputs decode four contiguous address ranges of 16 Kbytes each. This submode supports the selection of smaller RAM/ROM devices.

With CSMOD2-0 = (0,1,1) the select outputs decode four contiguous address ranges with 512 Kbytes each. Memory bank selection may be supported with this submode.
If CSMOD2 = 1 [submodes CSMOD2-0 = (1,0,0), (1,0,1), (1,1,0), (1,1,1)] at a submode, either $\overline{CS0}$ and $\overline{CS1}$ or $\overline{CS2}$ and $\overline{CS3}$ are active. These four submodes may be used to generate 2 memory and 2 I/O chip select lines. If, for example, the M/$\overline{IO}$ line of a processor is connected to CSMOD0, $\overline{CS0}$ and $\overline{CS1}$ can be used as I/O chip select lines with a range of 256 bytes, and in this case $\overline{CS2}$ and $\overline{CS3}$ have an address range of 128 Kbytes (CSMOD1 = 0) or 512 Kbytes (CSMOD1 = 1) each.

Operating Mode 4

Transceiver Operation

In operating mode 4 the BIC offers a 18-bit latch/buffer with its bidirectional input/output lines DV0-17 and DW0-17. If a port is used as an input port the strobe signal STB controls the input port latch. The input latch is transparent if STB = high. The data at the inputs of a port is latched at the high-to-low transition of STB. If the latches are not used STB must be set tied high.

The signal DT/$\overline{R}$IN determines the buffer transfer direction. DT/$\overline{R}$IN is latched at the falling edge of STB. With DT/$\overline{R}$IN = low (high) the transfer is performed from port W to port V (from port V to port W). DT/$\overline{R}$IN may be connected to the DT/$\overline{R}$OUT output of the bus controller part in operating mode 4. The data outputs of a port including the parity and parity error outputs are enabled with $\overline{DENIN}$ = low. If $\overline{DENIN}$ = high the data and parity output lines are driven into the high-impedance state and the parity error outputs is driven inactive. $\overline{DENIN}$ may be connected to the $\overline{DENOUT}$ output of the bus controller part in operating mode 4.

The polarity of the data at port W is inverted by INVW = high. This also inverts the parity inputs/outputs. Using the swap feature by activating SWAP/CEN286 = high, the data at the input port lines 0-7 (8-15) is swapped bytewise to the output port lines 8-15 (0-7). SWAP is latched with ALE if $\overline{AEN}$ = low (see description of bus controller part). If $\overline{AEN}$ = high SWAP is not latched and affects directly the swap logic.

Parity Modes

In operating mode 4 the SAB 82220 supports 2 parity modes (figure 14) with even or odd parity generating and checking. The selection of these modes is done with pin strapping. An even (odd) parity bit is set if the data which must be protected has an odd (even) number of 1s. In parity mode B the bus width of port V and W is reduced to 16 bit. The two parity generators/checkers produce and check 2 parity bits, one for the lower and one for the higher byte of the 16-bit port. In case of an 8-bit transfer with parity logic enabled the unused part of the ports must have well defined contents and a proper parity bit, too. Otherwise, undesired parity error conditions may result.

Parity mode A

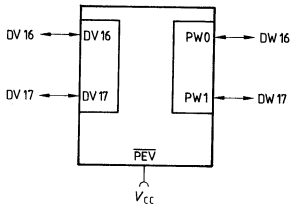
In parity mode A the parity logic is disabled. In this mode the ports have the full width of 18 bits. Parity mode A is selected by strapping $\overline{PEV}$ to V_{CC}.

Parity mode B

Parity mode B is enabled by connecting $\overline{PEV}$ to GND. In this mode 2 parity generators and checkers are available at port W. The PW0 and PW1 parity input/output lines correspond to DW0-7 and DW8-15. The parity generators are active during a transfer from port V to port W. The parity checkers are in use if a transfer is performed from port W to port V. If a parity error occurs at minimum on one of the parity inputs, the parity error signal $\overline{PERR}$ will go low. $\overline{PERR}$ is an open-drain output and must be externally connected via a pullup resistor to V_{CC}. If PE/$\overline{O}$ = low (high), odd (even) parity mode is selected.

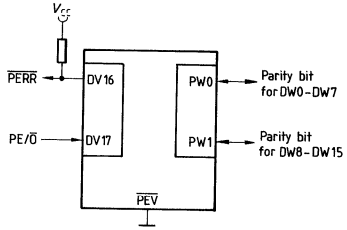
Figure 14
Parity Modes in Operating Mode 4

Parity Mode A: $\overline{PEV} = V_{CC}$



Parity generating/checking disabled
18-bit bus width

Parity Mode B: $\overline{PEV}$ = GND



Parity generating if transfer from V → W

Parity checking if transfer from W → V

SAB 8288 Compatible Bus Controller Mode

The bus controller part of the BIC in operating mode 4 is programmed to work in an SAB 8288 compatible mode by strapping MOD286 to GND. In this bus controller mode the command logic decodes the three SAB 8086/8088/80186/80188 status lines $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ to determine which bus cycle is to be performed (figure 15). In case of an SAB 8086/8088 system the clock input CLK of the BIC is connected to the CLK output of the SAB 8284B clock generator. In an SAB 80186/80188 system the CLKOUT line of the microprocessor is connected to the CLK input of the SAB 82220.

Figure 15
SAB 8288A Compatible Bus Controller Status Coding

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Processor State	Active Command Output Line
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$
0	1	1	Halt	None
1	0	0	Code Fetch	$\overline{MRDC}$
1	0	1	Read Memory Data	$\overline{MRDC}$
1	1	0	Write Memory Data	$\overline{MWTC}$
1	1	1	Passive State	None

Five command outputs are available: $\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$ and $\overline{INTA}$. $\overline{MRDC}$ and $\overline{MWTC}$ are used as read and write-enable lines to ROM and RAM devices. Reading from or writing to I/O devices is performed by the $\overline{IORC}$ and $\overline{IOWC}$ command lines. The $\overline{INTA}$ command line is active as an I/O-read control during an interrupt cycle. All command lines are forced into the inactive state (high) with CEN86 = low. CEN86 = high enables all command lines. The state of the command outputs is also affected by $\overline{AEN}$. $\overline{AEN}$ = high puts all command outputs into the high-impedance state and $\overline{DENOUT}$ in the inactive state (high). With $\overline{AEN}$ = low the command lines are enabled.

The write command lines $\overline{MWTC}$ and $\overline{IOWC}$ will go active 1 clock cycle earlier if the Multibus select input MB = low. This feature is comparable to the advanced write function of the SAB 8288A except that the SAB 8288A has two separate advanced write command output lines.

The MCE output is active during an interrupt sequence. It is used to control the transfers of a cascade address from a master interrupt controller (SAB 8259A) at the local bus via the address latch (controlled by ALE) to the cascade address inputs of the slave interrupt controllers at the system bus. With MCE = high, additional cascade address drivers may be enabled to put the cascade address on the local bus. This cascade address may be strobed into the address latch with ALE.

If the bus transceiver part of the BIC is used as the data bus transceiver with port V at the local bus (CPU) side, $\overline{DENOUT}$ and DT/$\overline{ROUT}$ should be connected directly to $\overline{DENIN}$ and DT/$\overline{RIN}$.

The inputs CMDLY and $\overline{READY}$ are not used in the SAB 8288 compatible bus controller mode.

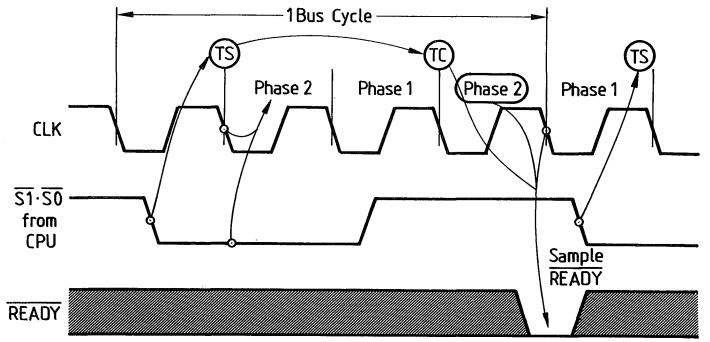
SAB 82288 Compatible Bus Controller Mode

Bus State and Cycle Definition

The bus controller part in the SAB 82288 compatible mode operates with three bus states: idle (TI), status (TS) and command (TC) state (figure 16). Each of these bus states is two CLK cycles long. The TI state occurs when no bus cycle is currently active at the SAB 80286 local bus. A bus cycle starts with a TS state and ends after one or more TC states.

$\overline{S0}$ and $\overline{S1}$ are sampled every falling edge of CLK and if they become active (low) the local bus enters the TS state. The TC state follows the TS state. The shortest bus cycle has one TS and one TC state. Longer bus cycles are performed by repeating TC states. At the end of each TC state $\overline{READY}$ is sampled and if detected high, a new TC state, a wait state, is inserted. The control and command outputs do not change their state during wait states. When $\overline{READY}$ is sampled low, the current bus cycle is terminated.

Figure 16
Bus Cyde Definition SAB 82288 Compatible Mode



Operating Modes

Two types of buses are supported by the BIC in the SAB 82288 compatible bus controller mode: Multibus and non-Multibus. In Multibus mode, which is programmed by MB = high, the activation of the command and control outputs is delayed to meet the IEEE-796 (Multibus) specification concerning address to command active and write data to command active setup timing. Therefore one wait state is required in the Multibus cycle. The non-Multibus mode (MB = low) does not require wait states. In this mode the swap feature of the bus transceiver is disabled.

Command and Control Outputs

The command logic decodes the status lines M/$\overline{IO}$, $\overline{S1}$ and $\overline{S0}$ of the SAB 80286 CPU to determine which command line is to be issued. The CLK output of the SAB 82284 system clock generator must be connected to the CLK input of the BIC. Figure 17 indicates the cycle decoding of the SAB 82288 compatible mode and the effect on command, DT/$\overline{ROUT}$, $\overline{DENOUT}$, ALE and MCE outputs.

Figure 17
SAB 82288 Compatible Bus Controller Status Coding

Type of Bus Cycle	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Command Activated	DT/$\overline{R}$OUT State	ALE, $\overline{DENOUT}$ Issued?	MCE Issued?
Interrupt Acknowledge	0	0	0	$\overline{INTA}$	Low	Yes	Yes
I/O Read	0	0	1	$\overline{IORC}$	Low	Yes	No
I/O Write	0	1	0	$\overline{IOWC}$	High	Yes	No
None; Idle	0	1	1	None	High	No	No
Halt/Shutdown	1	0	0	None	High	No	No
Memory Read	1	0	1	$\overline{MRDC}$	Low	Yes	No
Memory Write	1	1	0	$\overline{MWTC}$	High	Yes	No
None; Idle	1	1	1	None	High	No	No

Three different types of bus cycles may occur: read, write and halt. Read bus cycles include memory read, I/O read and interrupt acknowledge. For all read bus cycles the timing of command outputs, ($\overline{MRDC}$, $\overline{IORC}$, $\overline{INTA}$), control outputs (ALE, $\overline{DENOUT}$, DT/$\overline{R}$OUT) and control inputs ($\overline{AEN}$, CENL, CMDLY, MB, $\overline{READY}$) is identical. Read cycles differ only in the command output activated. The MCE control output is only asserted during interrupt acknowledge cycles. The two possible write bus cycles activate the $\overline{MWTC}$ or $\overline{IOWC}$ outputs. The control outputs/inputs of a write bus cycle have a different timing than read bus cycles. During halt bus cycles no command or control output is activated. All control inputs are ignored until the next bus cycle is started via $\overline{S1}$ and $\overline{S0}$.

The basic command and control output timings for read and write bus cycles are shown in the figures 18 to 22. The signal label $\overline{CMD}$ represents the appropriate command output for the bus cycle. For the 5 figures the CMDLY input is connected to GND and CENL to V_{CC}. The next 3 figures show non-Multibus cycles with MB = low.

Figure 18
Idle-Read-Idle Bus Cycles with MB = 0

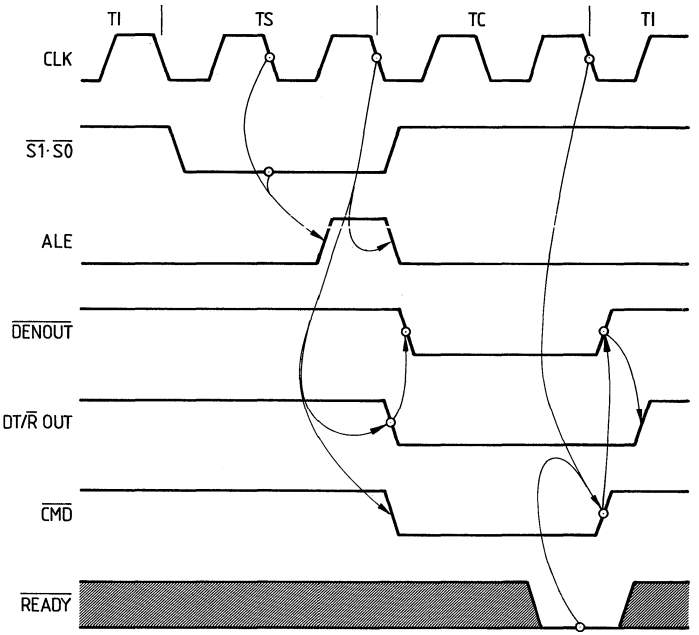


Figure 18 shows a read cycle with no wait state. Figure 19 shows a write cycle with one wait state. The READY input is shown to illustrate how wait states are added.

Bus cycles can occur back-to-back with no TI bus state between TC and TS. Back-to-back cycles do not affect the timing of the command and control outputs. They always reach the states shown for the same clock edge (within TS, TC or following bus state) of a bus cycle.

A special case in control timing occurs for back-to-back write cycles with MB = low. In this case, DT/ROUT remains high and DENOUT remains low (see respective write-write bus cycle diagram). The command and ALE output timing does not change.

Figure 19
Idle-Write-Idle Bus Cycles with MB = 0

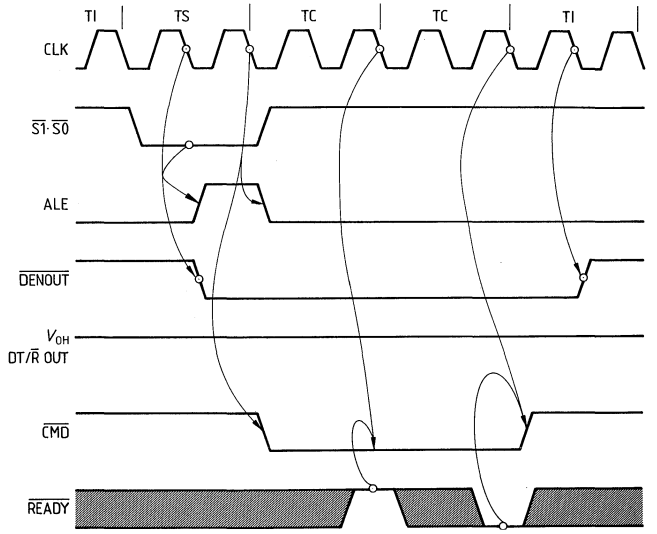
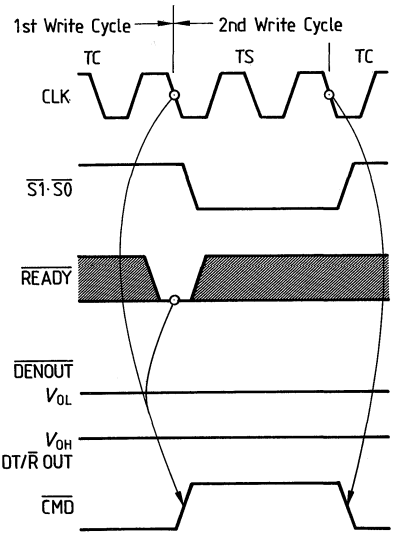


Figure 20
Write-Write Bus Cycles with MB = 0



In the Multibus bus controller mode (MB = high) the timing of command and $\overline{\text{DENOUT}}$ outputs has changed. These outputs are automatically delayed to satisfy three requirements:

1. 50 ns minimum setup time for valid address before any command output becomes active.
2. 50 ns minimum setup time for valid write data before any write command output becomes active.
3. 65 ns maximum time from when any read command becomes inactive until the slave's read data drivers reach tristate off.

Therefore three signal transitions are delayed by MB = high, compared to the timing with MB = low:

1. The high-to-low transition of $\overline{\text{IORC}}$, $\overline{\text{MRDC}}$ and $\overline{\text{INTA}}$ is delayed for one clock cycle.
2. The high-to-low transition of $\overline{\text{IOWC}}$ and $\overline{\text{MWTC}}$ is delayed for two clock cycles.
3. The high-to-low transition of $\overline{\text{DENOUT}}$ for write cycles is delayed for one CLK cycle.

Due to the Multibus requirements, at least one wait state (TC) must be inserted in every bus cycle via $\overline{\text{READY}}$ (if MB = high).

Figure 21
Idle-Read-Idle Bus Cycles with MB = 1

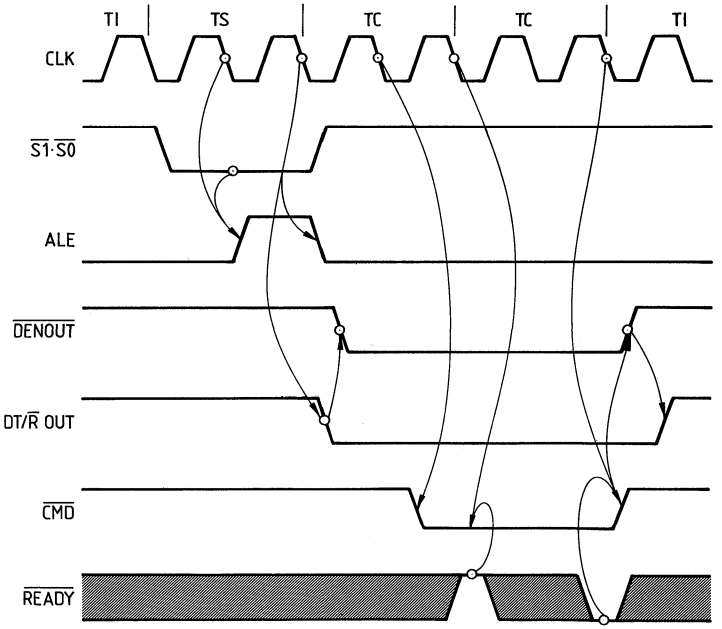
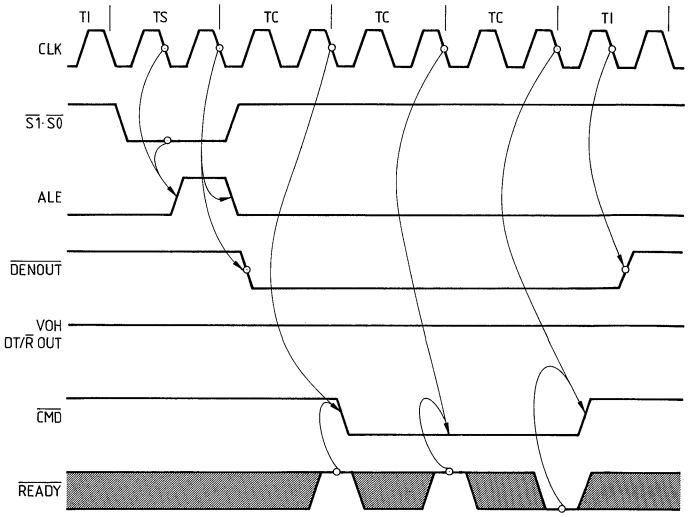


Figure 22
Idle-Write-Idle Bus Cycles with MB = 1

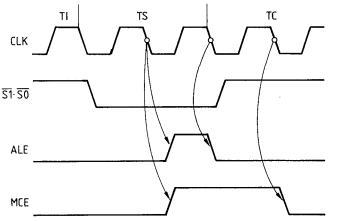


Back-to-back bus cycles with MB = high do not change the timing of any of the command or control outputs. DENOUT always becomes inactive between bus cycles with MB = high.

Except for a halt or shutdown cycle ALE will be issued during the second half of TS for any bus cycle. ALE becomes inactive at the end of the TS state to allow latching the address to keep it stable during the entire bus cycle. ALE is not affected by any control input.

Figure 23 shows the MCE timing during interrupt acknowledge bus cycles. MCE is one CLK cycle longer than ALE to hold the cascade address from a master SAB 8259A interrupt controller valid after the falling edge of ALE. With the exception of the MCE control output, an INTA bus cycle is identical in timing with a read bus cycle.
MCE is not affected by any control input.

Figure 23
MCE Operation for an INTA Bus Cycle



The transfer direction of a data bus transceiver may be controlled by DT/ROUT. During write bus cycles DT/ROUT stays at high level. With DENOUT (at the BIC active low instead of active high at the SAB 82288) the outputs of a bus transceiver may be enabled.

Control Inputs

The control inputs can alter the basic timing of command outputs, allow interfacing to multiple buses, and share a bus between different masters. An SAB 80286 system may have several bus controllers but only one bus controller may be used to perform a bus cycle. Some buses may be shared by more than one CPU (e.g. Multibus) requiring only one of them to use the bus at a time.

Systems with multiple and shared buses use two control input signals of the bus controller: $\overline{AEN}$ and CENL. $\overline{AEN}$ enables the command outputs of the bus controller and CENL enables the bus controller to control the current bus cycle. CENL is latched at the end of each TS state. If CENL is sampled low the command outputs and $\overline{DENOUT}$ will not go active and DT/$\overline{R}$OUT will stay high. In this case the bus controller will ignore the CMDLY and $\overline{READY}$ inputs until another bus cycle is started via $\overline{S0}$ and $\overline{S1}$. During a write bus cycle with MB = low, $\overline{DENOUT}$ becomes active before CENL is sampled. So if CENL is sampled low, the $\overline{DENOUT}$ will be forced high during TC. $\overline{AEN}$ going inactive (high) immediately puts the command outputs into the high-impedance state and $\overline{DENOUT}$ into the inactive state (high). $\overline{AEN}$ is intended to be driven by a bus arbiter (SAB 82289 or a BIC in operating mode 5) which assures that only one bus controller is driving a shared bus at any time. $\overline{AEN}$ goes inactive only during TI or TS bus states but may become active during any T-state. $\overline{AEN}$ = low immediately allows $\overline{DENOUT}$ to go to the appropriate state. Three CLK edges later, the command outputs will go active (MB = high). The Multibus requires this delay for the address and data to be valid at the bus before the commands become active.

If MB = low the asynchronous input CEN286 also affects the command and $\overline{DENOUT}$ outputs. With CEN286 = low the command outputs and $\overline{DENOUT}$ are immediately forced inactive. When CEN286 makes a low-to-high transition the command outputs and $\overline{DENOUT}$ go to the appropriate state. $\overline{READY}$ must still become active to terminate a bus cycle if CEN286 remains low for a selected bus controller (CENL was latched high).

With the CMDLY input the activation of commands can be delayed. If CMDLY is sampled high at the end of a TS state, the command output is not activated and CMDLY is again sampled at the next falling edge of CLK. Once sampled low, the proper command output becomes active immediately if MB = low. If MB = high the proper command output goes active with a delay, CMDLY does not affect the control output ALE, MCE, $\overline{DENOUT}$ and DT/$\overline{R}$OUT. $\overline{READY}$ may terminate a bus cycle before CMDLY allows a command to be issued. In this case the bus controller will deactivate $\overline{DENOUT}$ and DT/$\overline{R}$OUT in the same manner as if a command had been issued.

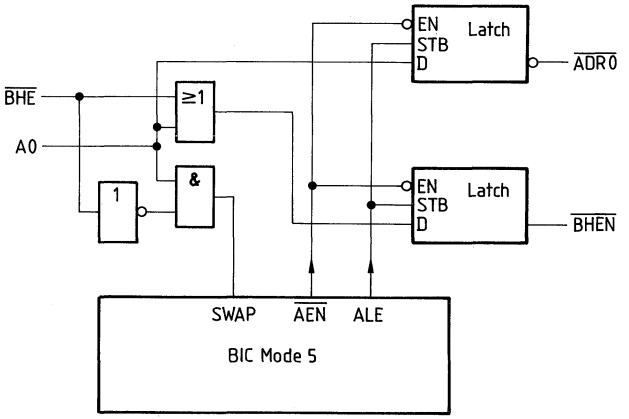
Operating Mode 5

Transceiver Operation

In operating mode 5 the BIC offers a 16-bit transceiver with the bidirectional input/output lines DV0–15 and DW0–15. No latch function is available in mode 5. The control of the transceiver transfer direction and output enable is achieved internally by the bus controller part if $\overline{AEN}$ = low. If the SAB 82220 has an access right to the Multibus ($\overline{AEN}$ = high), the transceiver may be controlled externally via DT/$\overline{R}$IN and $\overline{DEN}$IN. This feature can be used in a system where the data transceiver must be controlled also by another master at a multiprocessor system bus (e.g. programming of an ADMA controller in a remote mode system). The outputs of the ports are enabled with $\overline{DEN}$IN = low. DT/$\overline{R}$IN selects the buffer transfer direction. With DT/$\overline{R}$IN = low (high) the data transfer is performed from port W to port V (from port V to port W).

The polarity of port W may be inverted by INVW/$\overline{LOCK}$ = high during RESET active (high). If INVW/$\overline{LOCK}$ = low during RESET, true polarity of port W is selected. The swap feature is selected via the SWAP input. SWAP is internally latched with ALE. If SWAP is sampled high the data at the input port at the lines 0–7 (8–15) is swapped bytewise to the output port lines 8–15 (0–7). If the byte swapping feature is used in a Multibus configuration, the decoding concerning the SWAP input and the generation of the Multibus signal $\overline{BHEN}$, must be done externally (see figure 24).

Figure 24
Generation of SWAP and $\overline{BHEN}$ for BIC and Multibus in Mode 5



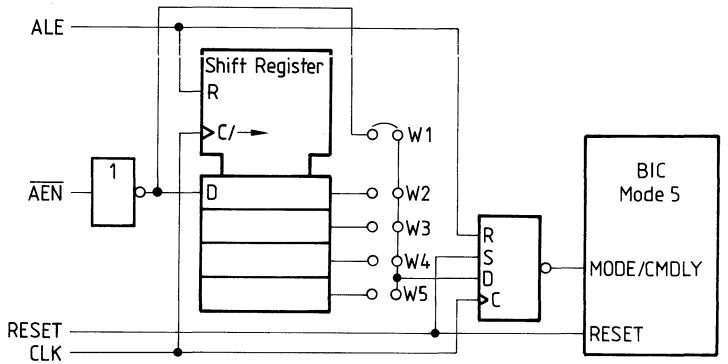
SAB 82288 Compatible Bus Controller

The SAB 82220 bus controller part in operating mode 5 always works in an SAB 82288 compatible mode. For a detailed description of this mode refer to the functional description of operating mode 4. This section only describes the differences of the bus controller part between operating mode 4 and 5.

The mode 5 bus controller always generates Multibus cycles. Therefore no MB input signal is available. The transceiver control outputs (DT/$\overline{R}$, $\overline{DEN}$) of the bus controller are not available outside the BIC. If $\overline{AEN}$ = low they directly control internally the bus transceiver. $\overline{AEN}$ is an output signal of the bus arbiter part. It is internally wired to the bus controller and externally available at $\overline{AEN}$. No command enable/disable input is available in mode 5. The control of the bus controller command outputs is done via the SYSB/$\overline{RESB}$ bus arbiter input.

Additionally to the mode programming via BMOD, SUBMOD0 and SUBMOD1, the MODE/CMDLY input is used during initialization with RESET. If the command delay function of the bus controller part is not used, MODE/CMDLY must be connected to GND. If the command delay feature is needed (MODE/CMDLY = low during RESET active), the circuit of figure 25 may be used to realize the command delay and the mode 5 initialization requirements.

Figure 25
Mode 5 Initialization when Using the Command Delay Feature



Connections	Number of Delay Cycles n
W1	1
W2	2
W3	3
W4	4
W5	5

In the circuit shown in figure 25, MODE/CMDLY is low during the active RESET state. In this way mode 5 is invoked. After RESET going inactive (low), the occurence of ALE during $\overline{AEN}$ = low activates MODE/CMDLY= high for n CLK cycles. If ALE occurs during $\overline{AEN}$ = high, MODE/CMDLY is activated for n CLK cycles after $\overline{AEN}$ has gone low. Up to 5 delay cycles are generated with the circuit of figure 25. Using longer shift registers, a larger number of delay cycles may be generated.

SAB 82289 Compatible Bus Arbiter

The bus arbiter part of the BIC in operating mode 5 interfaces an SAB 80286 processor or an SAB 82258 (ADMA) in remote mode to a multimaster system bus (e.g. Multibus). The bus arbiter performs all signaling to request, obtain and release the system bus. External logic is required to determine which bus cycle requires the system bus and to resolve the priorities of simultaneous requests for control of the system bus.

In an SAB 80286 system using the bus arbiter of the BIC, the CPU is unaware of the arbiter's existence and issues commands as if it would have exclusive use of a multimaster system bus. If the processor cycle requires Multibus access the arbiter requests control of the Multibus. Until the request is granted the bus arbiter keeps $\overline{AEN}$ disabled to prevent the bus controller and the address latches from accessing the Multibus. $\overline{AEN}$ inactive also disables the asynchronous ready enable (ARDYEN) input of an SAB 82284 clock generator so that the system bus will appear as not ready for the SAB 80286.

Typically, once the data transfer command has been issued by the bus controller part and the data transfer has taken place, a transfer acknowledge ($\overline{XACK}$ at Multibus) signal is returned to the processor on the multimaster system bus to indicate a "ready" from the accessed slave device. The processor remains in repeated TC states (wait states) until the addressed device responds with $\overline{XACK}$ to the SAB 82284 $\overline{ARDY}$ input and the SAB 82284 asserts $\overline{READY}$ to the processor. The CPU then completes its bus cycles. (Details about bus state and bus cycle definitions concerning the SAB 80286 are given in the description of operating mode 4.)

CPU interface

The interface between CPU and bus arbiter includes two groups of control input and outputs: status inputs and local system control I/O lines.

The status inputs include the SAB 80286 bus interface lines $\overline{S0}$, $\overline{S1}$, M/$\overline{IO}$, CLK and $\overline{READY}$. $\overline{S0}$, $\overline{S1}$ and M/$\overline{IO}$ define the type of a bus cycle and are directly connected to the corresponding outputs of the CPU (ADMA). The CLK input and the $\overline{READY}$ input of the BIC are connected to the corresponding outputs of an SAB 82284 clock generator. $\overline{READY}$ must be low during RESET. The M/$\overline{IO}$ line is also used to select a special bus arbiter mode, the ADMA mode. Local system control lines are INVW/$\overline{LOCK}$, $\overline{CBQLCK}$/$\overline{ALWAYS}$, SYSB/$\overline{RESB}$, RESET and $\overline{AEN}$.

The RESET input serves for two functions: mode initialization and resetting of the bus arbiter logic. By activating RESET, all pending requests of the bus arbiter are cleared and the multimaster system bus is released.

SYSB/$\overline{RESB}$ is an input signal which determines whether the multimaster system bus is required for the current bus cycle. The signal can be generated from an address decoder attached to the processor's address lines. If SYSB/$\overline{RESB}$ is sampled high at the end of a TS state, the bus arbiter will request or retain control of the system bus. During an interrupt acknowledge cycle SYSB/$\overline{RESB}$ is sampled high or the bus cycle is terminated by the $\overline{READY}$ line.

The $\overline{AEN}$ output of the bus arbiter controls the address latches, the command outputs of the mode 5 internal bus controller and the ready logic inside an SAB 82284 clock generator. With $\overline{AEN}$ = 1 address latch output drivers and bus controller command outputs are disabled and also the asynchronuous ready input ($\overline{ARDY}$) of the SAB 82284, $\overline{AEN}$ goes active relative to $\overline{BCLK}$ and goes inactive relative to CLK.

The $\overline{CBQCLK}$/$\overline{ALWAYS}$ and the INVW/$\overline{LOCK}$ signal are discussed later in the operating mode 5 description.

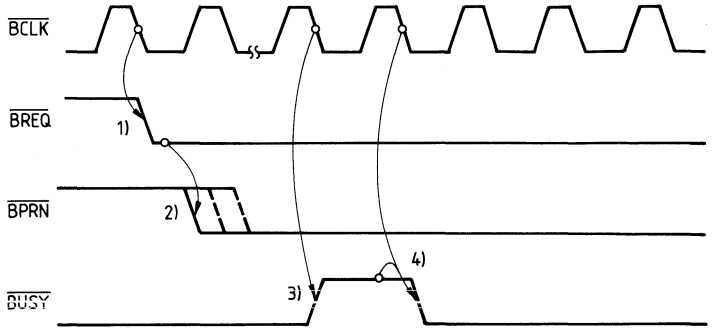
Arbitration between bus masters

The Multibus protocol allows multiple processing elements to compete with each other in accessing common system resources. Since the local SAB 80286 processor does not have exclusive use of the system bus, if the Multibus is "BUSY", the SAB 80286 processor will have to wait before it can access the system bus.

The bus arbiter provides an integrated solution for controlling access to a multimaster system bus. The bus arbiter allows both higher and lower priority bus masters to acquire the system bus depending on which release mode is used. In general higher priority masters obtain the bus immediately after any lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus or the proper surrender conditions exist. The bus arbiter handles this arbitration in a manner completely transparent to the bus master (e.g. SAB 80286 processor).

At the end of each transfer, the arbiter may retain or release the system bus. This decision is controlled by the processor state, bus arbitration inputs and arbiter strapping options.

Figure 26
Bus Exchange Timing for the Multibus



1) Higher Priority Bus Arbiter Requests the Multimaster System Bus.
2) Attains Priority.(Does not Yet Own Bus).
3) Lower Priority Arbiter Releases $\overline{\text{BUSY}}$.
4) Higher Priority Bus Arbiter then Acquires the Bus and Pulls $\overline{\text{BUSY}}$ Low.

Priority resolving techniques

Some means of resolving priority between bus masters requesting the multimaster bus simultaneously must be provided. The bus arbiter supports parallel, serial and rotating system bus priority resolving techniques. All of these techniques are based on the concept that, at a given time, one bus master will have priority above all the others.

An individual arbiter is the highest priority arbiter requesting the Multibus when its $\overline{\text{BPRN}}$ input is asserted (low). The highest priority requesting arbiter cannot immediately seize the system bus. It must wait until the present bus transaction is completed. Upon completing its current transaction the present bus owner surrenders the bus by releasing $\overline{\text{BUSY}}$.

$\overline{\text{BUSY}}$ is an active-low "wired OR" Multibus signal connecting all bus arbiters on the system bus. When $\overline{\text{BUSY}}$ goes inactive, the arbiter which has requested the system bus and presently has bus priority ($\overline{\text{BPRN}}$ = low), seizes the bus by pulling $\overline{\text{BUSY}}$ low (see waveform in figure 26).

The generation of a multimaster bus request ($\overline{\text{BREQ}}$) is controlled by the type of bus cycle and the SYSB/$\overline{\text{RESB}}$ input. Whenever the processor signals the status for memory read, memory write. I/O read, I/O write or interrupt acknowledge cycle, and SYSB/$\overline{\text{RESB}}$ is high at the end of TS, a bus request is generated.

When the status inputs indicate an interrupt acknowledge bus cycle, the arbiter allows external logic to decide (through the SYSB/$\overline{\text{RESB}}$ input) whether the interrupt acknowledge cycle should use the Multibus.

Figure 27 shows how SYSB/$\overline{\text{RESB}}$ is repeatedly sampled until it is sampled high or the bus cycle is terminated. If the bus cycle is completed ($\overline{\text{READY}}$ is sampled low) before SYSB/$\overline{\text{RESB}}$ is sampled high, the arbiter will not request the Multibus.

The bus arbiter does not generate a separate $\overline{\text{BREQ}}$ for each bus cycle. Instead the bus arbiter generates $\overline{\text{BREQ}}$ when it requests the bus and holds $\overline{\text{BREQ}}$ active during the time that it has possession of the bus. Note that all multimaster system bus requests (via $\overline{\text{BREQ}}$) are synchronized to the system bus clock ($\overline{\text{BCLK}}$).

Figure 27
Bus Request Timing during an Interrupt Acknowledge Cycle

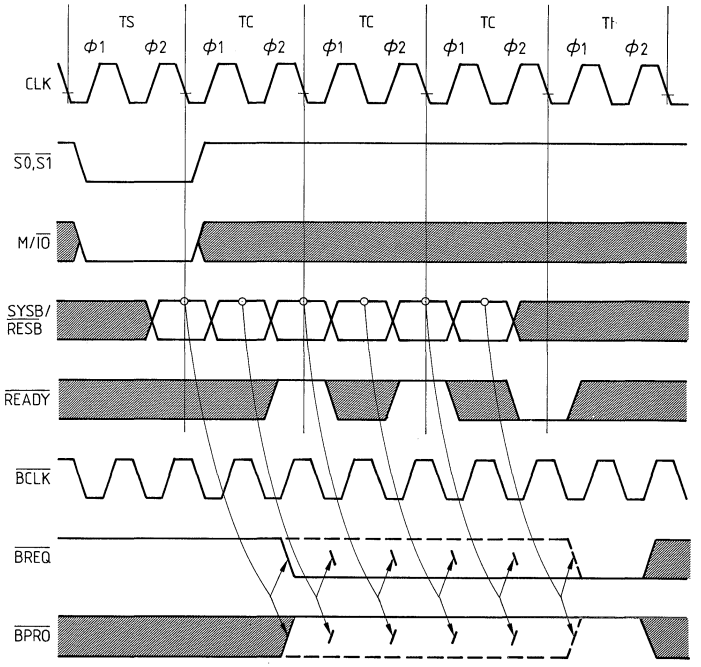


Figure 28
Parallel Priority Resolving Technique

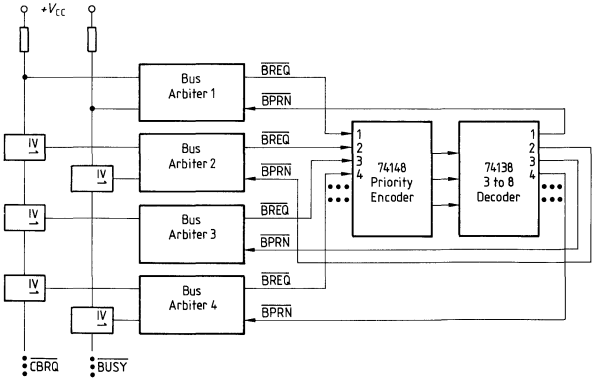
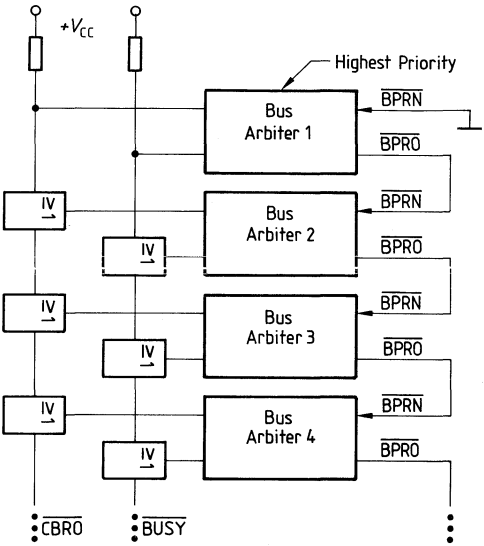


Figure 29
Connections for Serial Priority Resolving Technique



Parallel priority resolving technique

The parallel priority resolving technique requires a separate bus request line (BREQ) for each arbiter on the multimaster system bus (see figure 28). Each BREQ line enters a priority encoder which generates the binary address of the highest priority BREQ line currently active. The binary address is decoded to select the BPRN line corresponding to the highest priority arbiter requesting the bus. In a parallel scheme, the BPRO output is not used.

The arbiter receiving priority (BPRN low) then allows its associated bus master onto the multimaster system bus as soon as the bus becomes available (i.e. the bus is no longer busy). Any number of bus masters may be accommodated in this way, limited only by the complexity of the external priority resolving circuitry. Such circuitry must resolve the priority within one BCLK period.

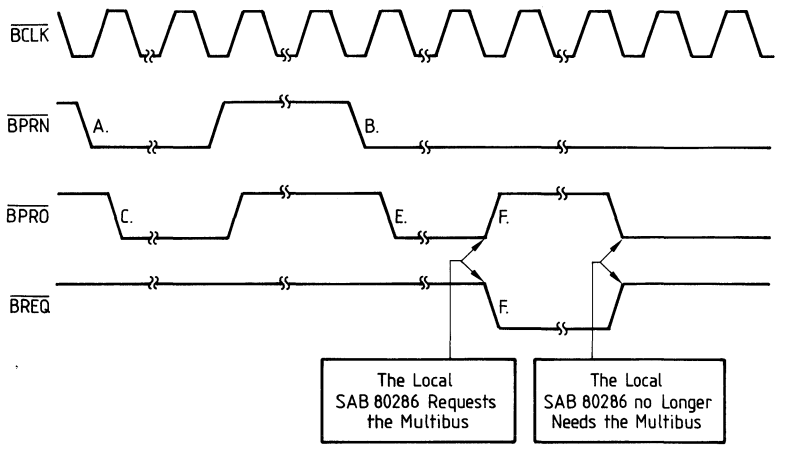
Serial priority resolving technique

The serial priority resolving technique eliminates the need for the priority circuitry of the parallel technique by daisy-chaining the bus arbiters together, that is, connecting the higher priority arbiter's BPRO output to the BPRN of the next lower priority arbiter (see figure 29). The highest priority bus arbiter would have its BPRN tied low in this configuration, signifying to the arbiter that it always has the highest priority when requesting the system bus. In a serial scheme, the BREQ output is not used.

Since arbitration must be resolved within one BCLK period the number of arbiters connected together in the serial priority is limited by the arbiter's BPRN to BPRO propagation delay.

$$\text{Maximum number of chained-priority devices} = \frac{\overline{\text{BCLK}}\text{ period}}{\overline{\text{BPRN}}\text{ to }\overline{\text{BPRO}}\text{ delay}}$$

Figure 30
Serial Priority Bus Behavior



Note: Events A through F described in the following.

When using the serial priority resolving scheme, a higher priority arbiter (for example, arbiter 2, figure 29) passes priority to the next lower priority arbiter (arbiter 3) by asserting its $\overline{BPRO}$ signal (low). This asserts $\overline{BPRN}$ of next arbiter (arbiter 3) as shown in figure 30, event A and event B. An arbiter's $\overline{BPRO}$ is asserted if the arbiter has priority ($\overline{BPRN}$ is asserted) but is not accessing or requesting the system bus (as indicated by $\overline{BREQ}$ inactive as shown in figure 30, event C and event E for arbiter 3). Whenever a higher priority arbiter (arbiter 3) issues a bus request its $\overline{BPRO}$ goes inactive causing the next lower priority arbiter (arbiter 4) to lose its bus priority (figure 30, event F). Any arbiter (arbiter 3) will also bring its $\overline{BPRO}$ inactive if its $\overline{BPRN}$ goes inactive (from arbiter 2), thereby passing the loss of bus priority on to the lower priority arbiters (e.g. arbiter 4) as shown in figure 30, event D.

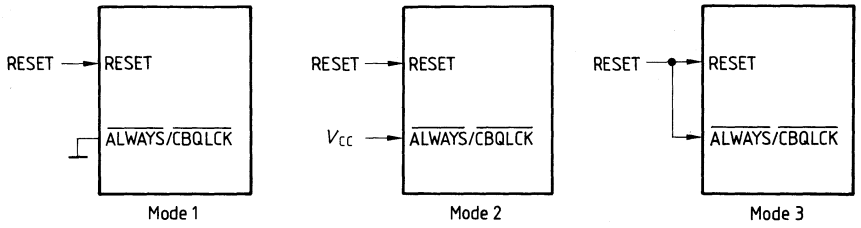
Rotating priority resolving technique

The rotating priority resolving technique is similar to the parallel priority resolving technique except that priority is dynamically re-assigned. The priority encoder is replaced by a more complex circuitry which rotates priority between requesting arbiters, thus giving each arbiter an equal chance to use the multimaster system bus over a given period of time.

Selecting the appropriate priority resolving technique

The choice of a priority resolving technique involves a trade-off between external logic complexity and ease of Multibus access for the different bus masters in the system. The rotating priority resolving technique requires a substantial amount of external logic, but guarantees all the bus masters an equal opportunity to access the system bus. The serial priority resolving technique uses no external logic but has fixed bus master priority levels and can accommodate only a limited number of bus arbiters. The parallel priority resolving technique is in general a compromise between the other two techniques (for example the parallel priority configuration of figure 20 allows up to eight arbiters to be present on the Multibus, with fixed priority levels, while not requiring a large amount of complex external logic to implement).

Figure 31
BIC Mode 5 – Release Mode Configurations



BIC Mode 5 – Release Modes

Release Mode	Conditions under which the Bus Arbiter Releases the System Bus
Mode 1	The bus arbiter always releases the bus at the end of each transfer cycle. In ADMA mode, the ADMA's HLDA is tied low and the BIC releases the bus when the ADMA has finished its unseparable cycles indicated through HOLD line low (SYSB/$\overline{RESB}$ = 0).
Mode 2	The bus arbiter retains the bus until: • a higher-priority bus master requests the bus, driving $\overline{BPRN}$ high • a lower-priority bus master requests the bus by pulling $\overline{CBRQ}$ low
Mode 3	The bus arbiter retains the bus until: • a higher-priority bus master requests the bus, driving $\overline{BPRN}$ high ($\overline{CBRQ}$ low ignored)

Releasing the Multibus

Following a data transfer cycle on the Multibus, the bus arbiter can either retain control of the system bus or release the bus for use by some other bus master. It can operate in one of three modes, defining different conditions under which the arbiter relinquishes control of the multimaster system bus. These release modes are described in figure 31.

If the arbiter was programmed to operate in "always release mode" (mode 1) during the previous reset, it will surrender the Multibus after each complete transfer cycle. If the arbiter is not in "always release mode", it will not surrender the bus until the local SAB 80286 processor enters a halt state, the arbiter is forced off the bus by the loss of $\overline{BPRN}$ (mode 2 or 3), or by a common bus request when the $\overline{CBRQ}$ input is enabled by the $\overline{CBQLCK}$ input (mode 2).

The 3 bus release operating modes have the same operation when supporting either the SAB 80286 processor or the ADMA (SAB 82258) controller.

$\overline{CBRQ}$ can save the bus exchange overhead in many cases. If $\overline{CBRQ}$ is high, it indicates to the bus master that no other master is requesting the bus and therefore the present bus master can retain the bus. Without $\overline{CBRQ}$, only $\overline{BPRN}$ indicates whether or not another master is requesting the bus and this happens only if the other master is of higher priority. Between its bus transfer cycles the master must give up the bus in order to allow lower priority masters to take the bus if they need it. At the start of the master's next transfer cycle, the bus must be regained. If no other master has the bus, this can take approximately two $\overline{BCLK}$ periods. To avoid this overhead of unnecessarily giving up and regaining the bus when no other master needs it, $\overline{CBRQ}$ is extremely useful. Any master that wants but does not have the bus, must assert $\overline{CBRQ}$ (low). If the $\overline{CBRQ}$ line is not asserted the bus does not have to be released, thereby eliminating the delay of regaining the bus at the start of the next cycle.

The $\overline{LOCK}$ input to the arbiter can be used to override any of the conditions shown in figure 31. While $\overline{LOCK}$ is asserted, the arbiter will not surrender control of the Multibus to any other requesting arbiter. Note that the arbiter will surrender the Multibus (synchronous to $\overline{BCLK}$) either in response to RESET or $\overline{INIT}$ signals independent of the current release mode or the state of the arbiter inputs.

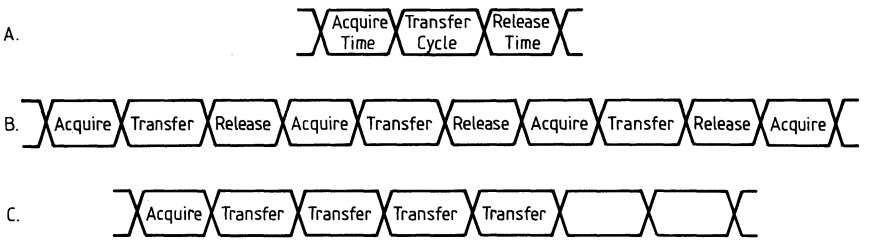
Selecting the appropriate release mode

The choice of which release mode to use may affect the bus utilization of the individual subsystems, and the system as a whole. Mode-dependent performance variations are due to the bus acquisition/release overhead. The effect of these acquire and release times on the system bus efficiency is illustrated in figure 32.

An isolated transfer on the multimaster system bus is depicted in figure 32-A. Figure 32-B shows utilization for the bus arbiter operation in mode 1. The arbiter must request and release the system bus for each transfer cycle. Lower priority arbiters have easy access to the system bus, but overall bus efficiency is low. Bus utilization for a bus arbiter operating in mode 2 or 3 is shown in the figure 32-C. In this situation the arbiter acquires the bus once for a sequence of transfers. The arbiter retains the bus until forced off by another bus master's request as defined in table of figure 31.

The three release modes of the BIC allow the designer to optimize the utilization of the Multibus.

Figure 32
Effects of Bus Contention on Bus Efficiency



Usage of INVW/$\overline{\text{LOCK}}$ input and $\overline{\text{LLOCK}}$ output

Independent of the particular release mode of the bus arbiter, the SAB 80286 processor can assert a $\overline{\text{LOCK}}$ signal synchronously to CLK to prevent the arbiter from releasing the Multibus. This software-controlled $\overline{\text{LOCK}}$ signal prevents the bus arbiter from surrendering the system bus to any other bus master, no matter whether that bus master is of higher or lower priority. The $\overline{\text{LOCK}}$ signal is typically used for implementing software semaphores for shared resources or for critical processes that must run in real time.

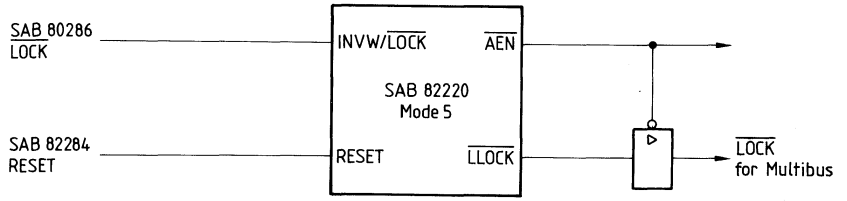
When the SAB 80286 asserts the $\overline{\text{LOCK}}$ signal, the BIC converts this temporary input into a level-lock signal ($\overline{\text{LLOCK}}$), which drives the Multibus $\overline{\text{LOCK}}$ status line. The $\overline{\text{LOCK}}$ input is sampled at the end of a TS state.

If a low is detected, $\overline{\text{LLOCK}}$ is activated (low) and the bus arbiter retains the Multibus control. $\overline{\text{LLOCK}}$ will stay active until the next unlocked bus cycle is sent from the SAB 80286. The $\overline{\text{LLOCK}}$ signal must be connected to the Multibus $\overline{\text{LOCK}}$ status line via a tristate driver, which is controlled by the $\overline{\text{AEN}}$ output of the BIC (figure 33).

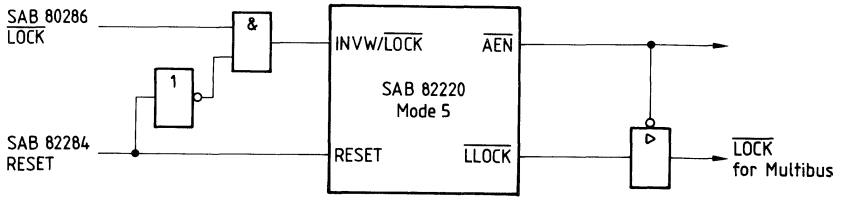
Due to pin limitation, the BIC control input INVW/$\overline{\text{LOCK}}$ has two functions: invert option of port W and $\overline{\text{LOCK}}$ support for the SAB 80286. The invert option is selected during the active RESET phase. In case of inverted polarity at port W, the SAB 80286 $\overline{\text{LOCK}}$ output is directly connected to the INVW/$\overline{\text{LOCK}}$ input of the BIC. External logic is required if true polarity of port W is desired.

Figure 33
Level Lock Generation for Multibus/Port W Polarity Selection

With inverted polarity of port W:



With true polarity of port W:

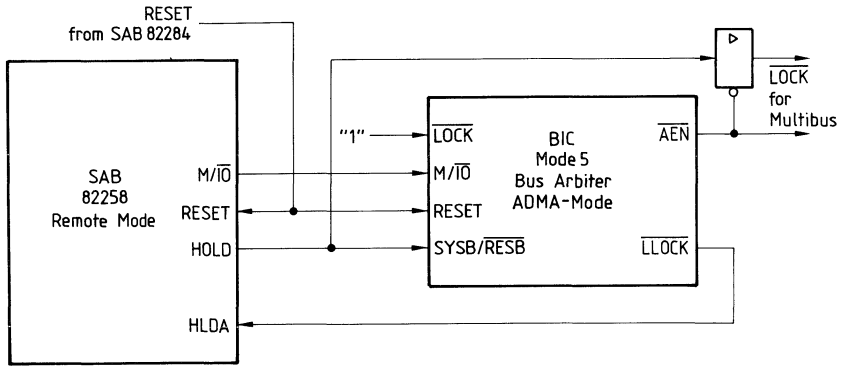


While $\overline{\text{LOCK}}$ is asserted, the arbiter will not surrender control of the Multibus to any other requesting arbiter. Note that the arbiter will surrender the Multibus in response an active RESET or $\overline{\text{INIT}}$ signal independent of the current release mode and the states of the arbiter inputs.

SAB 82258/SAB 82220 – ADMA Remote Mode Interface

When supporting the ADMA controller SAB 82258 in a remote mode configuration (the ADMA is connected to a multimaster system bus as a bus master), the HOLD output of the SAB 82258 must be connected to the SYSB/$\overline{\text{RESB}}$ pin of the BIC.

Figure 34
BIC Mode 5 – ADMA Mode Interface



During reset, the ADMA mode of the BIC is selected by a high level at the M/$\overline{\text{IO}}$ pin. Contrary to the ADMA, the SAB 80286 drives M/$\overline{\text{IO}}$ low during reset.

Working in the ADMA mode, the BIC bus arbiter will not surrender the system bus until the HOLD signal is going low, even if $\overline{\text{BPRN}}$ is high. In the ADMA mode, the $\overline{\text{LLOCK}}$ output changes its meaning. It now becomes a "system bus release request" output and is activated if another bus master is selected by the bus arbitration logic as the next active bus master.

$\overline{\text{LLOCK}}$ is connected to the HLDA (hold acknowledge) pin of the ADMA signaling to the ADMA to surrender system bus control as soon as possible. The ADMA controller will finish the system bus activities (in worst case after finishing execution of unseparable bus cycles) and deactivates its HOLD line. After HOLD has gone low, the BIC surrenders the bus, $\overline{\text{BUSY}}$ goes inactive and $\overline{\text{BPRO}}$ is put to low level. In the ADMA mode, the SYSB/$\overline{\text{RESB}}$ input is not latched.

Operating Mode 6

Transceiver/Latch Operation

In operating mode 6 the BIC offers an 18-bit address latch with the outputs DA0-17 and a bidirectional 16-bit data bus transceiver which connects the multiplexed address/data bus DX0-15 to the buffered data bus DY0-15. DX16 and DX17 are inputs to the address latch. Only the address latch at port A is controlled by ALE (address latch enable) and $\overline{AEN}$ (address enable). The information (address) at DX0-15 and DX16, DX17 is latched at the high-to-low transition of ALE. With ALE = high the latch is transparent. The outputs DA0-17 are active during $\overline{AEN}$ = low and tristated by $\overline{AEN}$ = high.

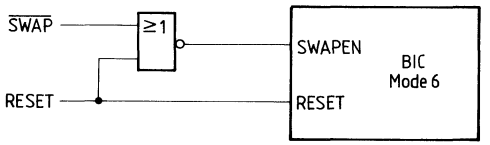
The signal DT/$\overline{R}$ selects the transfer direction of the bus transceiver. DT/$\overline{R}$ is latched at the falling edge of ALE. With DT/$\overline{R}$ = low (high), the transfer is performed from port Y to port X (from port X to port Y). $\overline{DEN}$ = low enables the output port of the bus transceiver. This output port is tristated with $\overline{DEN}$ = high.

Swap Operation

The SAB 82220 in operating mode 6 supports an automatic byte swapping capability for Multibus application as well as a manual swap control mechanism. If the swap feature is not used, SWAPEN must be tied to GND.

The manual swap mode is enabled by SWAPEN = low during RESET = high. In this mode an external signal $\overline{SWAP}$ is used to control the swap function (figure 35). With $\overline{SWAP}$ = low (SWAPEN = high the lower (bit 0-7) and the higher (bit 8-15) part of the transceiver input/output ports are swapped. $\overline{BHE}$ is latched with ALE and directly routed to the $\overline{BHEN}$ output. Also SWAPEN is latched with ALE.

Figure 35
Manual Byte Swapping in Mode 6



The automatic swap mode is selected by connecting SWAPEN to RESET. For Multibus application with an inverted polarity at address and data bus additionally MODE/INV must be tied to V_{CC} (see chapter programming). In the automatic swap mode the meaning of the $\overline{BHEN}$ output differs from that of the $\overline{BHE}$ input. In the automatic swap mode the BIC performs an automatic swap between the lower and the higher part of the data bus transceiver depending on the address line A0 (input DX0) and the input $\overline{BHE}$. This swap operation (figure 36) occurs during a byte transfer from or to an odd byte address on port X (DX0 = 1 and $\overline{BHE}$ = 0). In this case the $\overline{BHEN}$ output signal differs from the $\overline{BHE}$ input signal. $\overline{BHEN}$ is active (low) only during a transfer at DY8-DY15.

Figure 36
Automatic Byte Swapping in Mode 6

Port X Bus Operation	DX0 Address A0	$\overline{BHE}$ Input	Swap Function	Transfer Operation	$\overline{BHEN}$ Output
Word Transfer	0	0	Not Active	DX0-15 ↔ DY0-15	0
Byte Transfer on Even Address	0	1	Not Active	DX0-7 ↔ DY0-7	1
Byte Transfer on Odd Address	1	0	Active	DX8-15 ↔ DY0-7	1
–	1	1	Not Active	DX0-7 ↔ DY0-7	1

System Configurations

Figure 37
SAB 8086 System Configuration Example with BIC in Mode 6

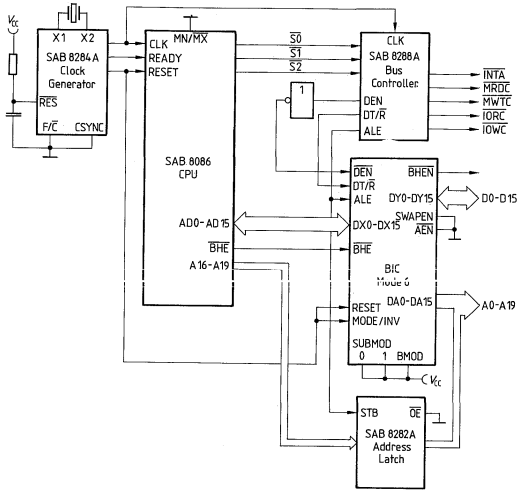


Figure 38
SAB 8086 System Configuration Example with 2 BICs in Mode 2 and 4

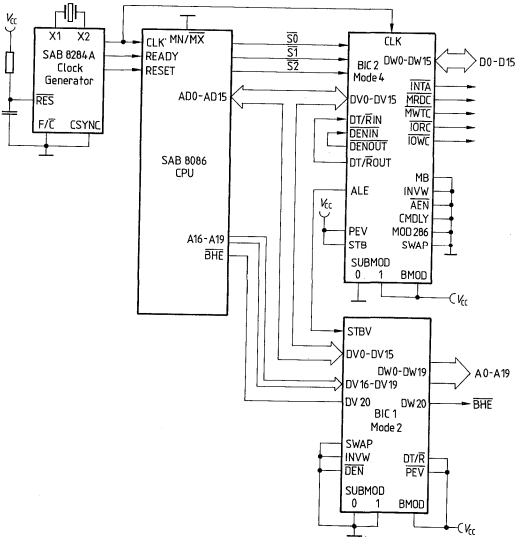


Figure 39
SAB 80186/82258 System Configuration Example with 2 BICs in Mode 2 and 4

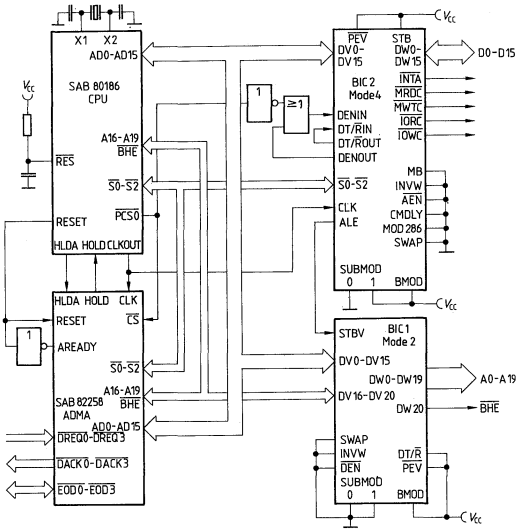


Figure 40
SAB 80186 System Configuration Example with BIC in Mode 6

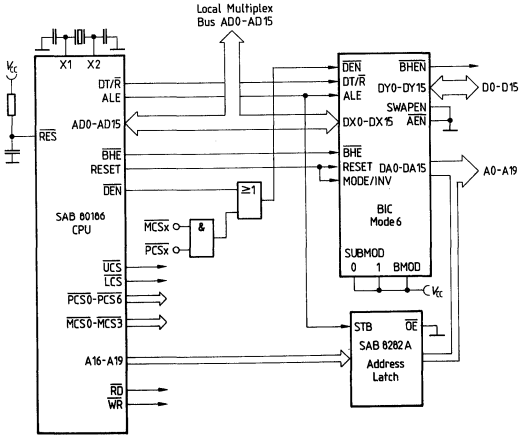
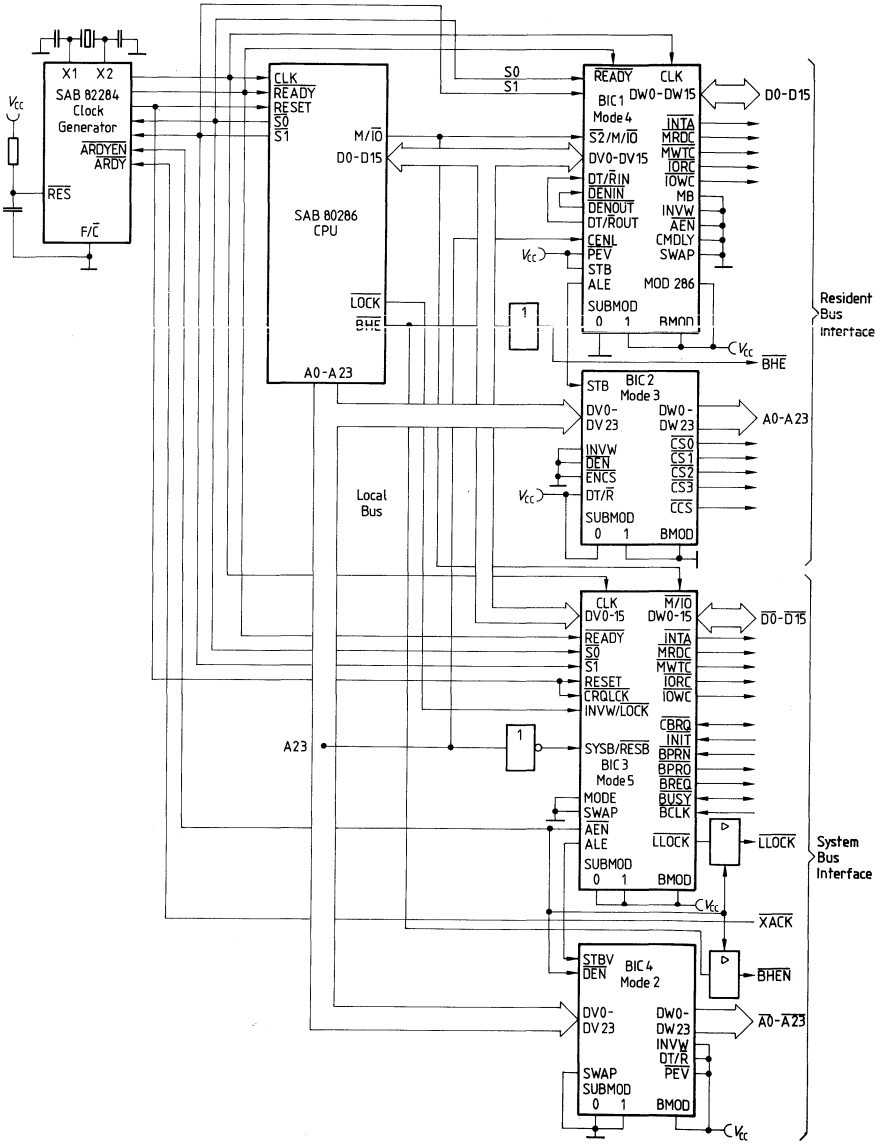


Figure 41
SAB 80286 System Configuration Example with Resident/System Bus



Absolute Maximum Ratings [1]

Ambient temperature under bias	0°C to 70°C
Storage temperature	−65°C to +150°C
All output and supply voltages	−0.5V to +7V
All input voltages	−1.0V to +5.5V
Power dissipation	650 mW

DC Characteristics

T_A = 0 to 70°C; V_{CC} = +5V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_C	Input clamp voltage	–	−1	V	I_C = −15 mA
I_{CC}	Power supply current Signal levels 0.8V/2.0V Signal levels 0.5V/3.5V	–	 130 50	 mA mA	All outputs open
I_L	Input leakage current	–	10	µA	V_R = 5.25V
I_{OFF}	Output off current	–	20	µA	0.45V<V_{OFF}<5.25V
V_{OL}	Output low voltage	–	0.45	V	[2]
V_{OH}	Output high voltage	V_{CC} −1.0	–	V	[3]
V_{IL}	Input low voltage	−0.5	0.8	V	V_{CC} = 5.0V
V_{IH}	Input high voltage	2.0	V_{CC} + 0.5V	V	V_{CC} = 5.0V
V_{ILC}	CLK input low voltage	−0.5	0.6	V	
V_{IHC}	CLK input high voltage	3.8	V_{CC} + 0.5V	V	
C_{IN}	Input capacitance	–	10	pF	f = 1 MHz, V_{CC} = 5V T_A = 25°C V_{BIAS} = 2.5V

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] I_{OL} = 48 mA in mode 1 : Y outputs
mode 2, 3 : W outputs
mode 4, 5 : W, command outputs
mode 6 : Y outputs
I_{OL} = 32 mA all other outputs

[3] I_{OH} = −15 mA in mode 1 : Y outputs
mode 2, 3 : W outputs
mode 4, 5 : W, command outputs
mode 6 : Y outputs
I_{OH} = −10 mA all other outputs

AC Characteristics

Transceiver Timing Mode 1 – 6: (Figures 42, 43, 51, 61)

T_A = 0 to 70°C; V_{CC} = +5 V ±10%

Symbol	Parameter	Limit values			Unit	Test condition[1]
		min.	typ.	max.		
t_{IVOV}	Input to output delay: mode 1					
	Port Z → port Y	6	30	46	ns	
	Other directions: lines 0–15	6	24	37	ns	
	Other directions: lines 16, 17	6	30	40	ns	
	Input to output delay: mode 2					
	Lines 0–23	6	24	37	ns	Port Y or W: TL1
	Lines 24–26	6	30	40	ns	Other outputs: TL2
	Input to output delay: mode 3 + 5	6	24	37	ns	
	Input to output delay: mode 4 + 6					
	Lines 0–15	6	24	37	ns	
	Lines 16, 17	6	30	40	ns	
t_{EHTV}	Direction hold time	5	–	–	ns	
t_{TVEL}	Direction setup time	8	–	–	ns	
t_{EHOZ}	Output disable time	6	14	28	ns	Port W or Y: TL3 Other outputs: TL4
t_{ELOV}	Output enable time	6	14	28	ns	
t_{PYOU}	Parity generation output delay	10	30	60	ns	
t_{PERR}	Parity error output delay	10	25	40	ns	
t_{CSVLD}	Data input $\overline{CSi}$ delay	10	30	50	ns	
t_{ECS}	$\overline{ENCS}$ to $\overline{CSi}$ enable time	8	24	35	ns	
t_{DCS}	$\overline{ENCS}$ to $\overline{CSi}$ disable time	8	24	35	ns	
t_{STBS}	Strobe data setup time	0	–	–	ns	
t_{STBH}	Strobe data hold time	20	–	–	ns	
t_{SHTS}	Strobe high time	20	–	–	ns	Port W or Y: TL1 Other outputs: TL2
t_{DS}	Direction control setup	10	–	–	ns	
t_{DH}	Direction control hold	10	–	–	ns	
t_{SHOV}	Strobe to output delay	5	25	40	ns	
t_{SHPV}	Strobe to parity outputs	8	30	60	ns	
t_{SHPEV}	Strobe time to parity error	8	30	60	ns	
t_{SWAP}	Swap to output delay	6	30	40	ns	
t_{SWS}	Swap setup time	0	–	–	ns	
t_{SWH}	Swap hold time	15	–	–	ns	
t_{SCSV}	STB to chip select valid	10	30	50	ns	
t_{OLOH}	Input/output rise time	–	–	8	ns	from 0.8 V to 2 V
t_{OHOL}	Input/output fall time	–	–	8	ns	from 2 V to 0.8 V

[1] For test load definitions refer to figure 63.

Mode 4: Bus Controller Timing (8288 mode, figures 44, 45)

T_A = 0 to 70°C; V_{CC} = +5V ±10%

Timing Requirements

Symbol	Parameter	Limit values			Unit	Test condition
		min.	typ.	max.		
t_{CLCL}	CLK cycle period	100	–	–	ns	–
t_{CLCH}	CLK low time	50	–	–	ns	–
t_{CHCL}	CLK high time	30	–	–	ns	–
t_{SVCH}	Status active setup time	35	–	–	ns	–
t_{CHSV}	Status active hold time	10	–	–	ns	–
t_{SHCL}	Status inactive setup time	35	–	–	ns	–
t_{CLSH}	Status inactive hold time	10	–	–	ns	–
t_{OLOH}	Input rise time	–	–	20	ns	from 0.8V to 2V
t_{OHOL}	Input fall time	–	–	12	ns	from 0.8V to 2V

Timing Responses

Symbol	Parameter	Limit values			Unit	Test condition[1]
		min.	typ.	max.		
t_{CVNV}	Control active delay	5	30	45	ns	
t_{CVNX}	Control inactive delay	10	30	45	ns	
t_{CLLH} t_{CLMCH}	ALE, MCE active delay (from CLK)	–	20	35	ns	
t_{SVLH} t_{SVMCH}	ALE, MCE active delay (from status)	–	20	35	ns	$\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{INTA}$: TL1
t_{CHLL}	ALE inactive delay	4	20	35	ns	Other outputs: TL2
t_{CLML}	Command active delay	10	30	45	ns	
t_{CLMH}	Command inactive delay	10	25	40	ns	
t_{CHDTL}	Direction control active delay	–	–	50	ns	
t_{CHDTH}	Direction control inactive delay	–	–	40	ns	
t_{AELCH}	Command enable time	–	–	40	ns	
t_{AEHCZ}	Command disable time	–	–	40	ns	TL3
t_{AEVNV}	$\overline{AEN}$ to $\overline{DENOUT}$ time	–	–	20	ns	
t_{CEVNV}	CEN86 to $\overline{DENOUT}$ time	–	–	40	ns	$\overline{MRDC}$, $\overline{MWTC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{INTA}$: TL1
t_{CELRH}	CEN86 to command time	–	–	35	ns	
t_{AENSU}	$\overline{AEN}$ setup time	20	–	–	ns	Other outputs: TL2
t_{AENHO}	$\overline{AEN}$ hold time	0	–	–	ns	
t_{OLOH}	Input/output rise time	–	–	20	ns	from 0.8V to 2V
t_{OHOL}	Input/output fall time	–	–	12	ns	from 0.8V to 2V

[1] For test load definitions refer to figure 63.

Mode 4/5: Bus Controller Timing (82288 mode, figures 46–50)

T_A = 0 to 70°C; V_{CC} = +5 V ± 10%

Symbol	Parameter	Limit values			Unit	Test condition[3]
		min.	typ.	max.		
t_1	CLK period	62.5	–	250	ns	at 1.5 V
t_2	CLK high time	20	–	235	ns	at 3.6 V
t_3	CLK low time	15	–	230	ns	at 1.0 V
t_4	CLK fall time	–	–	10	ns	3.6 V to 1.0 V
t_5	CLK rise time	–	–	10	ns	1.0 V to 3.6 V
t_6	M/$\overline{IO}$ and status setup	22	–	–	ns	–
t_7	M/$\overline{IO}$ and status hold	1	–	–	ns	–
t_8	CENL setup time	20	–	–	ns	–
t_9	CENL hold time	1	–	–	ns	–
t_{10}	$\overline{READY}$ setup time	38	–	–	ns	–
t_{11}	$\overline{READY}$ hold time	25	–	–	ns	–
t_{12}	CMDLY setup time	20	–	–	ns	–
t_{13}	CMDLY hold time	1	–	–	ns	–
t_{14}	$\overline{AEN}$ setup time [1]	30	–	–	ns	–
t_{15}	$\overline{AEN}$ hold time [1]	1	–	–	ns	–
t_{16}	ALE, MCE active time	3	20	35	ns	TL2
t_{17}	ALE, MCE inactive time	–	20	40	ns	TL2
t_{18}	$\overline{DENOUT}$ write inactive from CENL	–	25	35	ns	TL2
t_{19}	DT/$\overline{ROUT}$ low from CLK	–	25	45	ns	TL2
t_{20}	$\overline{DENOUT}$ read active from DT/$\overline{ROUT}$	5	–	25	ns	TL2
t_{21}	$\overline{DENOUT}$ read inactive delay	3	–	40	ns	TL2
t_{22}	DT/$\overline{ROUT}$ high from $\overline{DENOUT}$ inactive	5	–	25	ns	TL2
t_{23}	$\overline{DENOUT}$ write active delay	–	25	40	ns	TL2
t_{24}	$\overline{DENOUT}$ write inactive delay	3	25	35	ns	TL2
t_{25}	$\overline{DENOUT}$ inactive from CEN	–	20	35	ns	TL2
t_{26}	$\overline{DENOUT}$ active from CEN	–	20	35	ns	TL2
t_{27}	DT/$\overline{ROUT}$ from CLK, CEN [2]	–	30	60	ns	TL2
t_{28}	$\overline{DENOUT}$ active from $\overline{AEN}$	–	–	35	ns	TL2

[1] $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold time is specified to guarantee the response shown in the waveforms.

[2] t_{27} only applies to bus cycles where MB = 0 is selected and $\overline{DENOUT}$ = 1, when the cycle is terminated (because CEN = 0).

[3] For test load definitions refer to figure 63.

Mode 4/5: Bus Controller Timing (82288 mode, cont'd, Figures 47–50)

Symbol	Parameter	Limit values			Unit	Test condition[1]
		min.	typ.	max.		
t_{29}	Command active delay	3	20	40	ns	TL1
t_{30}	Command inactive delay	3	20	35	ns	TL1
t_{31}	Command inactive from CEN	–	–	30	ns	TL1
t_{32}	Command active from CEN	–	–	30	ns	TL1
t_{33}	Command inactive enable from $\overline{AEN}$	–	20	40	ns	TL1
t_{34}	Command float time	–	–	40	ns	TL3
t_{35}	MB setup time	20	–	–	ns	–
t_{36}	MB hold time	0	–	–	ns	–
t_{37}	Command inactive enable from MB	–	–	40	ns	TL1
t_{38}	Command float time MB	–	–	40	ns	TL3
t_{39}	$\overline{DENOUT}$ active from MB	–	–	30	ns	TL1

[1] For test load definitions refer to figure 63.

Mode 5: Bus Arbiter Timing (Figures 52–60)

T_A = 0 to 70°C; V_{CC} = +5 V ±10%

Symbol	Parameter	Limit values			Unit	Test condition[1]
		min.	typ.	max.		
t_1	CLK cycle period	62.5	–	t_5 + 50	ns	at 1.5 V
t_2	CLK low time	15	–	230	ns	at 1.0 V
t_3	CLK high time	20	–	235	ns	at 3.6 V
t_4	CLK fall/rise time	–	–	10	ns	1.0 V to 3.6 V
t_5	$\overline{\text{BCLK}}$ cycle time	100	–	–	ns	–
t_6	$\overline{\text{BCLK}}$ high low time	30	–	–	ns	–
t_7	$\overline{\text{S0}}$, $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ setup time	22	–	–	ns	–
t_8	$\overline{\text{S0}}$, $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ hold time	1	–	–	ns	–
t_9	$\overline{\text{READY}}$ setup time	38	–	–	ns	–
t_{10}	$\overline{\text{READY}}$ hold time	25	–	–	ns	–
t_{11}	$\overline{\text{LOCK}}$, SYSB/$\overline{\text{RESB}}$ setup time	20	–	–	ns	–
t_{12}	$\overline{\text{LOCK}}$, SYSB/$\overline{\text{RESB}}$ hold time	1	–	–	ns	–
t_{13}	RESET setup time	20	–	–	ns	–
t_{14}	RESET hold time	1	–	–	ns	–
t_{15}	RESET active pulse width	16	–	–	CLK cycles	–
t_{16}	$\overline{\text{INIT}}$ setup time	45	–	–	ns	[2]
t_{17}	$\overline{\text{INIT}}$ hold time	1	–	–	ns	[2]
t_{18}	$\overline{\text{INIT}}$ active pulse width	$3(t_1) + 3(t_{14})$	–	–	ns	–
t_{19}	$\overline{\text{BUSY}}$, $\overline{\text{BPRN}}$, $\overline{\text{CBRQ}}$, $\overline{\text{CBQLCK}}$/$\overline{\text{ALWAYS}}$ setup to $\overline{\text{BCLK}}$ (or to RESET)	20	–	–	ns	–
t_{20}	$\overline{\text{BUSY}}$, $\overline{\text{BPRN}}$, $\overline{\text{CBRQ}}$, $\overline{\text{CBQLCK}}$/$\overline{\text{ALWAYS}}$ hold to $\overline{\text{BCLK}}$ (or to RESET)	1	–	–	ns	–
t_{21}	$\overline{\text{BCLK}}$ to $\overline{\text{BREQ}}$ delay	–	–	30	ns	TL2
t_{22}	$\overline{\text{BCLK}}$ to $\overline{\text{BPRO}}$ delay	–	–	35	ns	TL2
t_{23}	$\overline{\text{BPRN}}$ to $\overline{\text{BPRO}}$ delay	–	–	25	ns	TL2

[1] For test load definitions refer to figure 63.

[2] $\overline{\text{INIT}}$ is asynchronous to CLK and to $\overline{\text{BCLK}}$. However, for component testing purposes this specification is required to assure signal recognition at specific CLK and $\overline{\text{BCLK}}$ edges.

Mode 5: Bus Arbiter Timing (cont'd, figures 52–60)

Symbol	Parameter	Limit values			Unit	Test condition[1]
		min.	typ.	max.		
t_{24}	$\overline{\text{BCLK}}$ to $\overline{\text{BUSY}}$ active delay	1	–	60	ns	TL1
t_{25}	$\overline{\text{BCLK}}$ to $\overline{\text{BUSY}}$ float delay	–	–	35	ns	TL3
t_{26}	$\overline{\text{BCLK}}$ to $\overline{\text{CBRQ}}$ active delay	–	–	55	ns	TL2
t_{27}	$\overline{\text{BCLK}}$ to $\overline{\text{CBRQ}}$ float delay	–	–	35	ns	TL4
t_{28}	$\overline{\text{BCLK}}$ to $\overline{\text{AEN}}$ active delay	1	25	40	ns	TL1
t_{29}	CLK to $\overline{\text{AEN}}$ inactive delay	3	25	45	ns	TL1
t_{30}	CLK to $\overline{\text{LLOCK}}$ delay	–	20	40	ns	TL1
t_{31}	RESET to $\overline{\text{LLOCK}}$ delay	–	20	35	ns	TL1
t_{32}	CLK to $\overline{\text{BCLK}}$ setup time	38	–	–	ns	2)

1) For test load definitions refer to figure 63.

2) In actual use, CLK and $\overline{\text{BCLK}}$ are usually asynchronous to each other. However, for component testing purposes this specification is required to assure signal recognition at specific CLK and $\overline{\text{BCLK}}$ edges.

Figure 42
Mode 1, 2, 4 – Bus Transceiver Timing

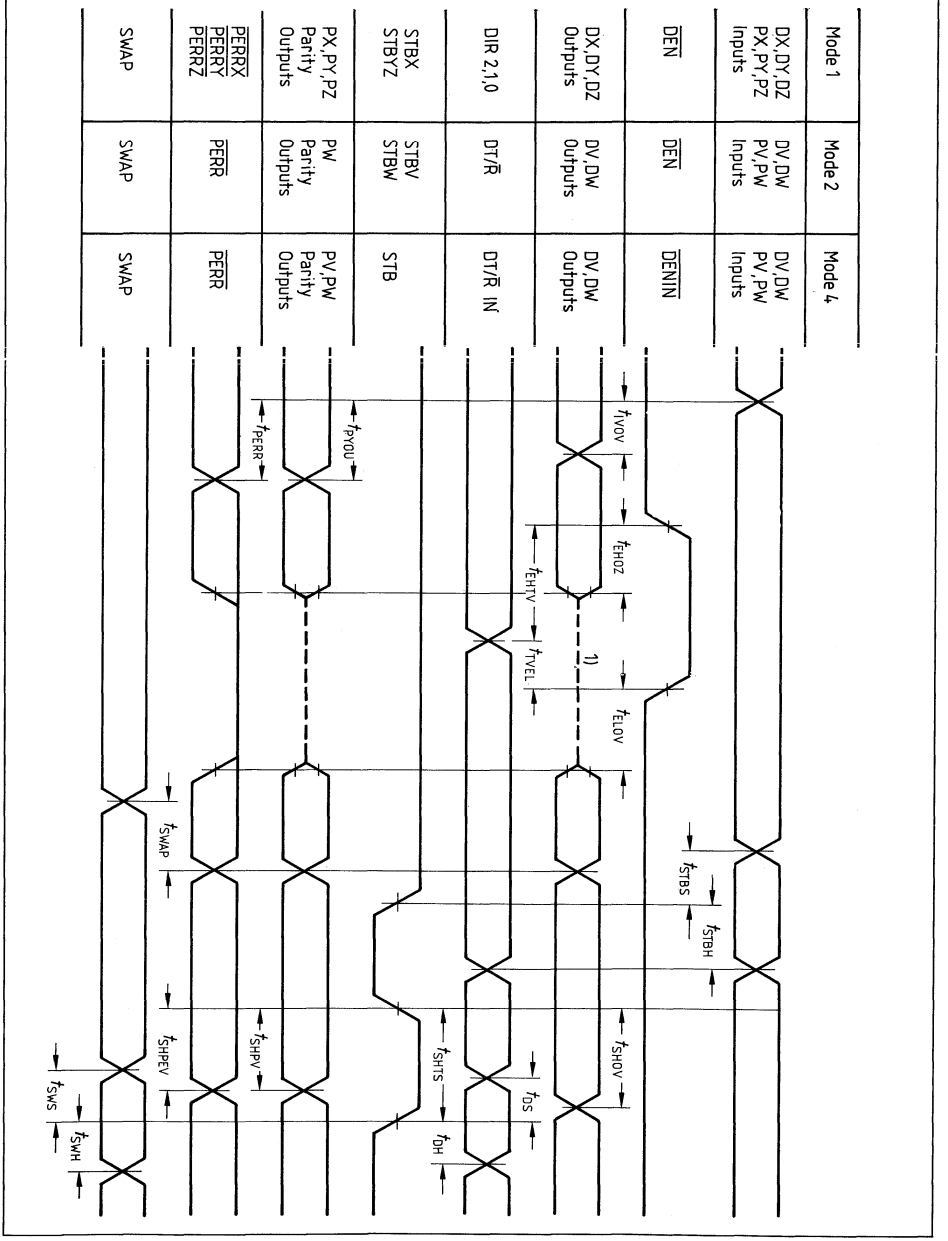


Figure 43
Mode 3 – Bus Transceiver Timing

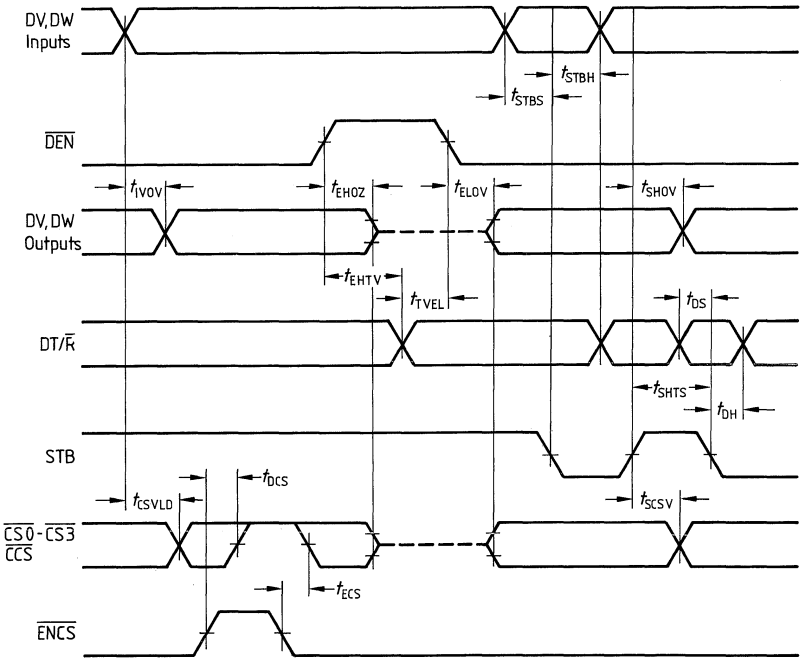
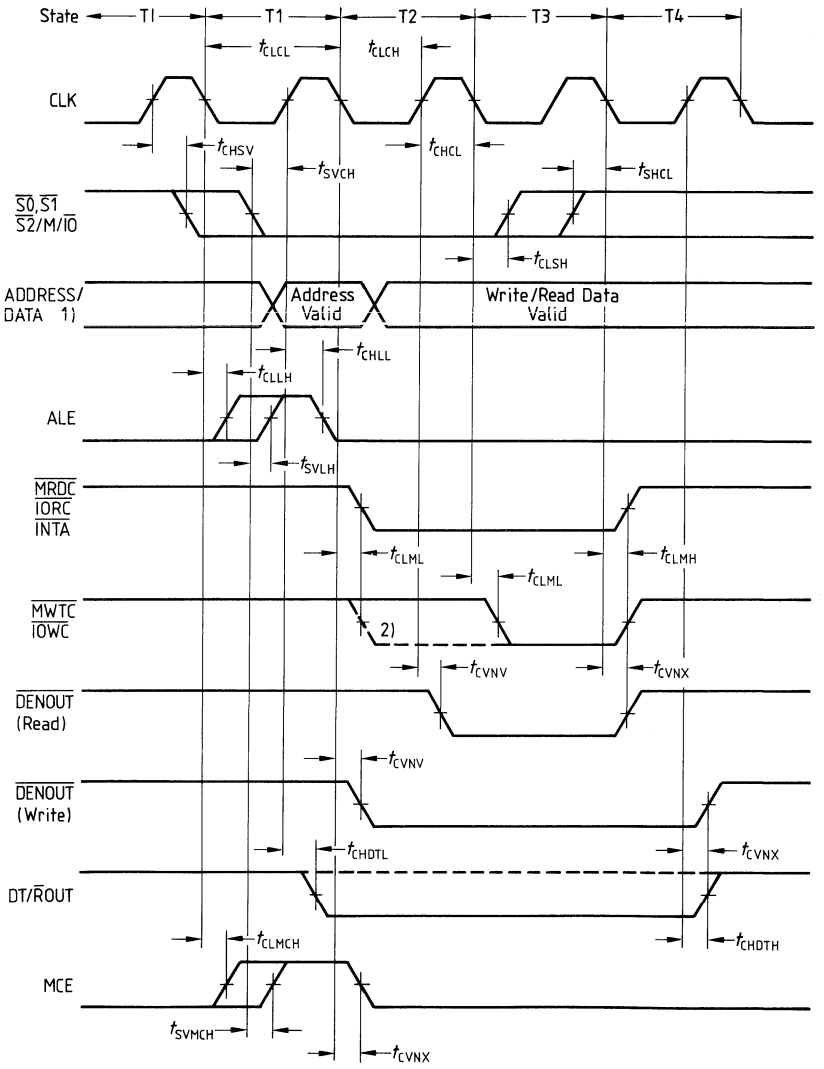


Figure 44
Mode 4 – Bus Controller Timing (8288)



1) Address/data bus is shown for reference purposes.
2) $\overline{MWTC}$ or $\overline{IOWC}$ is active during T2 if MB=low.

Figure 45
Mode 4 – Bus Controller Timing (8288)

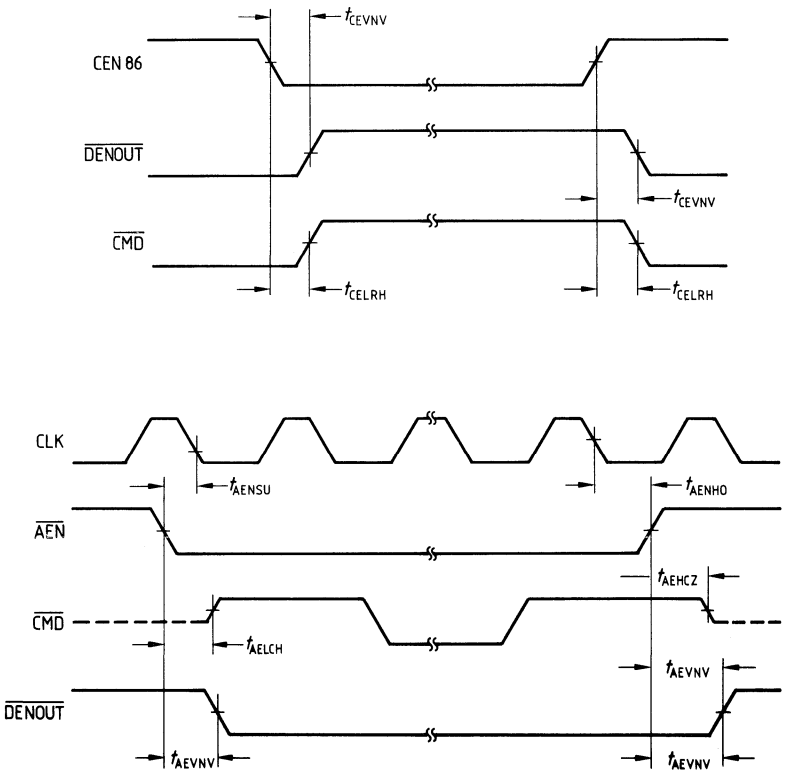
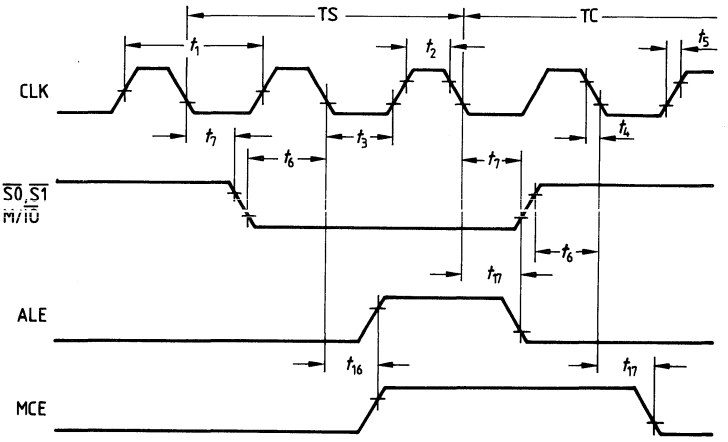
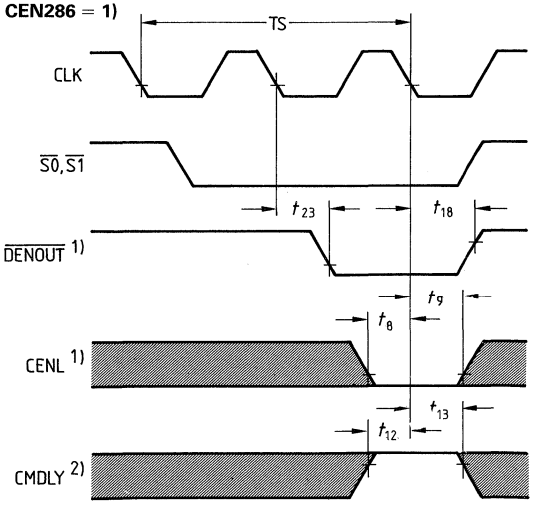


Figure 46
Mode 4/5 – Bus Controller Timing (82288)

CLK, Status, ALE, MCE Characteristics



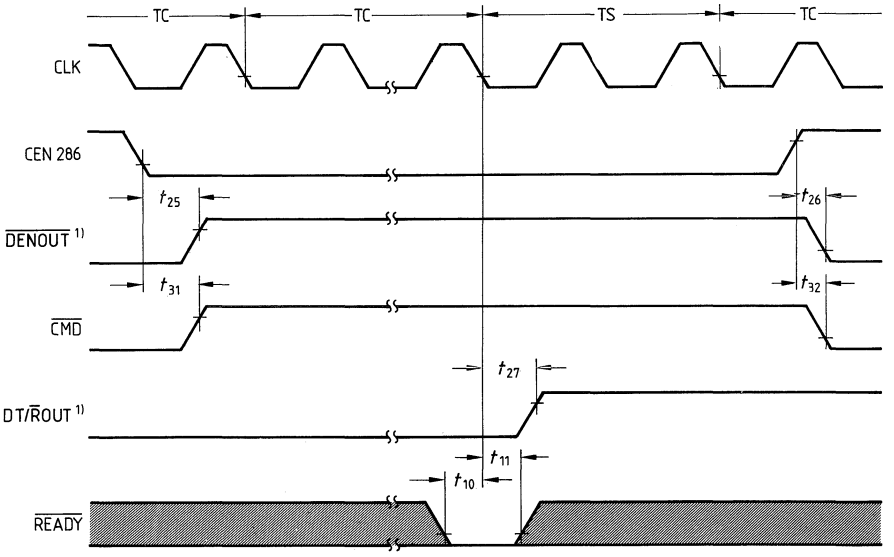
CENL, CMDLY, $\overline{DENOUT}$ Characteristics during Write Cycle
(Mode 4: MB = 0, CEN286 = 1)



1) Signal is not available in mode 5
2) In mode 5: MODE/CMDLY

Figure 47
Mode 4/5 – Bus Controller Timing (82288)

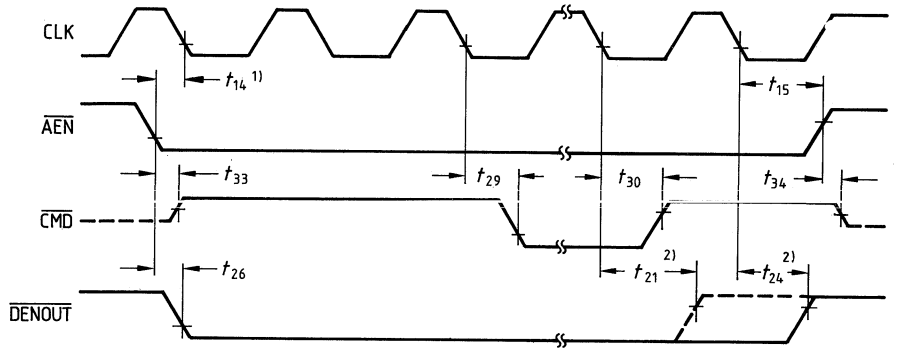
CEN Characteristics with MB=0
(only mode 4)



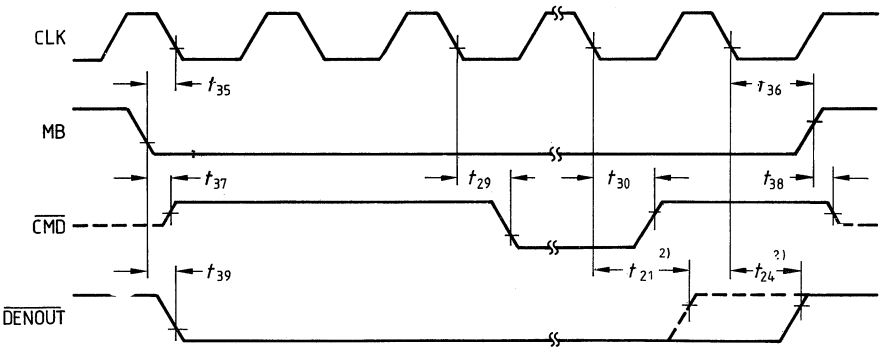
1) Signal is not available in Mode 5

Figure 48
Mode 4/5 – Bus Controller Timing (82288)

$\overline{AEN}$ Characteristics with MB=1
(only mode 4)



MB Characteristics with $\overline{AEN}$=1
(only mode 4)

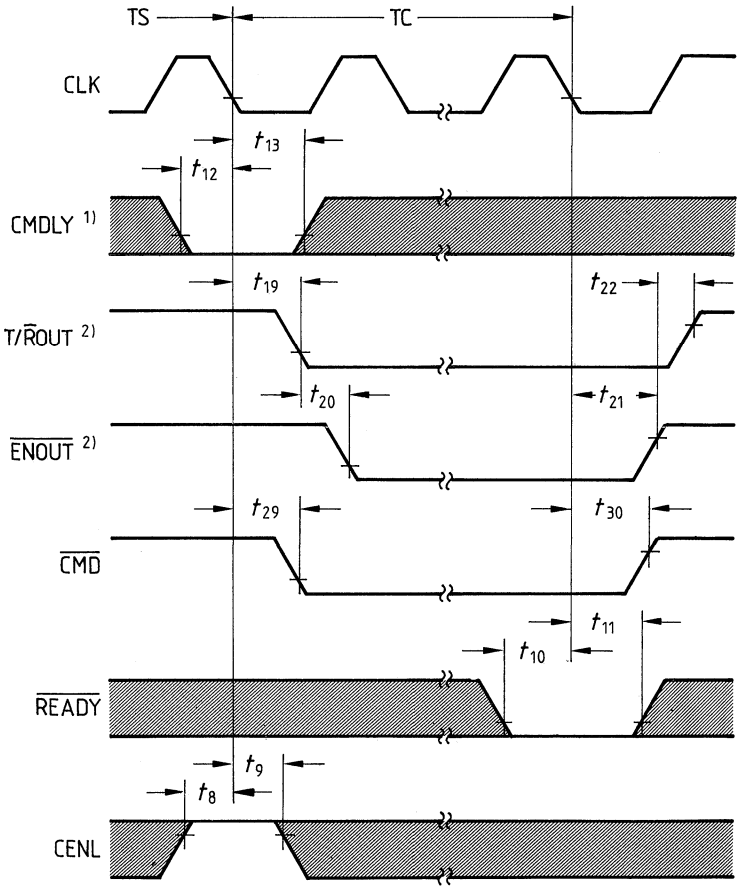


1) $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold time is specified to guarantee the response shown in the waveforms.

2) T21 applies to read bus cycles, T24 applies to write bus cycles.

Figure 49
Mode 4/5 – Bus Controller Timing (82288)

Read Cycle Characteristics
(mode 4: MB=0, CEN286=1)



1) In mode 5: MODE/CMDLY
2) Signal is not available in mode 5

Figure 50
Mode 4/5 – Bus Controller Timing (82288)

Write Cycle Characteristics
(only mode 4: MB=0, CEN286=1, DT/$\overline{R}$OUT=1)

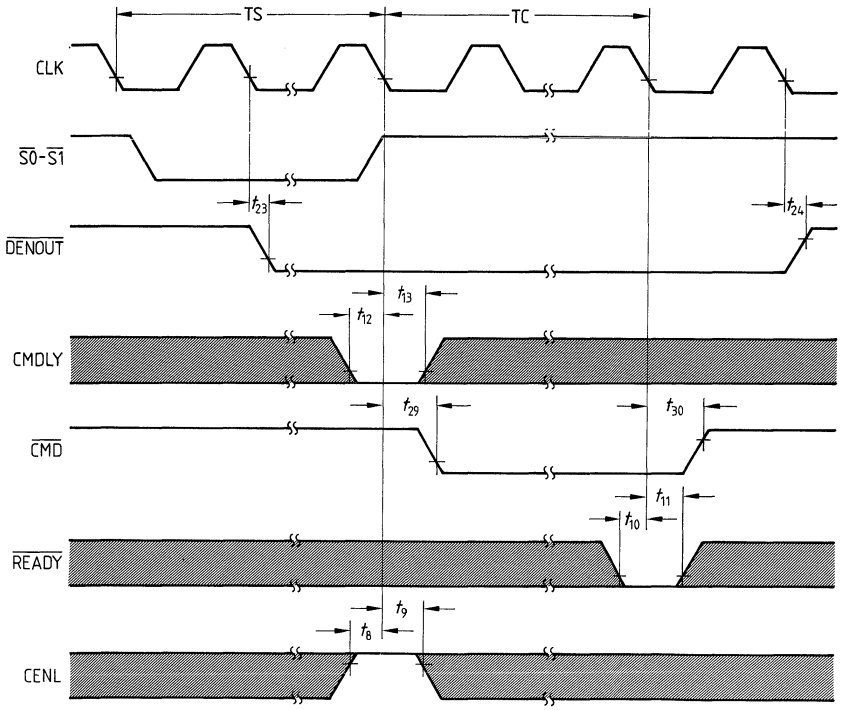


Figure 51
Mode 5 – Bus Transceiver Timing

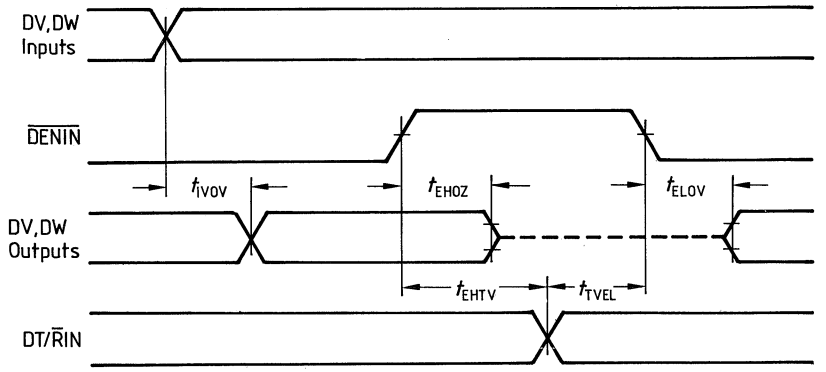
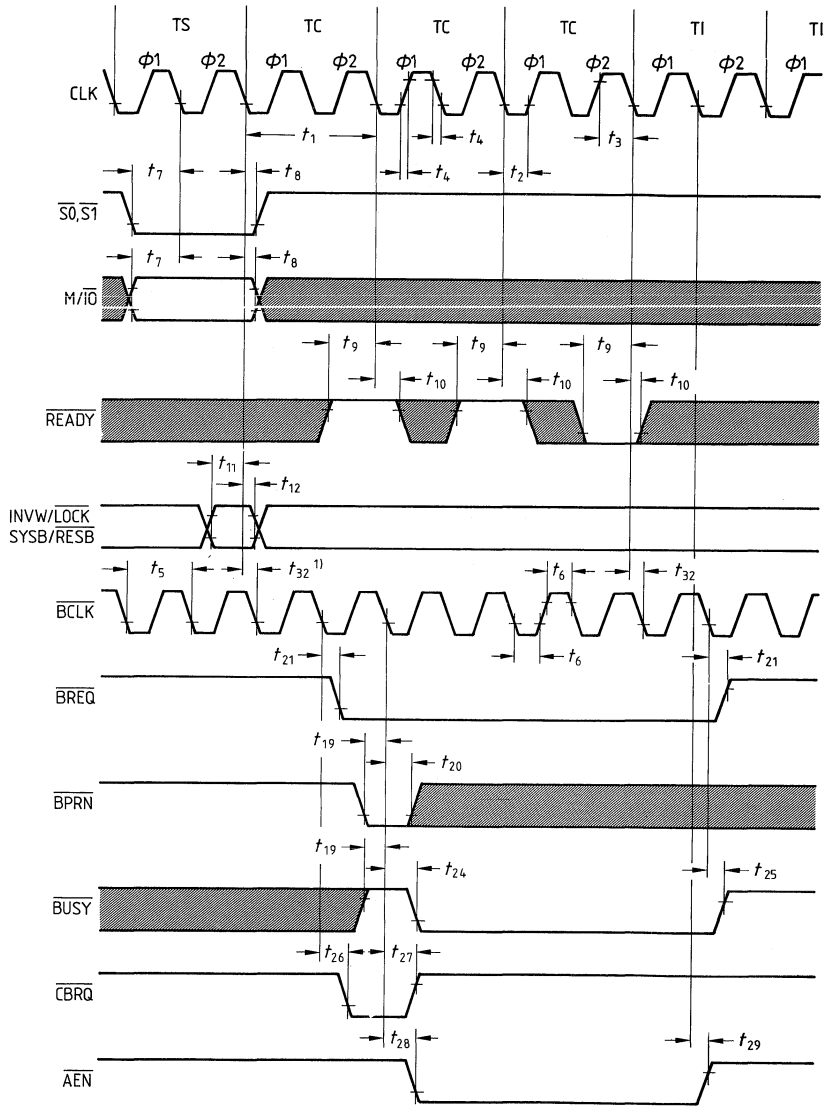
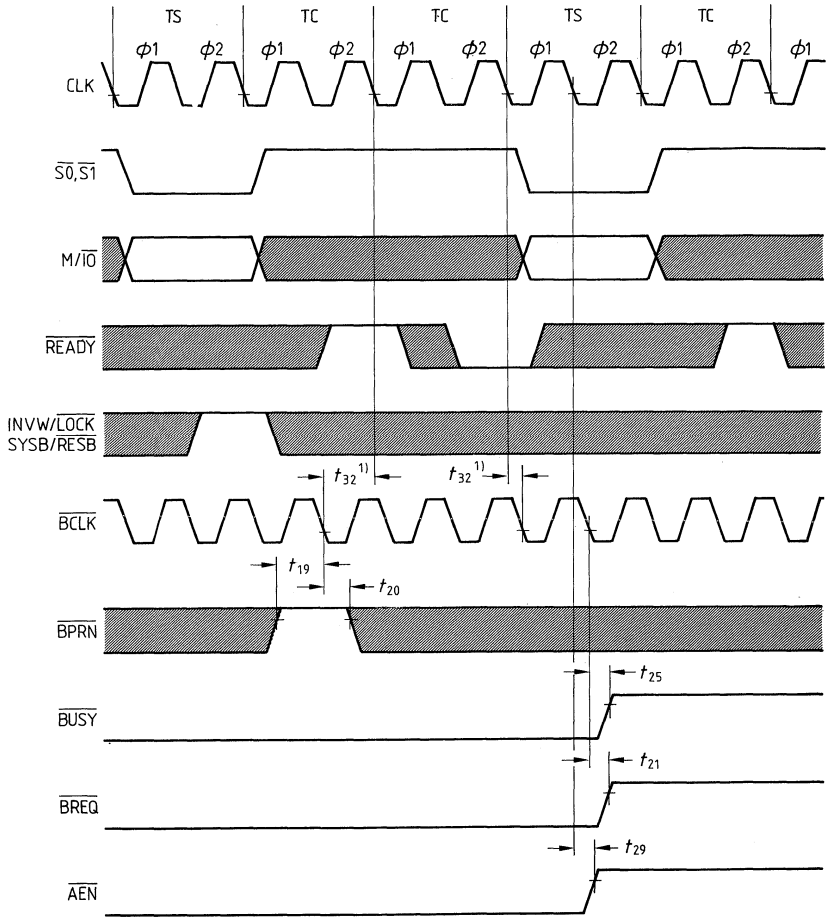


Figure 52
Mode 5 – Bus Arbiter Timing
Multibus Acquisition and Always-Release Operation



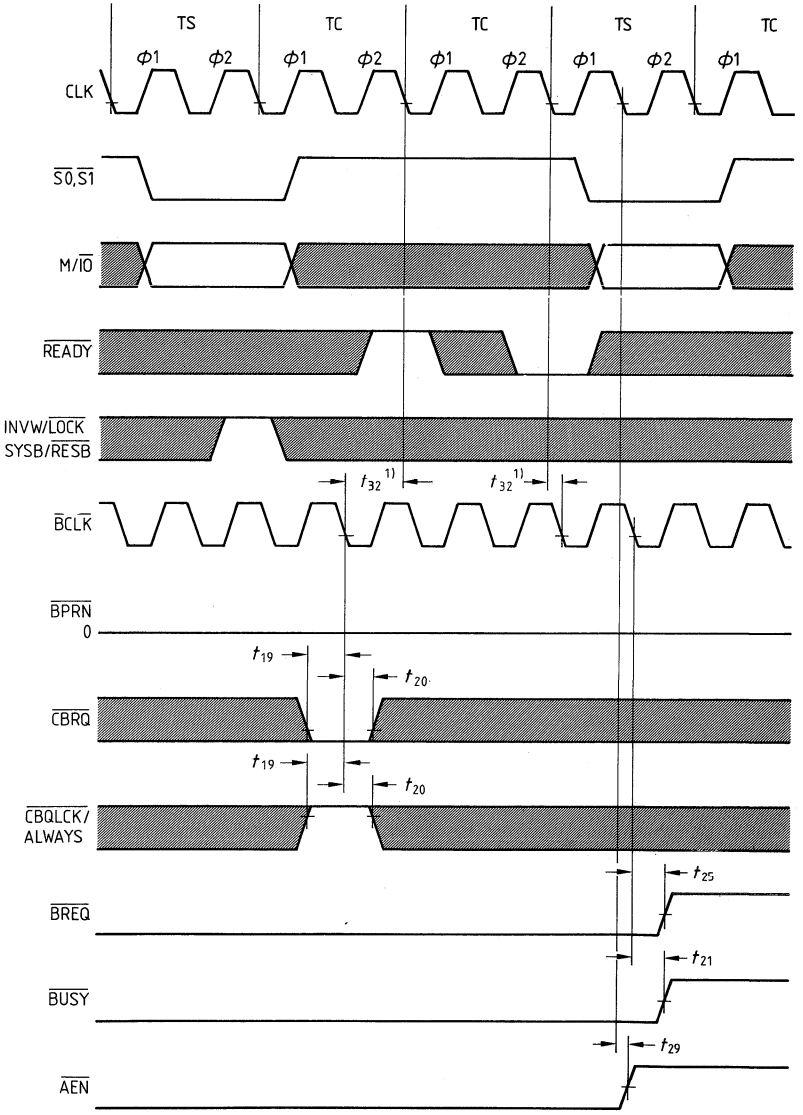
1) For SAB 82220 test purposes only

Figure 53
Mode 5 – Bus Arbiter Timing
Multibus Release due to $\overline{\text{BPRN}}$ inactive



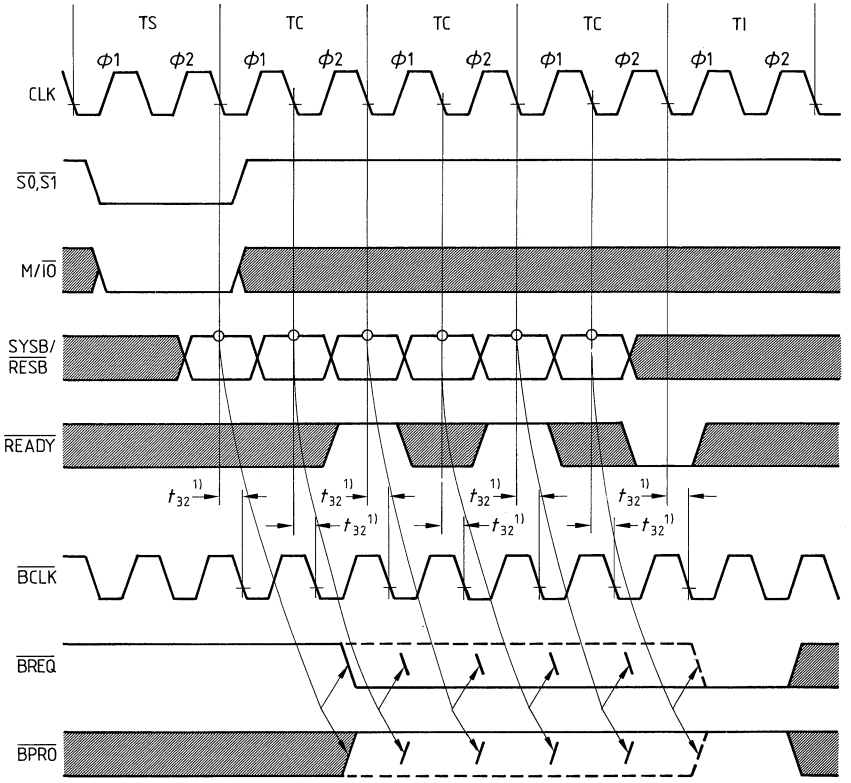
1) For SAB 82220 test purposes only

Figure 54
Mode 5 – Bus Arbiter Timing
Multibus Release due to $\overline{CBRQ}$ Active



1) For SAB 82220 test purposes only

Figure 55
Mode 5 – Bus Arbiter Timing
Multibus Acquisition during SAB 80286 INTA Cycles



1) For SAB 82220 test purposes only

Figure 56
Mode 5 – Bus Arbiter Timing
$\overline{BPRN}$ to $\overline{BPRO}$ Timing Relationship

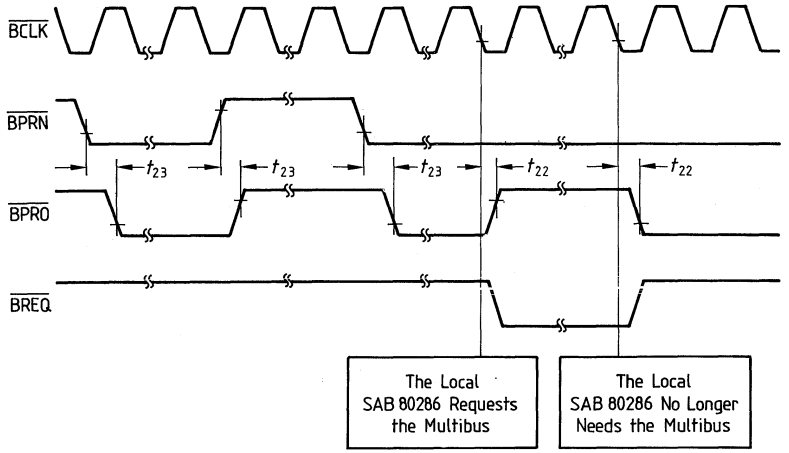


Figure 57
Mode 5 – Bus Arbiter Timing
SAB 80286 $\overline{LOCK}$ and SAB 82220 $\overline{LLOCK}$ Relationship

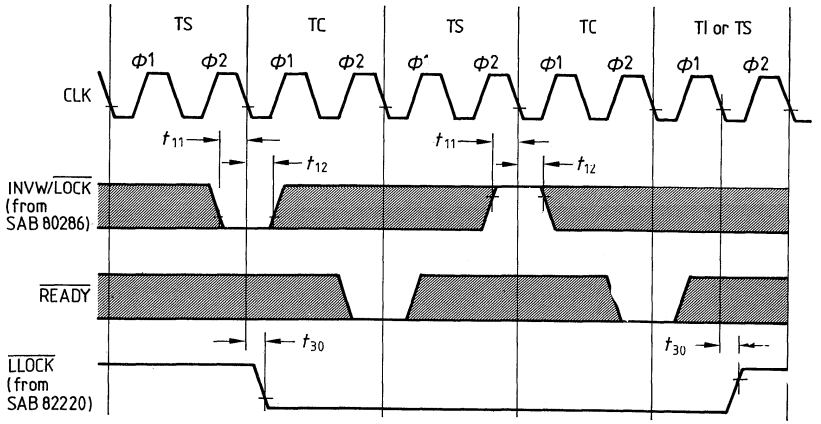
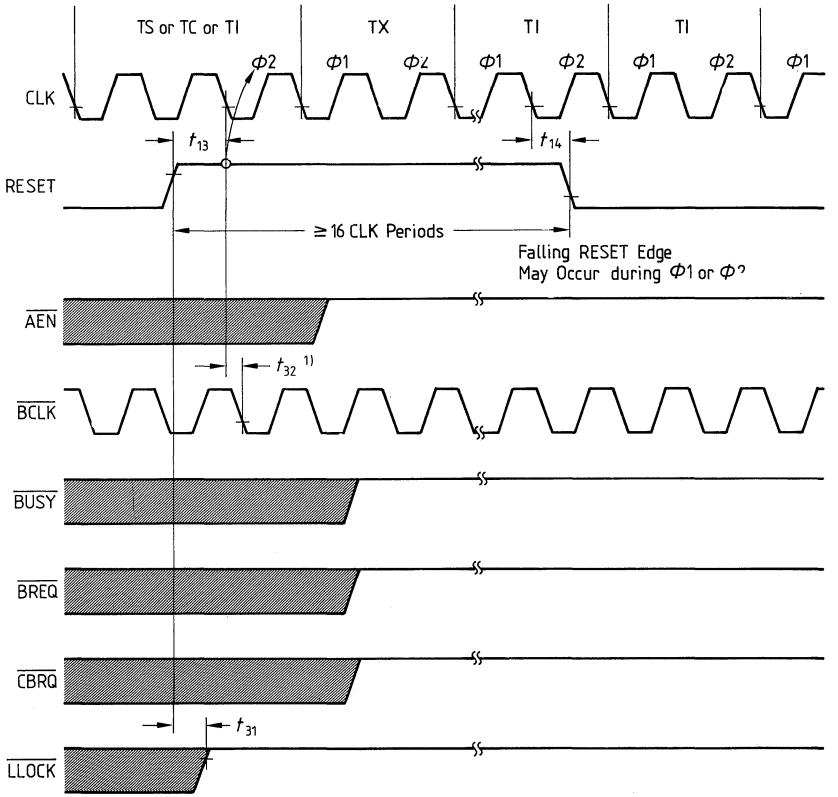
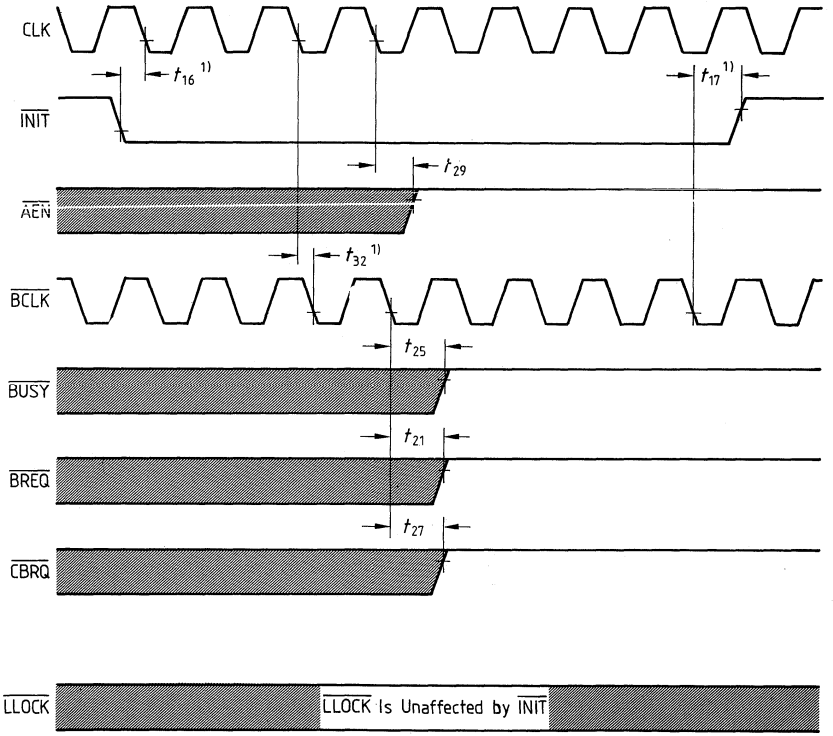


Figure 58
Mode 5 – Bus Arbiter Timing
RESET Active Pulse



1) For SAB 82220 test purposes only.

Figure 59
Mode 5 – Bus Arbiter Timing
$\overline{\text{INIT}}$ Active Pulse



1) For SAB 82220 test purposes only.

Figure 60
Mode 5 – Bus Arbiter Timing
Programming the Always-Release/Common-Bus-Request-Release Operation

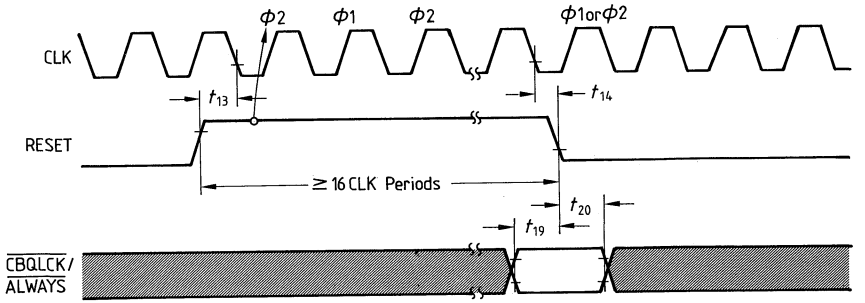


Figure 61
Mode 6 – Bus Transceiver Timing

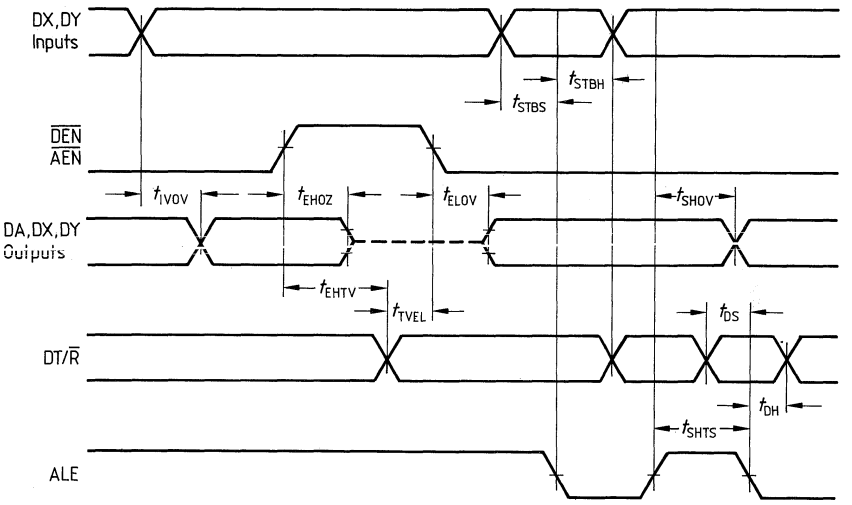


Figure 62
Input/Output Waveforms for AC Testing

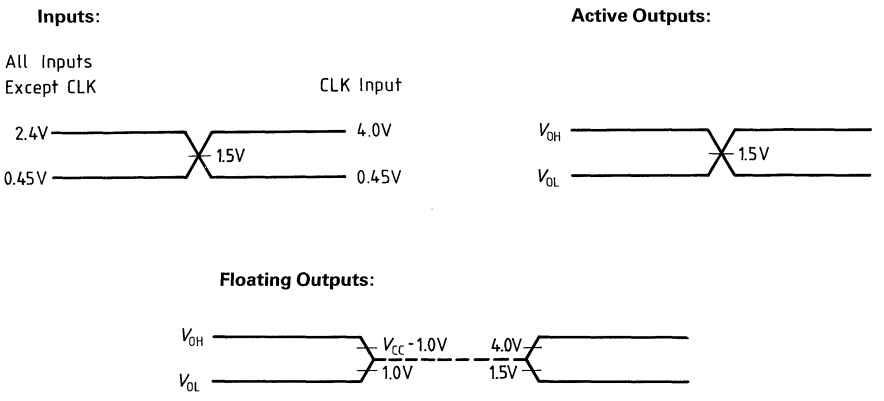
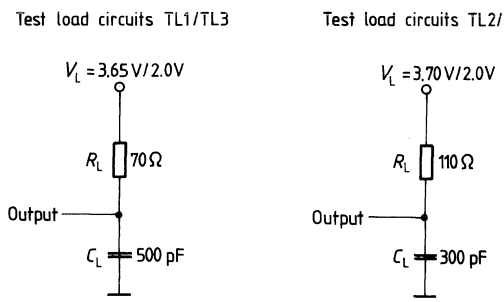


Figure 63
Output Test Load Circuits

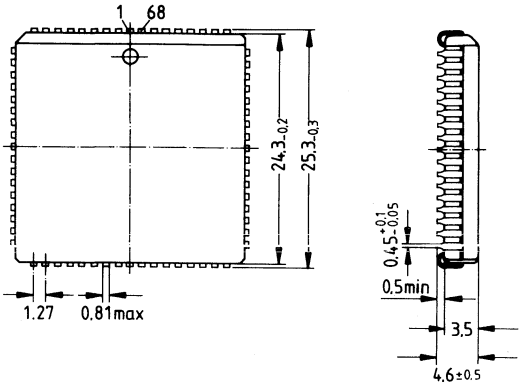


Test Condition Definition Table

R_L	C_L	V_L	Test Load	Remark
70 Ω	500 pF	3.65 V	TL 1	I_{OL}/I_{OH} = 48/−15 mA
110 Ω	300 pF	3.70 V	TL 2	I_{OL}/I_{OH} = 32/−10 mA
70 Ω	–	2.0 V	TL 3	Tristate
110 Ω	–	2.0 V	TL 4	Tristate

Package Outlines

Figure 64
Plastic Package, PLCC, 68 Pins



Dimensions in mm

Ordering Information

Type	Ordering Code	Function
SAB 82220-N	Q 67120-Y139	Bus interface controller

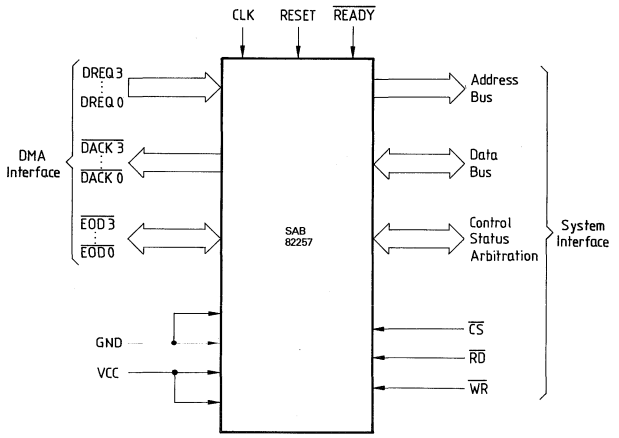
Preliminary

SAB 82257
High-Performance DMA Controller for 16-Bit Microcomputer Systems

SAB 82257 8 MHz
SAB 82257-6 6 MHz

- High-performance 16-bit DMA controller for the 16-bit family processors SAB 80286, SAB 80186/188, SAB 8086/88
- 4 independent high-speed DMA channels
- Adaptive on-chip bus interface for direct connection to processors
- Standalone operation for modular systems
- Programmable bus loading
- Transfer rates up to 8 Mbytes/s (8 MHz system)
- 16 Mbytes addressing range
- 16 Mbytes maximum block size
- Command chaining for automatic processing
- Automatic data chaining (scattering/gathering) for flexible data structures
- Single and double cycle transfers
- Automatic assembly/disassembly of data
- Memory-based communication scheme with CPU

Logic Symbol



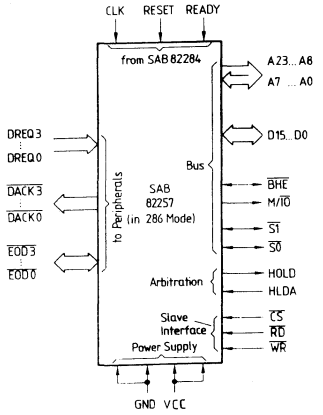
The SAB 82257 is a DMA (direct memory access) controller designed especially for the 16-bit microprocessors SAB 80286 and SAB 8086/186/88/188. In addition, the operation with other processors is supported by the remote mode. It has 4 independent DMA channels which can transfer data at rates up to 8 Mbytes/second at 8 MHz clock in an SAB 80286 system or up to 4 Mbytes/second at 8 MHz in an SAB 8086/80186 system. This great bandwidth allows the user to handle very fast data transfer or a large number of concurrent peripherals. The device is fabricated in advanced +5 V N-channel Siemens MYMOS technology and packaged in a 68-pin package.

Modes of Operation, Adaptive Bus Interface

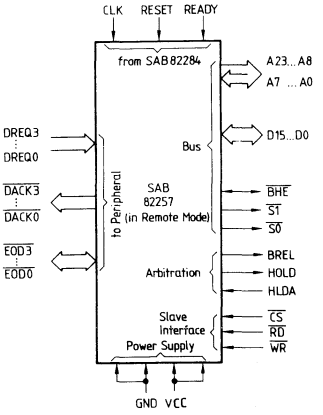
Like the advanced DMA controller SAB 82258, the SAB 82257 has been defined to work with all 16-bit processors, i.e. SAB 80286, SAB 80186/188 and SAB 8086/88 without additional support and interface logic. Hence the local buses of above processors are different in signals, functions and timings, the SAB 82257 has an adaptive bus interface to meet the different requirements of these local buses.

As a result of this, a bus compatibility with identical timing is attained with processors SAB 80286, SAB 80186 and SAB 8086. A compatibility with the 8-bit bus versions of these processors SAB 8088 and SAB 80188 is also guaranteed by defining the physical bus width of the SAB 82257 (per software) as 8 bits. The only difference in operation with SAB 8086 or SAB 80186 is that for SAB 8086 the HOLD pin functions as $\overline{RQ}/\overline{GT}$ line (if HLDA is held high on reset).

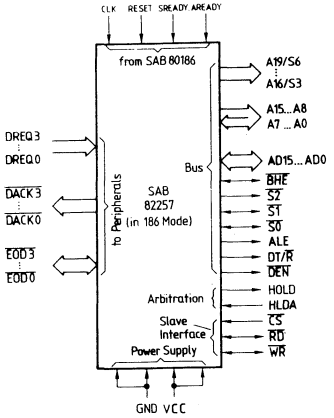
Logic Symbol in 286 Mode



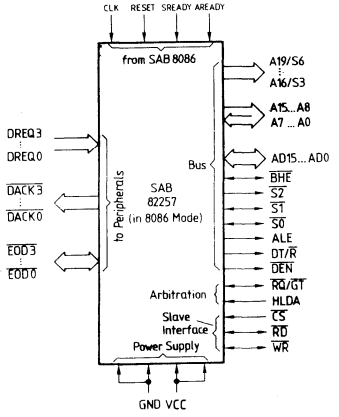
Logic Symbol in Remote Mode



Logic Symbol in 186 Mode



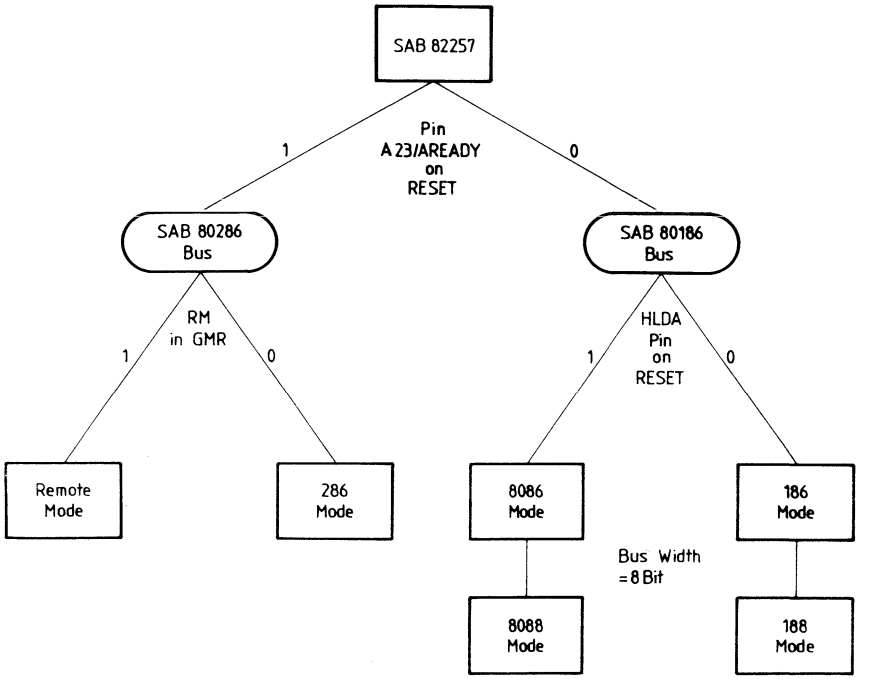
Logic Symbol in 8086 Mode



The SAB 82257 can also be operated in remote or standalone mode, in which case it is not coupled directly to a processor. In remote mode, the SAB 82257 can be operated as sole bus master in a multimaster environment.

The SAB 82257 is programmed to a specific mode of operation by applying defined logic levels to certain pins during reset and by setting the status of several control bits (see figure below).

Mode Selection



Pin Definitions and Functions

Some pins of the SAB 82257 serve for different purposes according to the different modes of bus operation. The table below summarizes the pinouts of the SAB 82257 in the various modes. A detailed description of the general pin functions as well as the mode-specific pin functions is given in the following sections.

Pin Names and Functions

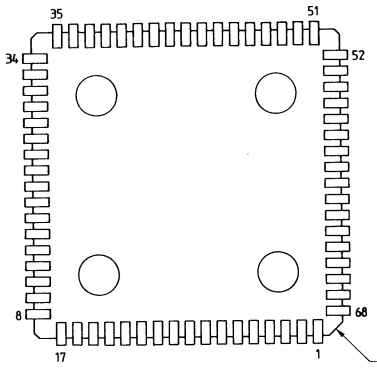
Pin	286 Mode		Remote Mode		186/8086 Mode	
	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)
16	HOLD	O	HOLD	O	HOLD or $\overline{RQ}/\overline{GT}$	O (186) I/O (8086)
17	HLDA	I	HLDA	I	HLDA	I
1	$\overline{BHE}$	I/O	$\overline{BHE}$	I/O	$\overline{BHE}$	I/O
14	M/$\overline{IO}$	O	BREL	O	$\overline{S2}$	O
11	$\overline{S1}$	I/O	$\overline{S1}$	O	$\overline{S1}$	I/O
13	$\overline{S0}$	I/O	$\overline{S0}$	O	$\overline{S0}$	I/O
8	$\overline{CS}$	I	$\overline{CS}$	I	$\overline{CS}$	I
2	$\overline{RD}$	I	$\overline{RD}$	I	$\overline{RD}$	I/O
3	$\overline{WR}$	I	$\overline{WR}$	I	$\overline{WR}$	I/O
10	$\overline{READY}$	I	$\overline{READY}$	I	SREADY	I
59	A23	O	A23	O	AREADY	I
58	A22	O	A22	O	ALE	O
57	A21	O	A21	O	DT/$\overline{R}$	O
56	A20	O	A20	O	$\overline{DEN}$	O
55	A19	O	A19	O	A19/S6	O
54	A18	O	A18	O	A18/S5	O
53	A17	O	A17	O	A17/S4	O
52	A16	O	A16	O	A16/S3	O
51	A15	O	A15	O	A15	O
50	A14	O	A14	O	A14	O
49	A13	O	A13	O	A13	O
48	A12	O	A12	O	A12	O
47	A11	O	A11	O	A11	O
46	A10	O	A10	O	A10	O
45	A9	O	A9	O	A9	O
44	A8	O	A8	O	A8	O
42	A7	I/O	A7	I/O	A7	I/O
41	A6	I/O	A6	I/O	A6	I/O
40	A5	I/O	A5	I/O	A5	I/O
39	A4	I/O	A4	I/O	A4	I/O
38	A3	I/O	A3	I/O	A3	I/O
37	A2	I/O	A2	I/O	A2	I/O
36	A1	I/O	A1	I/O	A1	I/O
35	A0	I/O	A0	I/O	A0	I/O

Pin Names and Functions (cont'd)

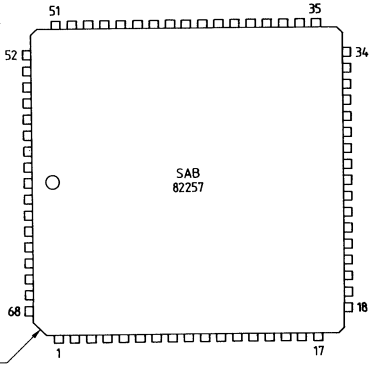
Pin	286 Mode		Remote Mode		186/8086 Mode	
	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)
18	D15	I/O	D15	I/O	AD15	I/O
20	D14	I/O	D14	I/O	AD14	I/O
22	D13	I/O	D13	I/O	AD13	I/O
24	D12	I/O	D12	I/O	AD12	I/O
27	D11	I/O	D11	I/O	AD11	I/O
29	D10	I/O	D10	I/O	AD10	I/O
31	D9	I/O	D9	I/O	AD9	I/O
33	D8	I/O	D8	I/O	AD8	I/O
19	D7	I/O	D7	I/O	AD7	I/O
21	D6	I/O	D6	I/O	AD6	I/O
23	D5	I/O	D5	I/O	AD5	I/O
25	D4	I/O	D4	I/O	AD4	I/O
28	D3	I/O	D3	I/O	AD3	I/O
30	D2	I/O	D2	I/O	AD2	I/O
32	D1	I/O	D1	I/O	AD1	I/O
34	D0	I/O	D0	I/O	AD0	I/O
7	DREQ0	I	DREQ0	I	DREQ0	I
6	DREQ1	I	DREQ1	I	DREQ1	I
5	DREQ2	I	DREQ2	I	DREQ2	I
4	DREQ3	I	DREQ3	I	DREQ3	I
61	$\overline{\text{DACK0}}$	O	$\overline{\text{DACK0}}$	O	$\overline{\text{DACK0}}$	O
62	$\overline{\text{DACK1}}$	O	$\overline{\text{DACK1}}$	O	$\overline{\text{DACK1}}$	O
63	$\overline{\text{DACK2}}$	O	$\overline{\text{DACK2}}$	O	$\overline{\text{DACK2}}$	O
64	$\overline{\text{DACK3}}$	O	$\overline{\text{DACK3}}$	O	$\overline{\text{DACK3}}$	O
65	$\overline{\text{EOD0}}$	I/O	$\overline{\text{EOD0}}$	I/O	$\overline{\text{EOD0}}$	I/O
66	$\overline{\text{EOD1}}$	I/O	$\overline{\text{EOD1}}$	I/O	$\overline{\text{EOD1}}$	I/O
67	$\overline{\text{EOD2}}$	I/O	$\overline{\text{EOD2}}$	I/O	$\overline{\text{EOD2}}$	I/O
68	$\overline{\text{EOD3}}$	I/O	$\overline{\text{EOD3}}$	I/O	$\overline{\text{EOD3}}$	I/O
15	RESET	I	RESET	I	RESET	I
12	CLK	I	CLK	I	CLK	I
9,43	GND	(Ground)	GND	(Ground)	GND	(Ground)
26,60	VCC	(Power Supply)	VCC	(Power Supply)	VCC	(Power Supply)

Pin Configuration

PLCC 68
Bottom view



PLCC 68
Top view



Pin Definitions for All Operating Modes

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{BHE}$</td><td>1</td><td>I/O</td><td>$\overline{BUS\ HIGH\ ENABLE}$
Indicates transfer of data on the upper byte of the data bus, D15 to D8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is active low and floats to tristate off when the SAB 82257 does not own the bus.
$\overline{BHE}$ and A0 encodings
<table>
<tr><th>$\overline{BHE}$</th><th>A0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Word transfer (D15–D0)</td></tr>
<tr><td>0</td><td>1</td><td>Byte transfer on upper half of data bus (D15–D8)</td></tr>
<tr><td>1</td><td>0</td><td>Byte transfer on lower half of data bus (D7–D0)</td></tr>
<tr><td>1</td><td>1</td><td>Odd-addressed byte on 8-bit bus (D7–D0)</td></tr>
</table></td></tr>
<tr><td>$\overline{RD}$</td><td>2</td><td>I</td><td>$\overline{READ}$
This command in conjunction with chip select enables reading out of the SAB 82257 register which is addressed by the address lines A7 to A0. This signal can be asynchronous to the SAB 82257 clock.</td></tr>
<tr><td>$\overline{WR}$</td><td>3</td><td>I</td><td>$\overline{WRITE}$
This command is used for writing into SAB 82257 registers. This signal can be asynchronous to the SAB 82257 clock.</td></tr>
<tr><td>DREQ0-
DREQ3</td><td>4-7</td><td>I</td><td>DMA REQUEST (0 TO 3)
These input signals are used for synchronized DMA transfers. These signals can be asynchronous to the SAB 82257 clock.</td></tr>
<tr><td>$\overline{CS}$</td><td>8</td><td>I</td><td>$\overline{CHIP\ SELECT}$
Is used to enable the access of a processor to SAB 82257 registers. This access is additionally controlled either by bus status signals or by the read or write command signals. Chip select can be asynchronous to the SAB 82257 clock.</td></tr>
<tr><td>CLK</td><td>12</td><td>I</td><td>CLOCK
It provides the fundamental timing. In 286 mode and remote mode it must be two times the system clock.
It can be directly connected to the SAB 82284 CLK output. It is divided by two to generate the SAB 82257 internal clock. The on-chip divide-by-two circuitry can be synchronized to the external clock generator by a low-to-high transition on the RESET input, or by first high-to-low transition on the status inputs $\overline{S0}$ or $\overline{S1}$ after reset. In 186/8086 mode no internal prescaling is done.</td></tr>
</table>

Pin Definitions for All Operating Modes (cont'd)

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{S0}$, $\overline{S1}$</td><td>11, 13</td><td>I/O</td><td>BUS STATUS LINES (0, 1)
These signals control the support circuits. The beginning of a bus cycle is indicated by $\overline{S1}$ or $\overline{S0}$ or both going active. The termination of a bus cycle is indicated by all status signals going inactive in 186 mode or bus ready signal ($\overline{READY}$) going active in 286 mode. The type of bus cycle is indicated by $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ (in 186 mode) or M/$\overline{IO}$ (in 286 mode). $\overline{S2}$ and M/$\overline{IO}$ have the same meaning but in 186 mode the $\overline{S2}$ signal can be active only when at least one of $\overline{S1}$ or $\overline{S0}$ is active, whereas in 286 mode the M/$\overline{IO}$ signal is valid with the address on the address lines. The SAB 82257 can generate the following bus cycles by activating the status signals (and M/$\overline{IO}$ in 286 mode):
<table>
<tr><th>M/$\overline{IO}$ or $\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Cycle Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Read I/O-vector (for multiplexer channel)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read from I/O space</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write into I/O space</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>No bus cycle, does not occur in 186 mode</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Does not occur</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read from memory space</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write into memory space</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>No bus cycle</td></tr>
</table>
When the SAB 82257 is not the master of the local bus the status signals are used as inputs for detection of synchronous accesses to the SAB 82257. The following table shows the bus status and $\overline{CS}$, signals and their interpretation by the SAB 82257.
<table>
<tr><th>$\overline{CS}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Description</th></tr>
<tr><td>1</td><td>X</td><td>X</td><td>SAB 82257 is not selected (no action)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No SAB 82257 access (no action)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read from an SAB 82257 register</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write into an SAB 82257 register</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>No bus cycle (note 1)</td></tr>
</table>
Note 1: SAB 82257 is selected but no synchronous access is activated. In this case the SAB 82257 monitors $\overline{RD}$ and $\overline{WR}$ signals for detection of an asynchronous access.</td></tr>
<tr><td>RESET</td><td>15</td><td>I</td><td>SYSTEM RESET
An activation of the reset signal forces the SAB 82257 to the initial state. The reset signal must be synchronous to CLK.</td></tr>
</table>

Pin Definitions for All Operating Modes (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{DACK0}$- $\overline{DACK3}$	61–64	O	$\overline{DMA\ ACKNOWLEDGE}$ (0 TO 3) Acknowledges the requests on the related DREQn signal. It is activated when the requested transfer(s) is (are) performed.
$\overline{EOD0}$- $\overline{EOD3}$	65–68	I/O	$\overline{END\ OF\ DMA}$ (0 TO 3) These signals are implemented as open drain output drivers with a high impedance pullup resistor and thus can be used as bidirectional lines. As **outputs** the signals are activated for two system clock cycles at the end of the DMA transfer of the corresponding channel (if enabled) or they are activated under program control (EOD output or interrupt output). If the signals are held internally high but forced to low by external circuitry, they act as "End of DMA" **inputs**. The current transfer is aborted and the SAB 82257 continues with the next command. Additionally, a special function is possible with the $\overline{EOD2}$ pin: this pin can also be used as common interrupt signal for all 4 channels. In this mode this signal is not an open drain output but a pushpull output (output only). The other $\overline{EOD}$ pins may be used as $\overline{EOD}$ outputs/inputs as described above.
VCC	26,60		POWER SUPPLY (+5 V)
GND	9,43		GROUND (0 V)

Pin Definitions for 286 Mode and Remote Mode

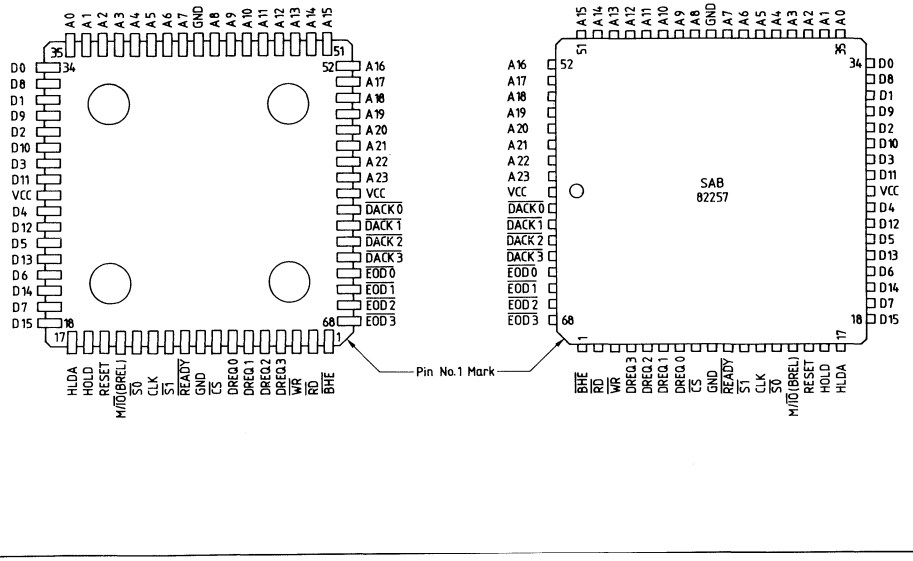
In 286 mode the SAB 82257 bus signals and bus timings are the same as for the SAB 80286 processor. Additional features of the SAB 82257 require a slight change in pin definitions. The processor can access internal registers of the SAB 82257. Therefore the bus signals must support these accesses. This means that some of the bus control signals must be bidirectional and some additional bus control signals are necessary. All additional pins and their functions are listed below.

In **remote mode** most of the bus signals are the same as in 286 mode. Pin 14 (M/$\overline{IO}$) serves as BREL output. The HOLD/HLDA arbitration in remote mode is used only for system bus accesses, the resident bus is accessed directly.
The $\overline{CS}$ input additionally requests access to the local bus of the SAB 82257. These accesses are enabled through the BREL output after the SAB 82257 has released the bus.

Pin Configuration in 286 Mode and Remote Mode

Component Pad View – As viewed from underside of component when mounted on the board

PC Board View – As viewed from the component side of the pc board



Pin Definitions for 286 Mode and Remote Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{READY}}$	10	I	$\overline{\text{BUS READY}}$ Terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{\text{READY}}$ low. $\overline{\text{READY}}$ is an active low synchronous input requiring setup and hold times relative to the system clock to be met for correct operation.
M/$\overline{\text{IO}}$	14 (286 mode)	O	MEMORY/ $\overline{\text{I/O}}$ SELECT In 286 mode, pin 14 is used to distinguish between memory and I/O space addresses.
BREL	14 (remote mode)	O	BUS RELEASE In remote mode pin 14 is used to indicate when the SAB 82257 has released the control of the local bus.
HOLD	16	O	BUS HOLD REQUEST When true, indicates a request for control of the local bus (286 mode) or the system bus (remote mode). When the SAB 82257 relinquishes the bus it drops the HOLD output. HOLD is connected to the bus arbiter in remote mode.
HLDA	17	I	BUS HOLD ACKNOWLEDGE When true, indicates that the SAB 82257 can acquire the control of the bus. When it goes low SAB 82257 must relinquish the bus at the end of its current cycle. HLDA can be asynchronous to the SAB 82257 clock. HLDA is connected to the bus arbiter in remote mode.
D0-D15	18-25, 27-34	I/O	DATA BUS (0 TO 15) This is the bidirectional 16-bit data bus. For use with an 8-bit bus, only the lower 8 data lines D7-D0 are relevant.
A0-A7	35-42	I/O	ADDRESS BUS (0 TO 7) The lower 8 address lines for DMA transfers. They are also used to input the register address when the processor accesses an SAB 82257 register.
A8-A23	44-59	O	ADDRESS BUS (8 TO 23) Higher address outputs.

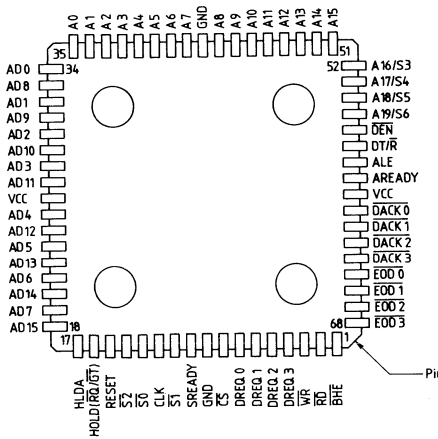
Pin Definitions for 186 Mode and 8086 Mode

In 186 mode and 8086 mode the SAB 82257 multiplexes the address with data and additional status lines.
Pins A0 to A15 retain their original function while pins A20 to A23 serve for different purposes (not used for address in 186/8086 mode).

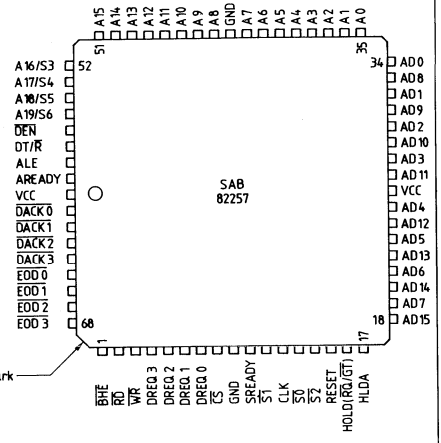
The $\overline{RD}$ and $\overline{WR}$ lines are additionally used as outputs in 186/8086 mode to support minimum mode systems.
Note that the HLDA input can be used to force the SAB 82257 off the bus in 8086 mode, even though the arbitration is done via the $\overline{RQ}/\overline{GT}$ line!

Pin Configuration in 186 Mode and 8086 Mode

Component Pad View – As viewed from underside of component when mounted on the board



PC Board View – As viewed from the component side of the pc board



Pin Definitions for 186 Mode and 8086 Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
ALE	58	O	ADDRESS LATCH ENABLE This signal provides a strobe to separate the address information on the multiplexed AD lines.
$\overline{DEN}$	56	O	$\overline{DATA\ ENABLE}$ This signal is used for enabling the data transceiver.
DT/$\overline{R}$	57	O	DATA TRANSMIT/$\overline{RECEIVE}$ This signal controls the direction of the data transceivers. When low, data is transferred to the SAB 82257, when high the SAB 82257 places data onto the data bus.
$\overline{S2}$	14	O	$\overline{STATUS\ LINE\ 2}$ Signal as for SAB 186/8086/88 processors (see also $\overline{S1}$, $\overline{S0}$ description in 286 mode).
AREADY	59	I	ASYNCHRONOUS READY The rising edge of this signal is internally synchronized, the falling edge must be synchronous to CLK. During reset this signal must be low for entering the 186 mode.
SREADY	10	I	SYNCHRONOUS READY This signal must be synchronized externally. The use of this pin permits a relaxed system-timing specification by eliminating the clock phase which is required for resolving the signal level when using the AREADY input.
CLK	12	I	SYSTEM CLOCK This is the input for the one time system clock. No internal prescaling is done.
AD0–AD15	18–25 27–34	I/O	ADDRESS/DATA BUS (0 TO 15) Lower address and data information is multiplexed on pin AD0 to AD 15. Additionally the demultiplexed address information is available on address pin A0 to A15.
A0–A7 A8–A15	35–42 44–51	I/O O	
A16/S3–A19/S6	52, 55	O	ADDRESS BUS (16 TO 19) / STATUS LINES (3 TO 6) The higher address bits are multiplexed with additional status information.
HLDA	17	I	BUS HOLD ACKNOWLEDGE When true, indicates that the SAB 82257 can acquire the control of the bus. When it goes low the SAB 82257 must relinquish the bus at the end of its current bus cycle. HLDA can be asynchronous to the SAB 82257 clock. In 8086 mode, HLDA can be used to force the SAB 82257 off the bus.
HOLD	16 (186 mode)	O	BUS HOLD REQUEST When true, indicates a request for control of the bus. When the SAB 82257 relinquishes the bus, it drops the HOLD output.
$\overline{RG}$/$\overline{GT}$	16	I/O	$\overline{REQUEST}$/$\overline{GRANT}$ In 8086 mode the HOLD output acts as $\overline{REQUEST}$/$\overline{GRANT}$ line. The $\overline{REQUEST}$/$\overline{GRANT}$ protocol implements a one-line communication dialog required to arbitrate the use of the system bus normally done via HOLD/HLDA. The $\overline{RG}$/$\overline{GT}$ signal is active low and has an internal pullup resistor.

Functional Description

General

The SAB 82257 is an advanced general-purpose DMA controller especially tailored for efficient high-speed data transfers on an SAB 80286 as well as on an SAB 80186/188 or SAB 8086/88 bus.
It supports two basic operating modes:

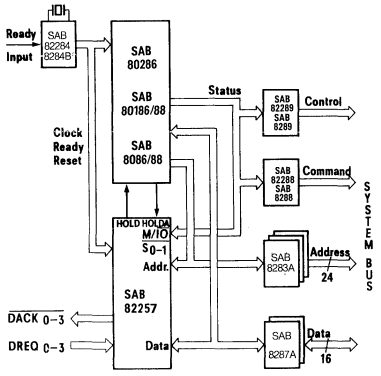
– local mode (tightly coupled to a processor) and
– remote mode (loosely coupled to a processor).

In the first case the SAB 82257 is directly coupled to the CPU and uses the same system support/control devices as the CPU (see figure a) below). This mode is possible with the above-mentioned processors.

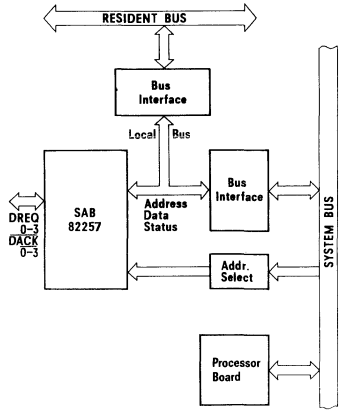
As a second basic operating mode a remote (standalone) mode is supported (see figure b) below). Here the SAB 82257 has his own sets of bus interface circuits and thus can dispose of its own local bus. This allows the DMA controller to work in parallel with the main CPU and therefore overall system performance could be increased. Besides, this mode is very useful for the design of modular systems and allows connecting the SAB 82257 to any other processor via the system bus independent of the processor's unique local bus.

Basic SAB 82257 Operating Modes

a) Local Mode

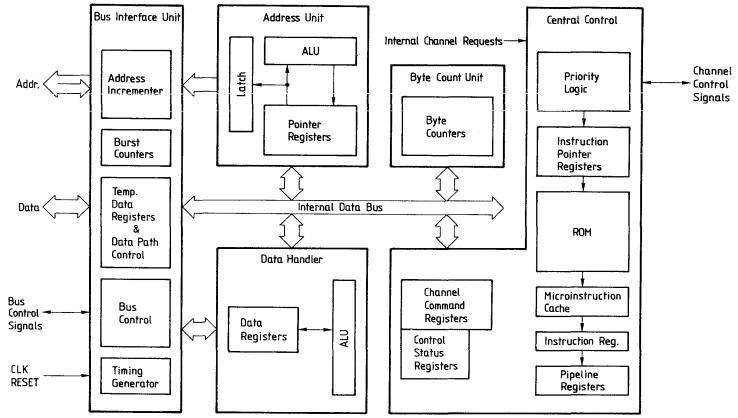


b) Remote Mode



The SAB 82257 has four independent DMA channels that can transfer up to 8 Mbytes/s in the single cycle mode (2 clocks/transfer). In the 2-cycle transfer mode the maximum rate is 4 Mbytes/s. Switching between channels induces no time penalty. Thus the overall maximum transfer rate of 8 Mbytes/s is also valid for multiple channel operation.
This fast operation is possible because of the pipelined architecture of the SAB 82257 that allows the different function units to work in parallel.

Block Diagram of SAB 82257



The SAB 82257 supports two address spaces, memory space and I/O space, each with a maximum address range of 16 Mbytes. In addition, the maximum block length (byte count) is also 16 Mbytes to support applications where large blocks of data have to be transferred (e.g. graphics).

As source or as destination, four parameters can be selected independently:

- address space (memory or I/O)
- physical bus width (8 bits or 16 bits),
- logical bus width (same as physical bus width or 8 bits on a 16-bit physical bus)
  and
- transfer direction (increasing, decreasing, fixed pointer or constant value).

If the physical bus width of source or destination does not meet the logical bus width an automatic byte/word assembly (word/byte disassembly) takes place if this minimizes the necessary transfers. The same is true if the logical bus widths of source and destination are different.
Transfers between different address spaces can be performed within one cycle or in two cycles, transfers within one address space can be performed only in two cycles.

The transfers can be executed free running or externally synchronized via DREQ where source or destination synchronization is possible.

In summary, this very symmetrical operation of the SAB 82257 gives the user a great amount of design flexibility.

Adaptive Bus Interface

As shown in the figure on page 3, the SAB 82257 bus interface has two basic timing modes: the 286 mode and the 186 mode. In 286 mode the SAB 82257 is directly coupled to an SAB 80286, in 186 mode to an SAB 80186 or SAB 80188. For each of these two modes a slightly different variation exists:

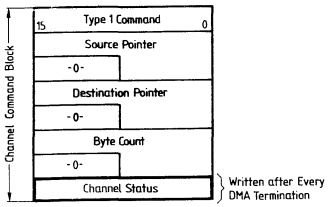
- For the 286 mode, the remote mode, where the SAB 82257 operates as a bus master on the system bus without being directly coupled to a processor. In this mode the SAB 82257 can dispose of its own local bus and the communication with the main processor is done via the system bus. To enable access to SAB 82257 registers by the main processor, the SAB 82257 must release its local bus. This "local bus arbitration" in remote mode is done via the $\overline{CS}$ and BREL lines.
- For the 186 mode the variation is the 8086 mode where the SAB 82257 supports the $\overline{RQ}/\overline{GT}$ protocol and thus can be directly coupled to an SAB 8086 or SAB 8088.

Memory-Based Communication

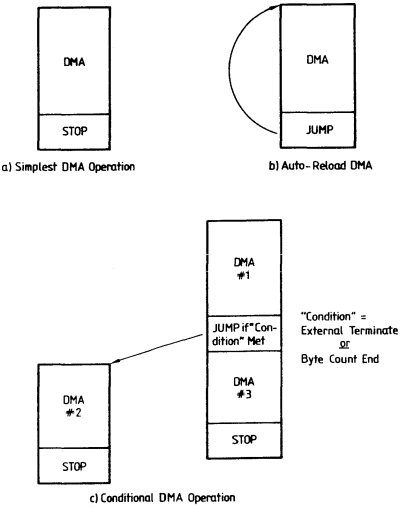
The normal communication between the SAB 82257 and the processor is memory-based. This means that all necessary data for a transfer is contained in a command block in memory accessible for CPU and SAB 82257 (see figure on next page). To start the transfer the CPU loads one of the command pointer registers of the SAB 82257 with the address of the command block and then gives a "start channel command". Getting the command the SAB 82257 loads the entire command block from memory into its on-chip channel registers and executes it.
On completing the operation, channel status information is written back by the SAB 82257 into the channel status word contained in the command block in memory. The command block structure of the SAB 82257 is identical with the structure of the SAB 82258 short command blocks. This allows to portate SAB 82257 software to the SAB 82258 and vice versa (in this case with restrictions).

Memory-Based Communication and Command Chaining

Memory-Based Communication



Command Chaining



Command Chaining

Command blocks for any channel can be chained for sequential execution (see figure above). When the SAB 82257 has completed the execution of a command, it automatically increments the command pointer, and starts to fetch and execute the next command block until a stop command is found. As a result a chain of command blocks can be executed by the SAB 82257 without any CPU intervention. Due to conditional and unconditional STOP and JUMP commands, quite complex sequences of DMA can be executed by the SAB 82257.

Data Chaining

Data chaining permits an automatic, dynamic linking of data blocks scattered in memory. There are two types: list and linked-list data chaining.

If for a DMA the source blocks are to be dynamically linked during DMA it is called source chaining and the effect is that of gathering data blocks and sending them out effectively as one block.

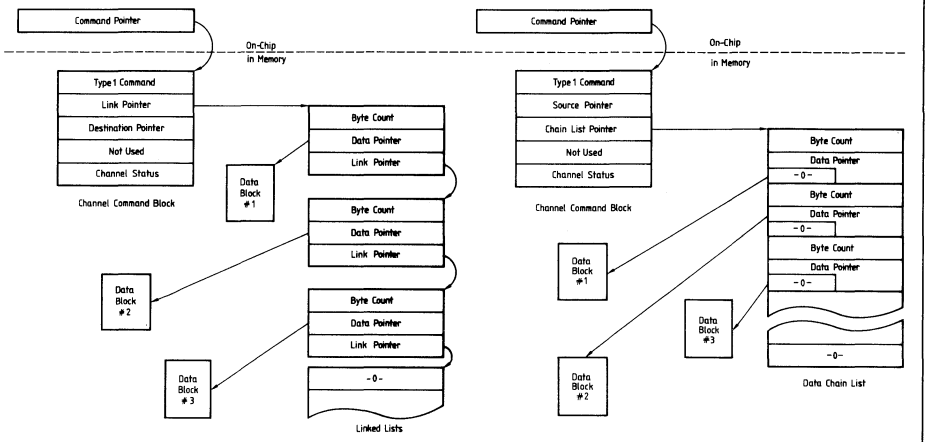
If one source block is dynamically broken up into multiple destination blocks, it is called destination chaining. This results in scattering of a block.

This dynamic linking and unlinking of data blocks makes the logical sequencing of data independent of its physical sequencing in memory.

Data Chaining

a) Linked List Chaining

b) List Chaining



In the case of linked list chaining (see figure a) above) each data block has a descriptor containing information on position of data block in memory, length of data block, and a pointer to the next descriptor.

During data transfer the data block 1 is sent out first, then 2 and so on till a 0 is encountered in the byte count field.

The second type of data chaining is list chaining (see figure b) above).

Unlike linked list chaining, here the data block descriptors are continuous in a block and thus determine the sequence of data blocks. The flexibility lost in terms of predefined sequence is gained in terms of linking time.

Operating the SAB 82257

Reset

When activating the reset input, the SAB 82257 is forced into its initial state. All channels and bus activities are stopped, tristate lines are tristated and the others enter the inactive state.
While the reset input is active, line A23/AREADY and HLDA must be forced to the appropriate levels to select the desired bus interface mode (see figures on page 3, 40 and 52).
After deactivating reset the inactive state is maintained, in addition the state of the SAB 82257 registers is as follows:

- general mode register, general burst register, general delay register, general status register and the four channel status registers are set to zero,
- all other registers and bits are undefined.

Note that the general mode register (GMR) should be loaded first to select the mode of operation before any other activity is started on the SAB 82257.

DMA Interface

The DMA interface consists of three lines:

- DREQ – DMA request,
- $\overline{\text{DACK}}$ – DMA acknowledge and
- $\overline{\text{EOD}}$ – end of DMA

The first two lines work as request and acknowledge lines to control synchronized DMA transfers as known from conventional DMA controllers.

A special feature of the SAB 82257 are the bidirectional $\overline{\text{EOD}}$ lines. Firstly they can be used as inputs to receive an asynchronous external terminate signal to terminate a running DMA. Secondly, as an output, they can be used to send out a pulse which interrupts the CPU and/or signals to the peripheral a specific status (e.g. transfer aborted, or end of a block, or send/receive next block ...).

The $\overline{\text{EOD}}$ output signal can be generated synchronously to a transfer (during the last transfer) or asynchronously to the transfers by a specific command.

In addition the $\overline{\text{EOD}}$ output of channel 2 can be used as a collective interrupt output for all DMA channels while the other three retain their normal function.

Slave Interface

The slave interface is used to access the SAB 82257 internal registers. Although nearly all of the communication between CPU and SAB 82257 is done via memory-based data blocks, some direct accesses to SAB 82257 registers are necessary. For example during the initialization phase the general mode register must be written, or to start a channel the command pointer register and the general command register must be loaded. Also during the debugging phase it is of great benefit to have access to all of the SAB 82257 internal registers.

The slave interface is enabled by the $\overline{\text{CS}}$ input and consists of the following lines:

- $\overline{\text{S0}}$, $\overline{\text{S1}}$ – status lines (inputs)
- $\overline{\text{RD}}$, $\overline{\text{WR}}$ – control lines (inputs)
- A0–A7 – register address (inputs)
- D0–D15 – data lines (inputs/outputs) and
- AD0–AD15 – address/data lines (inputs/outputs) for synchronous access in 186 mode

Note, that all of these lines are outputs if the SAB 82257 is an active bus master.

In 186 mode and 286 mode two types of accesses are possible:

- Synchronous access by means of the status lines. Processor and SAB 82257 are directly coupled and must use the same clock.
- Asynchronous access by using the control lines $\overline{\text{RD}}$ and $\overline{\text{WR}}$ (processor and SAB 82257 may have different clocks).

  In all modes except the synchronous access in 186 mode the register address must be supplied on address pins A0 to A7. Using synchronous access in 186 mode the address information is expected at address/data lines AD0 to AD7.

  In remote mode only the asynchronous access is possible because the SAB 82257 first has to release its local bus to enable the register access. On receiving an access request (activation of $\overline{\text{CS}}$ input) the SAB 82257 releases its local bus as soon as possible and signals this by activating the BREL line. Now the CPU can accomplish its access.

Bus Arbitration

To arbitrate access to the bus between the SAB 82257 and the processor, the signals HOLD and HLDA serve for communication. Normally the SAB 82257 competes for the bus via HOLD, the processor grants access to the bus via HLDA. The HLDA signal can also be deactivated in order to force the SAB 82257 off the bus for a certain reason (kick off). After reactivation of HLDA, the SAB 82257 will again get control of the bus.
In 8086 mode this communication is done by pulses via a single $\overline{\text{RQ}}/\overline{\text{GT}}$ line which uses the HOLD pin. In this case normally the HLDA input has no function. Nevertheless, even in 8086 mode the HLDA input can be used for kick-off. This provides some kind of additional bus arbitration.

Register Set

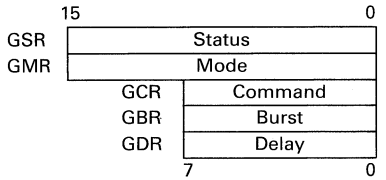
The following figure shows the user visible registers of the SAB 82257. A set of 5 registers, called the general registers, is used for all the 4 channels. The mode register is being written to first after reset and it describes the SAB 82257 environment – bus widths, etc. The general command register (GCR) is used to start and stop the DMA transfer on different channels. The general status register (GSR) shows the status of all the 4 channels; if the channel is running, if interrupt is pending, etc.

There is a set of channel registers for each of the 4 channels. Most channel registers serve as cache registers and need to be accessed only for debugging. During normal operation they are loaded automatically by the SAB 82257 (see next paragraph).

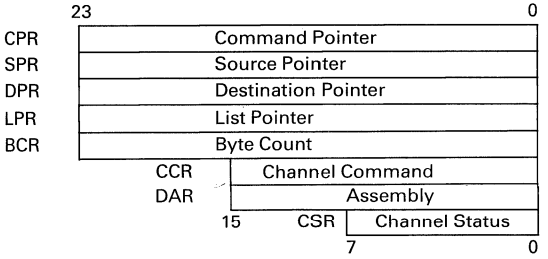
The layout of register addresses is shown in the figure on the next page. All register addresses are even. Locations not designated in that figure are reserved and should not be used.

SAB 82257 Register Set

General Registers



Channel Registers (4 sets; 1 per channel)



Register Address Arrangement

Address Bits 0–5	Address Bits 7, 6 00	01	10	11
0	GCR			
2				
4	GSR			
6				
8	GMR			
A	GBR			
C	GDR			
E				
10	CSR 0	CSR 1	CSR 2	CSR 3
12	DAR 0	DAR 1	DAR 2	DAR 3
14				
16				
18				
1A				
1C				
1E				
20	CPR L0	CPR L1	CPR L2	CPR L3
22	CPR H0	CPR H1	CPR H2	CPR H3
24	SPR L0	SPR L1	SPR L2	SPR L3
26	SPR H0	SPR H1	SPR H2	SPR H3
28	DPR L0	DPR L1	DPR L2	DPR L3
2A	DPR H0	DPR H1	DPR H2	DPR H3
2C				
2E				
30	LPR L0	LPR L1	LPR L2	LPR L3
32	LPR H0	LPR H1	LPR H2	LPR H3
34				
36				
38	BCR L0	BCR L1	BCR L2	BCR L3
3A	BCR H0	BCR H1	BCR H2	BCR H3
3C	CCR L0	CCR L1	CCR L2	CCR L3
3E	CCR H0	CCR H1	CCR H2	CCR H3

GCR = General Command Register
GSR = General Status Register
GMR = General Mode Register
GBR = General Burst Register
GDR = General Delay Register
CSR = Channel Status Register
DAR = Data Assembly Register

CPR = Command Pointer Register
SPR = Source Pointer Register
DPR = Destination Pointer Register
LPR = List Pointer Register
BCR = Byte Count Register
CCR = Channel Command Register

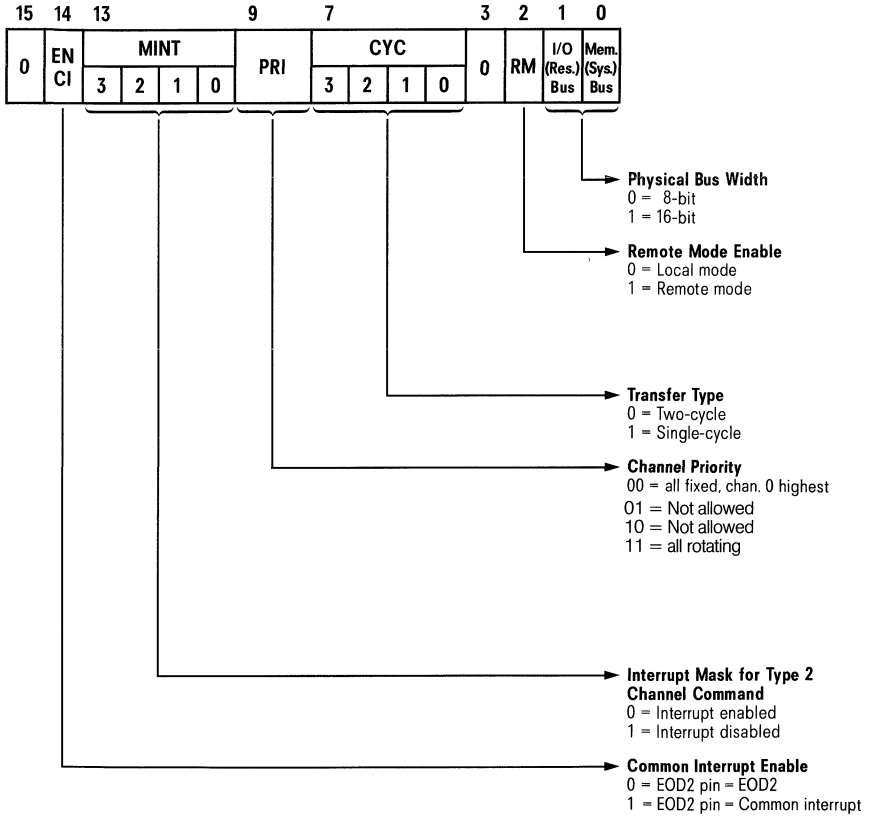
Register Description

General Mode Register

In the general mode register GMR (figure below) the system wide parameters are specified.

This register should be programmed first after reset; with an 8-bit bus program low byte first.

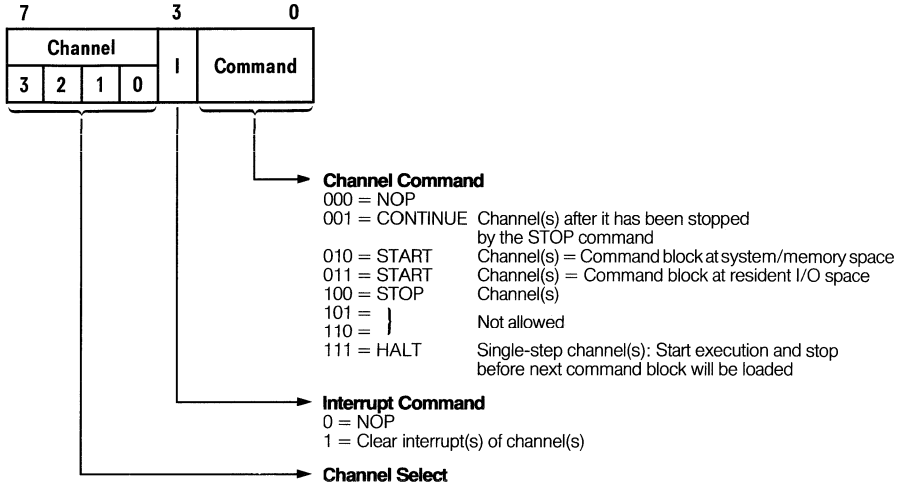
General Mode Register (GMR)



General Command Register

Individual channels are started and stopped by a command written to the general command register GCR (figure below). The GCR is directly loaded by the CPU.

General Command Register (GCR)



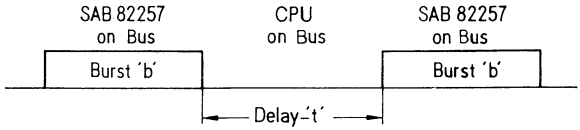
General Burst and Delay Register

It is possible to restrict the bus load generated by the SAB 82257 on the CPU bus by programming the burst and the delay register. The bus load is defined by the formula given in figure a) below. The factor b (burst) is programmed in the general burst register GBR, t (delay time) in the general delay register GDR (see figures b and c).

Since the SAB 82257 can also execute locked bus cycles, the maximum burst length consists of b+3 (8-bit bus) or b+2 (16-bit bus) bus cycles. GBR and GDR must be directly loaded by the CPU. Loading GBR with 0 leads to no bus load limitations for the SAB 82257 (default after reset).

General Burst and Delay Register

a) Bus Loading

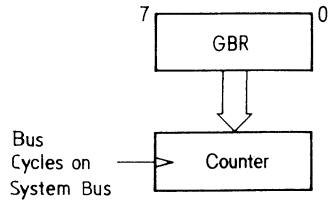


$$\text{Bus Load Due to SAB 82257} = \frac{b}{b+t}$$

b) General Burst Register (GBR) - to Program 'b'

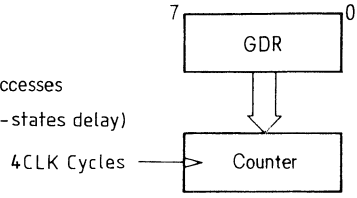
Determines Max. Number of Contiguous Bus Cycles from SAB 82257

If GBR=0, No Limit



c) General Delay Register (GDR) - to Program 't'

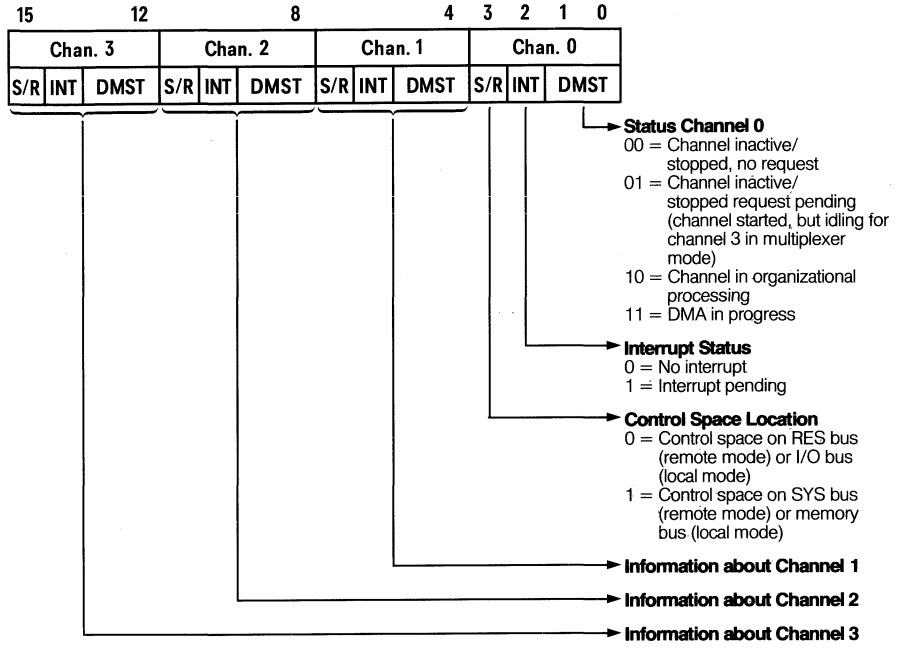
Determines Min. Number of Clock Cycles Between Burst Accesses (default after reset=0, i.e. 4 T-states delay)



General Status Register

The general status register GSR (figure below) shows the current states of all the channels.

General Status Register (GSR)



Channel Commands

The channel commands are contained in the channel command block. 15 bits are used to specify the command. There are two types of channel commands:

- Type 1: for data movement
- Type 2: for command chaining control

The command block for a type 1 command is 26 bytes long (see figure on page 17).

The type 1 command fields (see figure on page 27) contain information on:

a. Bus width of source and destination
b. If source and/or destination address should be incremented or decremented or kept constant during the transfer
c. If source/destination is in memory or I/O space (local mode) or in system or resident space (remote mode)
d. If data chaining (list or linked-list) is to be performed
e. If the data transfer is synchronized (source or destination).

Type 2 command blocks are 6 bytes long (see figure on page 28) of which the first 2 bytes form the command and the rest is either a relative displacement or an absolute address for the JUMP operation. There are two basic type 2 commands (see figure on page 28):

a. JUMP – conditional and non-conditional
b. STOP – conditional and non-conditional

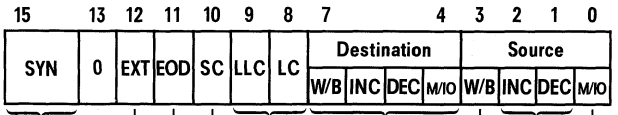
The conditional case tests for either of the 2 condition bits which are altered at the termination of any DMA operation:

- Termination due to byte count end
- Termination due to external terminate

It is thus possible to JUMP or STOP further execution of commands based on any of these conditions and optionally generate $\overline{EOD}$ or interrupt signal.

The combination of type 1 and 2 commands gives the SAB 82257 a high degree of "programmability". It can thus execute quite complex algorithms with a fairly low demand for CPU service.

Type 1 (DMA) Channel Command



Source Description
Associated Space
0 = I/O or resident
1 = Memory or system

Source Pointer
00 = Pointer not modified
01 = Decrement pointer
10 = Increment pointer
11 = No pointer (constant value)

Logical Bus Width
0 = 8-bit
1 = 16-bit

Destination Description
Same as source description

Data Chaining

LLC	LC	
0	0	No chaining
0	1	List chaining
1	0	Linked list chaining
1	1	Not allowed

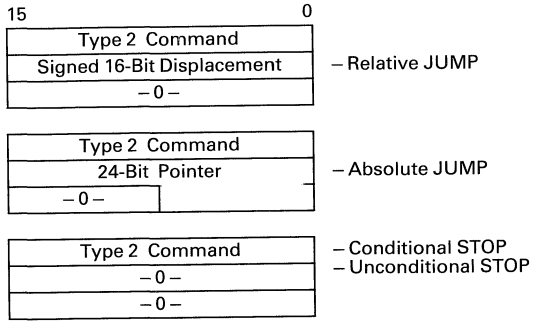
Select Chaining
0 = Destination data chaining
1 = Source data chaining

Enable $\overline{\text{EOD}}$ Output

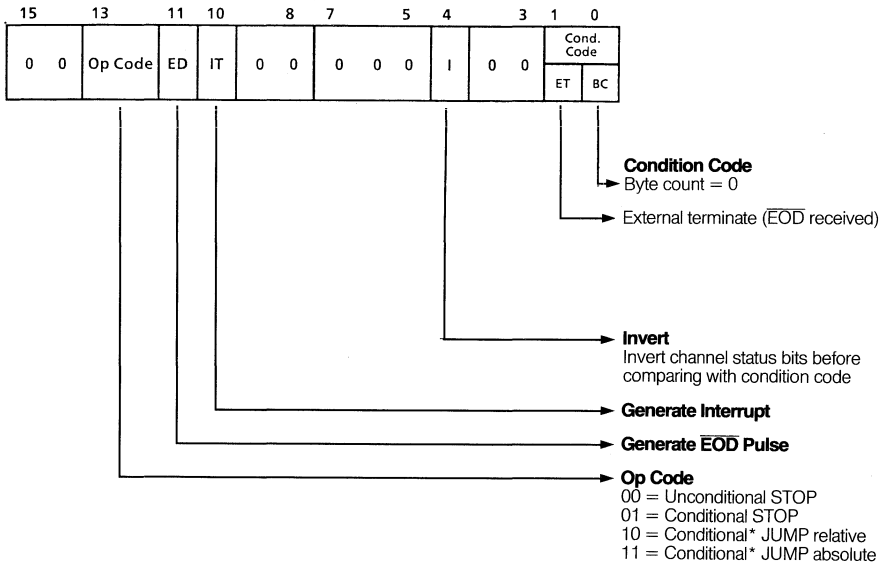
Enable External Terminate Input

Synchronization
00 = Not valid (type 2 command)
01 = Source synchronization
10 = Destination synchronization
11 = No synchronization (free running)

Type 2 Command Blocks (for command chaining control)



Type 2 Command Format

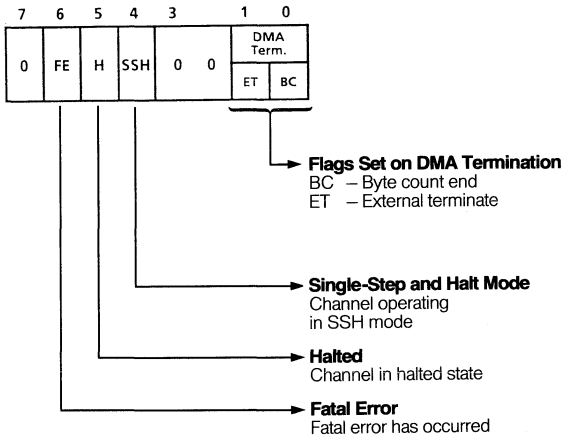


*) Unconditional JUMP when both condition code bits are set 1.

Channel Status Register

For each channel there is a channel status register (see figure below). This register shows the current state of the appropriate channel.

Channel Status Register



Timings

The bus timings in 286 and remote mode are identical to that for SAB 80286, in the 186 and 8086 mode the timings are identical to that for SAB 80186. For exact timings see timing diagrams of AC Characteristics.

Asynchronous control inputs are specified with setup and hold times which are only important to determine whether the SAB 82257 responds to the signal in the current cycle or the next cycle.

The following pages hold two sections of ac characteristics and waveforms. The first section refers to 286 mode and remote mode, the second one to 186 mode and 8086 mode.

Absolute Maximum Ratings [1]

Temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to +7V
Power dissipation	3.6W

DC Characteristics [2]

TA = 0 to 70°C; TC = 0 to 100°C; VCC = +5V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
VIL	Input low voltage (except CLK)	−0.5	+0.8	V	–
VIH	Input high voltage (except CLK)	2.0	VCC+0.5	V	–
VOL	Output low voltage	–	0.45	V	IOL = 3.0 mA
VOH	Output high voltage	2.4	–	V	IOH = −400 µA
ICC	Power supply current	–	450	mA	TA = 25°C, all outputs open
ILI	Input leakage current				
	$\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, M/$\overline{IO}$	–	−200	µA	0V ≤ VIN ≤ VCC
	HOLD ($\overline{RQ}$/$\overline{GT}$ mode), $\overline{EOD}$	–	−1.5	mA	0V ≤ VIN ≤ VCC
	A23 (AREADY), A21 [3]	–	−1.5	mA	0V ≤ VIN ≤ VCC
	other pins	–	±10	µA	0V ≤ VIN ≤ VCC
ILO	Output leakage current	–	±10	µA	0.45V ≤ VOUT ≤ VCC
VCL	Clock input low voltage	−0.5	+0.6	V	–
VCH	Clock input high voltage	3.8	VCC+1.0	V	–
CIN	Capacitance of inputs (except CLK)	–	10	pF	fC = 1 MHz
CIO	Capacitance of I/O or outputs	–	20	pF	fC = 1 MHz
CCLK	Capacitance of CLK input	–	12	pF	fC = 1 MHz

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Clock must be applied.

[3] This specification is valid only during RESET.

AC Characteristics SAB 82257 (286 mode)

TA = 0 to 70°C; TC = 0 to 100°C; VCC = +5V ±10%
Any output timing is measured at 1.5V.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
1	CLK cycle period	62	250	ns	–
2	CLK low time	15	230	ns	at 1.0 V
3	CLK high time	20	235	ns	at 3.6 V
4	Address/control output delay	–	60	ns	CL = 100 pF
5	Status output delay	–	40	ns	CL = 100 pF
6	Sync data setup time	10	–	ns	–
7	Sync data hold time	5	–	ns	–
8	Sync $\overline{\text{READY}}$ setup time	38	–	ns	–
9	Sync $\overline{\text{READY}}$ hold time	25	–	ns	–
10	Sync control input setup time	20	–	ns	–
11	Sync control/address input hold time	20	–	ns	–
12	Sync address setup time	2.5	–	ns	–
13	Data/control output delay	–	50	ns	CL = 100 pF
14	Data/control float delay	–	50	ns	–
15	$\overline{\text{BHE}}$ setup time	60	–	ns	–
16	Write command width	4CLK+40	–	ns	–
17	Async data setup time	2CLK+30	–	ns	–
18	Async address setup time	20	–	ns	–
19	Async data access time	–	5CLK+70	ns	–

AC Characteristics SAB 82257 (286 mode; cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
28	Mode select setup time	2CLK+20	–	ns	–
29	Mode select hold time	0	–	ns	–
33	Command recovery time	4CLK+40	–	ns	–
34	CLK rise time	–	15	ns	1.0 to 3.6V
35	CLK fall time	–	15	ns	3.6 to 1.0V
36	DREQ inactive after $\overline{\text{DACK}}$ active	0	–	ns	–
37	$\overline{\text{CS}}$ active response time	–	16CLK +80	ns	[1]
39	$\overline{\text{CS}}$ active after BREL inactive	0	–	ns	–
42	HOLD active to HLDA active	0	–	ns	–
43	Async input setup time	20	–	ns	[2]
44	Async input hold time	20	–	ns	[2]
47	Async HLDA high time	2CLK+40	–	ns	[3]
49	HOLD output low time	4CLK–50	–	ns	–
50	HLDA low to HOLD low delay	–	16CLK +70	ns	[1]
53	Read command width	T19	–	ns	–
54	Async access setup time	20	–	ns	–
55	Async access hold time	20	–	ns	–
56	$\overline{\text{CS}}$ hold time	40	–	ns	–

[1] If wait states are inserted, the maximum value has to be extended by the time required for the wait states for 3 bus cycles.

[2] These specifications are given for testing purposes only to assure recognition at a specific clock edge.

[3] This timing is valid if the signal is not synchronous, i.e. does not meet the specified setup and hold times.

AC Characteristics SAB 82257-6 (286 mode)

TA = 0 to 70°C; TC = 0 to 100°C; VCC = +5V ±10%
Any output timing is measured at 1.5V.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
1	CLK cycle period	80	250	ns	–
2	CLK low time	20	225	ns	at 1.0 V
3	CLK high time	25	230	ns	at 3.6 V
4	Address/control output delay	–	75	ns	CL = 100 pF
5	Status output delay	–	55	ns	CL = 100 pF
6	Sync data setup time	20	–	ns	–
7	Sync data hold time	8	–	ns	–
8	Sync $\overline{\text{READY}}$ setup time	50	–	ns	–
9	Sync $\overline{\text{READY}}$ hold time	35	–	ns	–
10	Sync control input setup time	30	–	ns	–
11	Sync control/address input hold time	30	–	ns	–
12	Sync address setup time	3	–	ns	–
13	Data/control output delay	0	65	ns	CL = 100 pF
14	Data/control float delay	–	65	ns	–
15	$\overline{\text{BHE}}$ setup time	80	–	ns	–
16	Write command width	4CLK+40	–	ns	–
17	Async data setup time	2CLK+50	–	ns	–
18	Async address setup time	30	–	ns	–
19	Async data access time	–	5CLK+95	ns	–

AC Characteristics SAB 82257-6 (286 mode; cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
28	Mode select setup time	2CLK+30	–	ns	–
29	Mode select hold time	0	–	ns	–
33	Command recovery time	4CLK+40	–	ns	–
34	CLK rise time	–	15	ns	1.0 to 3.6V
35	CLK fall time	–	15	ns	3.6 to 1.0V
36	DREQ inactive after $\overline{\text{DACK}}$ active	0	–	ns	–
37	$\overline{\text{CS}}$ active response time	–	16CLK +10	ns	[1]
39	$\overline{\text{CS}}$ active after BREL inactive	0	–	ns	–
42	HOLD active to HLDA active	0	–	ns	–
43	Async input setup time	30	–	ns	[2]
44	Async input hold time	30	–	ns	[2]
47	Async HLDA high time	2CLK+60	–	ns	[3]
49	HOLD output low time	4CLK–65	–	ns	–
50	HLDA low to HOLD low delay	–	16CLK +95	ns	[1]
53	Read command width	T19	–	ns	–
54	Async access setup time	30	–	ns	–
55	Async access hold time	30	–	ns	–
56	$\overline{\text{CS}}$ hold time	40	–	ns	–

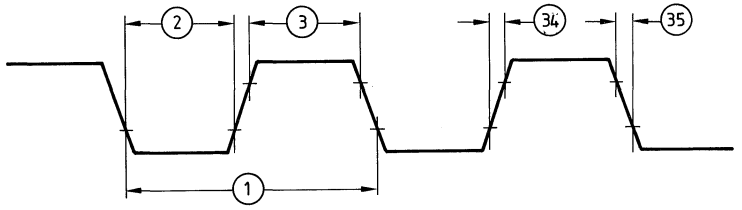
[1] If wait states are inserted, the maximum value has to be extended by the time required for the wait states for 3 bus cycles.

[2] These specifications are given for testing purposes only to assure recognition at a specific clock edge.

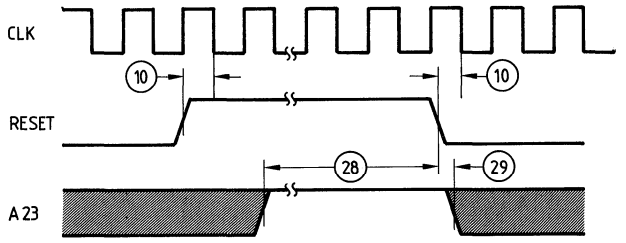
[3] This timing is valid if the signal is not synchronous, i.e. does not meet the specified setup and hold times.

Waveforms

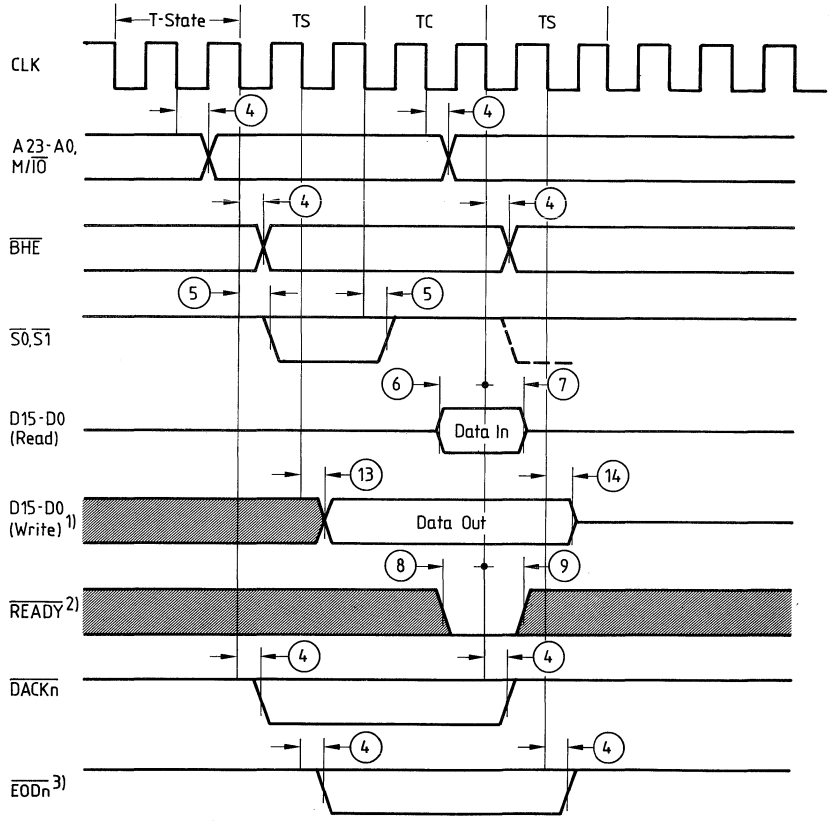
Clock Signal (286 mode)



Mode Selection on RESET (286 mode)

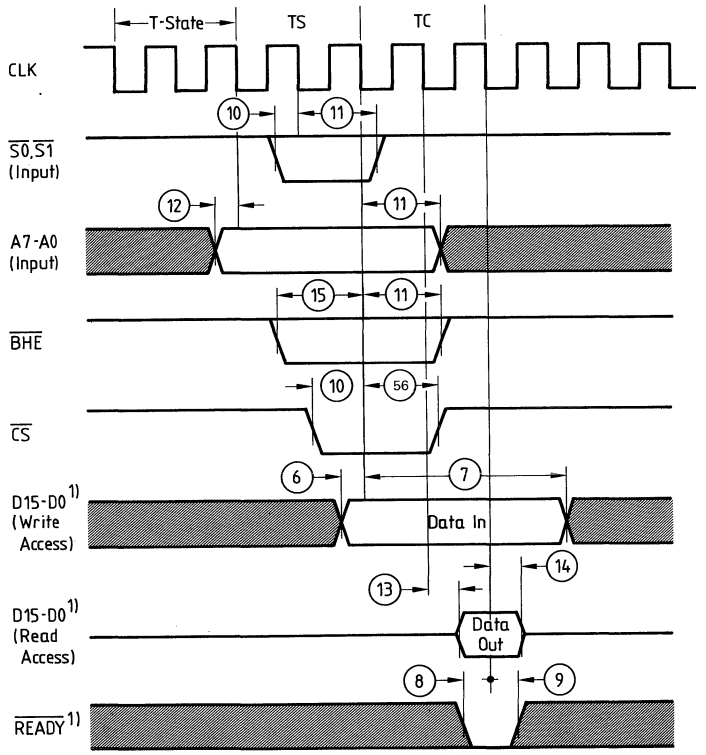


Major Timing for Active Bus Cycles (286 mode)



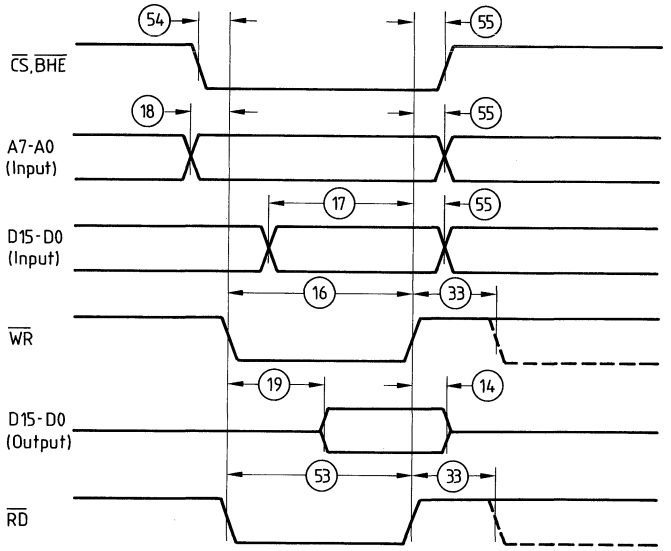
1) If executing a single cycle transfer, D15 to D0 float like during read cycles!
2) TC will be repeated if $\overline{\text{READY}}$ is inactive at the sampling point (end of current TC).
3) Initiated by terminal count.

Synchronous Access (286 mode)

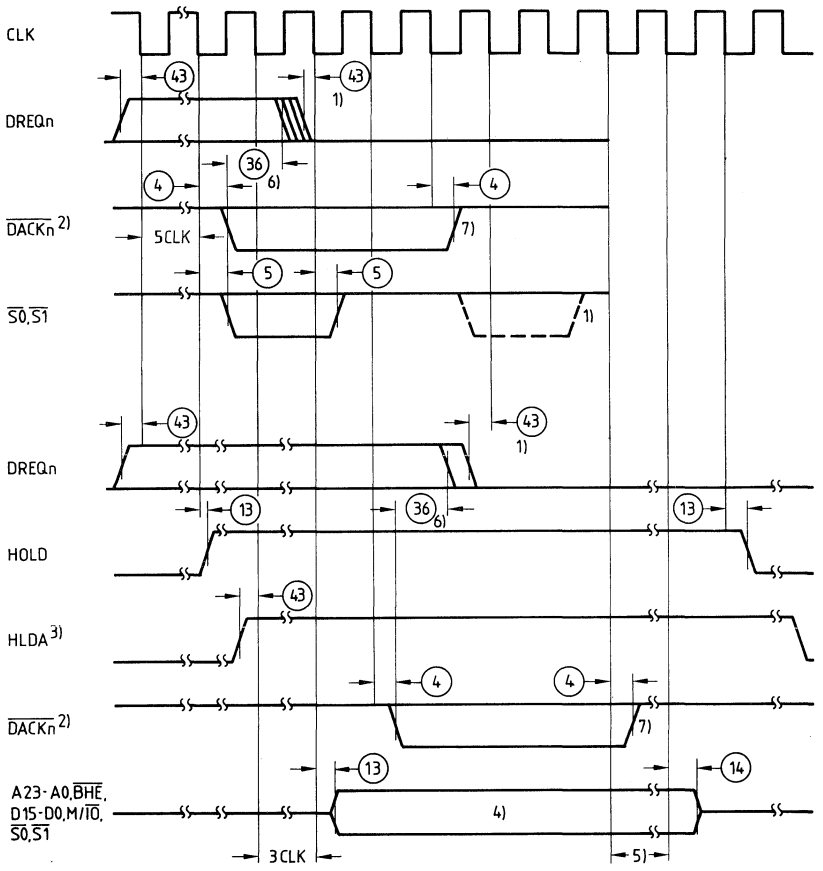


[1] The processor will repeat TC, if $\overline{\text{READY}}$ is not active at the sampling point (end of current TC). The SAB 82257 will output data until the end of the repeated TC (read access) or sample the data bus again at the beginning of the repeated TC (write access).

Asynchronous Access (286 mode)



DMA Control (286 mode)



[1] If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfers will be executed.

[2] Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.

[3] The SAB 82257 can be forced off the bus by driving HLDA inactive (see "Bus Arbitration").

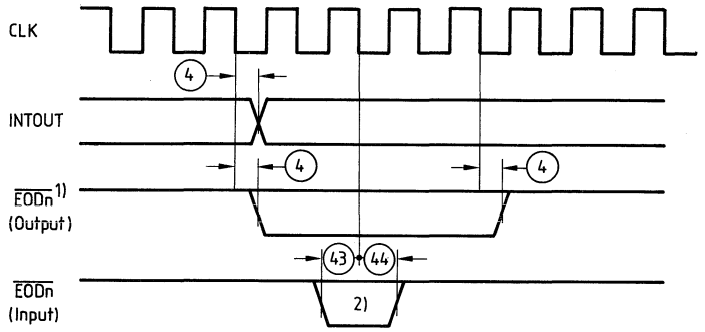
[4] Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycles".

[5] The SAB 82257 may execute additional bus cycles, e.g. for command chaining.

[6] Minimum time to execute bus cycle.

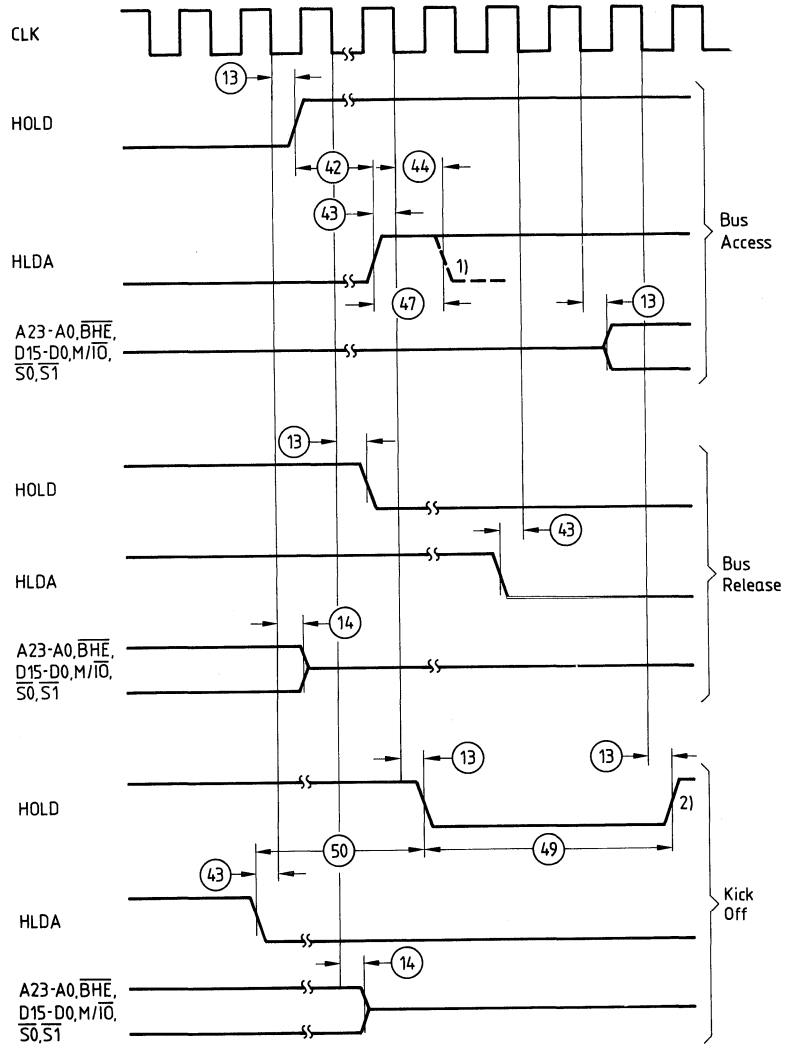
[7] If the SAB 82257 does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the $\overline{\text{DACKn}}$ signal can be prolonged by two T-states.

$\overline{\text{EOD}}$/INTOUT Timing (286 mode)



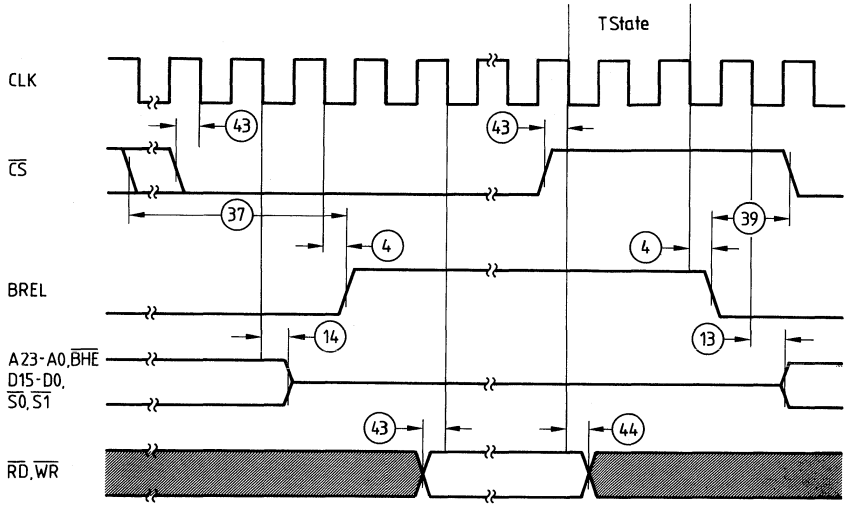
[1] Initiated by type 2 command.
[2] $\overline{\text{EOD}}$ input minimum pulse width is 3 CLKs if the signal is asynchronous.

Bus Arbitration (286 mode)



[1] Minimum HLDA high time before kick-off to respond to HOLD signal.
[2] Earliest possible reactivation of HOLD after deactivation of HLDA.

Access in Remote Mode



AC Characteristics SAB 82257 (186 mode)

TA = 0 to 70°C; TC = 0 to 100°C; VCC = +5V ±10%
Any output timing is measured at 1.5V.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
4	Control output delay	–	60	ns	–
6	Sync address/data setup time	10	–	ns	–
7	Sync data hold time	5	–	ns	–
10	Sync control input setup time	20	–	ns	–
11	Sync control/address input hold time	20	–	ns	–
13	Data/control delay	–	50	ns	CL = 100 pF
14	Data float delay	–	50	ns	–
16	Write command width	2CLK+40	–	ns	–
17	Async data setup time	CLK+30	–	ns	–
18	Async address setup time	20	–	ns	–
19	Async data access time	–	2CLK +T22+70	ns	–
20	CLK cycle period	125	500	ns	–
21	CLK low time	55	–	ns	at 1.5V
22	CLK high time	55	–	ns	at 1.5V
23	CLK rise time	–	15	ns	1.0 to 3.5V
24	CLK fall time	–	15	ns	3.5 to 1.0V
25	AREADY active setup time	20	–	ns	[2]
26	AREADY hold time	15	–	ns	[2]
27	AREADY inactive setup time	35	–	ns	–

[2] These specifications are given for testing purposes only to assure recognition at a specific clock edge.

AC Characteristics SAB 82257 (186 mode; cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
28	Mode select setup time	2CLK+20	–	ns	–
29	Mode select hold time	0	–	ns	–
30	Address/data output delay	10	50	ns	CL = 20 to 200 pF
31	Status output delay	10	55	ns	–
32	Float delay	10	50	ns	–
33	Command recovery time	2CLK+40	–	ns	–
36	DREQ inactive after $\overline{\text{DACK}}$ active	0	–	ns	–
38	ALE output delay	–	40	ns	–
40	Address/control input hold time	10	–	ns	–
41	Address input setup time	10	–	ns	–
42	HOLD active to HLDA active	0	–	ns	–
43	Async control input setup time	20	–	ns	[2]
44	Async control input hold time	20	–	ns	[2]
45	HLDA hold time	10	–	ns	–
46	Async HLDA high time	CLK+40	–	ns	[3]
48	HOLD output delay	5	70	ns	–
51	HOLD output low time	2CLK−70	–	ns	–
52	HLDA low to HOLD low delay	–	12CLK +90	ns	[1]
53	Read command width	T19	–	ns	–
54	Async access setup time	20	–	ns	–
55	Async access hold time	20	–	ns	–
57	SREADY hold time	15	–	ns	–
58	Status setup time	35	–	ns	–

[1] If wait states are inserted, the maximum value has to be extended by the time required for the wait states for 2 bus cycles.

[2] These specifications are given for testing purposes only to assure recognition at a specific clock edge.

[3] This timing is valid, if the signal is not synchronous, i.e. does not meet the specified setup and hold times.

AC Characteristics SAB 82257-6 (186 mode)

TA = 0 to 70°C; TC = 0 to 100°C; VCC = +5V ±10%
Any output timing is measured at 1.5V.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
4	Control output delay	–	75	ns	–
6	Sync address/data setup time	20	–	ns	–
7	Sync data hold time	8	–	ns	–
10	Sync control input setup time	25	–	ns	–
11	Sync control/address input hold time	25	–	ns	–
13	Data/control delay	0	65	ns	CL = 100 pF
14	Data float delay	–	80	ns	–
16	Write command width	2CLK+40	–	ns	–
17	Async data setup time	CLK+50	–	ns	–
18	Async address setup time	30	–	ns	–
19	Async data access time	–	2CLK +T22+85	ns	–
20	CLK cycle period	160	500	ns	–
21	CLK low time	75	–	ns	at 1.5V
22	CLK high time	75	–	ns	at 1.5V
23	CLK rise time	–	15	ns	1.0 to 3.5V
24	CLK fall time	–	15	ns	3.5 to 1.0V
25	AREADY active setup time	20	–	ns	[2]
26	AREADY hold time	15	–	ns	[2]
27	AREADY inactive setup time	35	–	ns	–

[2] These specifications are given for testing purposes only to assure recognition at a specific clock edge.

AC Characteristics SAB 82257-6 (186 mode; cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
28	Mode select setup time	2CLK+30	–	ns	–
29	Mode select hold time	0	–	ns	–
30	Address/data output delay	10	55	ns	CL = 20 to 200 pF
31	Status output delay	10	75	ns	–
32	Float delay	10	55	ns	–
33	Command recovery time	2CLK+40	–	ns	–
36	DREQ inactive after $\overline{\text{DACK}}$ active	0	–	ns	–
38	ALE output delay	–	50	ns	–
40	Address/control input hold time	15	–	ns	–
41	Address input setup time	10	–	ns	–
42	HOLD active to HLDA active	0	–	ns	–
43	Async control input setup time	30	–	ns	[2]
44	Async control input hold time	30	–	ns	[2]
45	HLDA hold time	10	–	ns	–
46	Async HLDA high time	CLK+60	–	ns	[3]
48	HOLD output delay	5	90	ns	–
51	HOLD output low time	2CLK−90	–	ns	–
52	HLDA low to HOLD low delay	–	12CLK +120	ns	[1]
53	Read command width	T19	–	ns	–
54	Async access setup time	30	–	ns	–
55	Async access hold time	30	–	ns	–
57	SREADY hold time	15	–	ns	–
58	Status setup time	35	–	ns	–

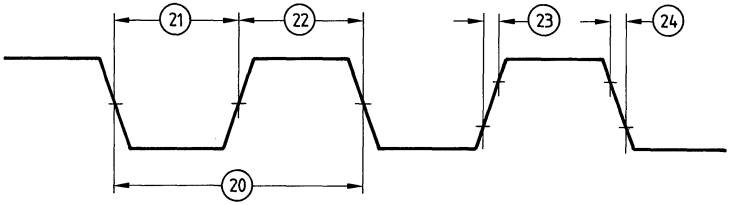
[1] If wait states are inserted, the maximum value has to be extended by the time required for the wait states for 2 bus cycles.

[2] These specifications are given for testing purposes only to assure recognition at a specific clock edge.

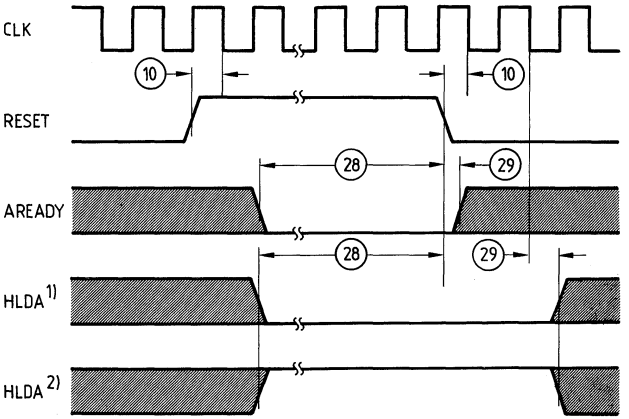
[3] This timing is valid, if the signal is not synchronous, i.e. does not meet the specified setup and hold times.

Waveforms

Clock Signal (186 mode)

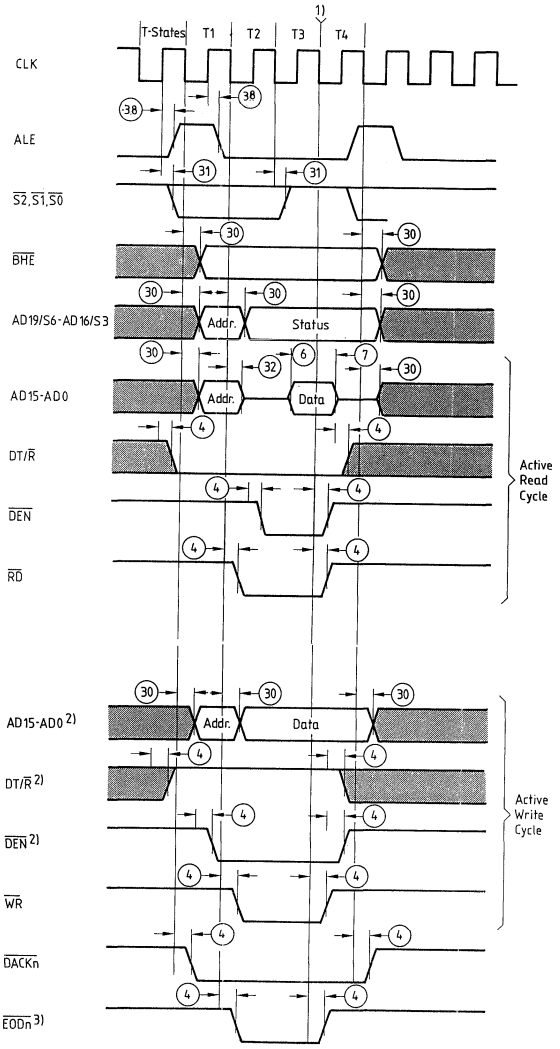


Mode Selection on RESET (186 mode)



1) To operate in 186 mode with HOLD/HLDA protocol.
2) To operate in 8086 mode with $\overline{RQ}/\overline{GT}$ protocol.

Major Timing for Active Bus Cycles (186 mode)

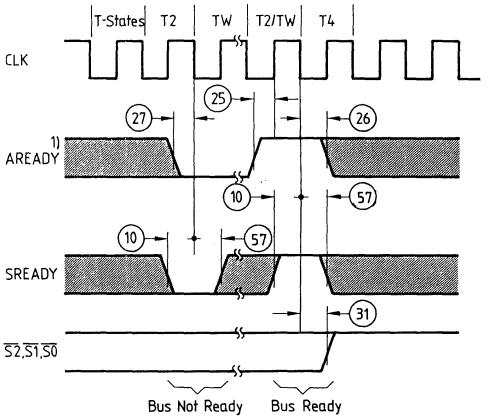


1) A wait state is inserted after T3 or TW, whenever the bus is not ready at the beginning of T3 or TW (see "Bus Cycle Termination"). The status must be valid just prior to T4.

2) For a single-cycle transfer the timing of AD15-AD0, DT/$\overline{R}$ and $\overline{DEN}$ is identical to a read cycle. AD15-AD0 will float as during a read cycle.

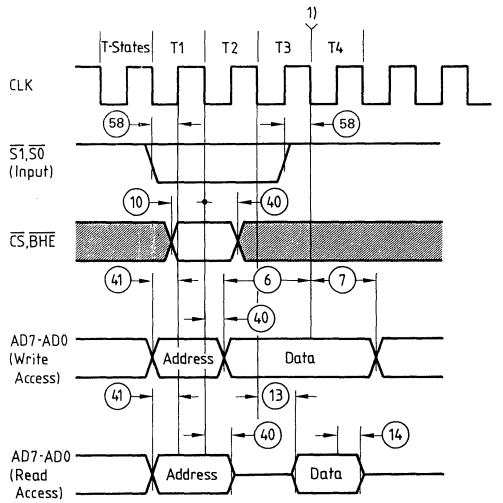
3) Initiated by terminal count.

Bus Cycle Termination (186 mode)



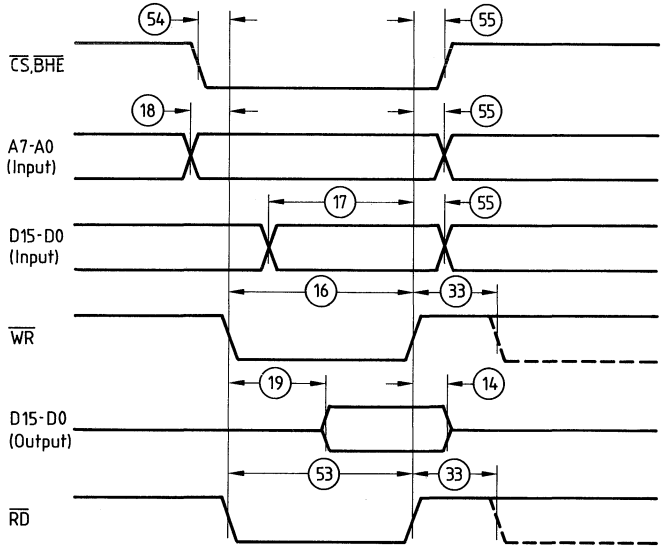
1) Only the rising edge of AREADY is synchronized internally to CLK.
The falling edge must be synchronized externally.

Synchronous Access (186 mode)

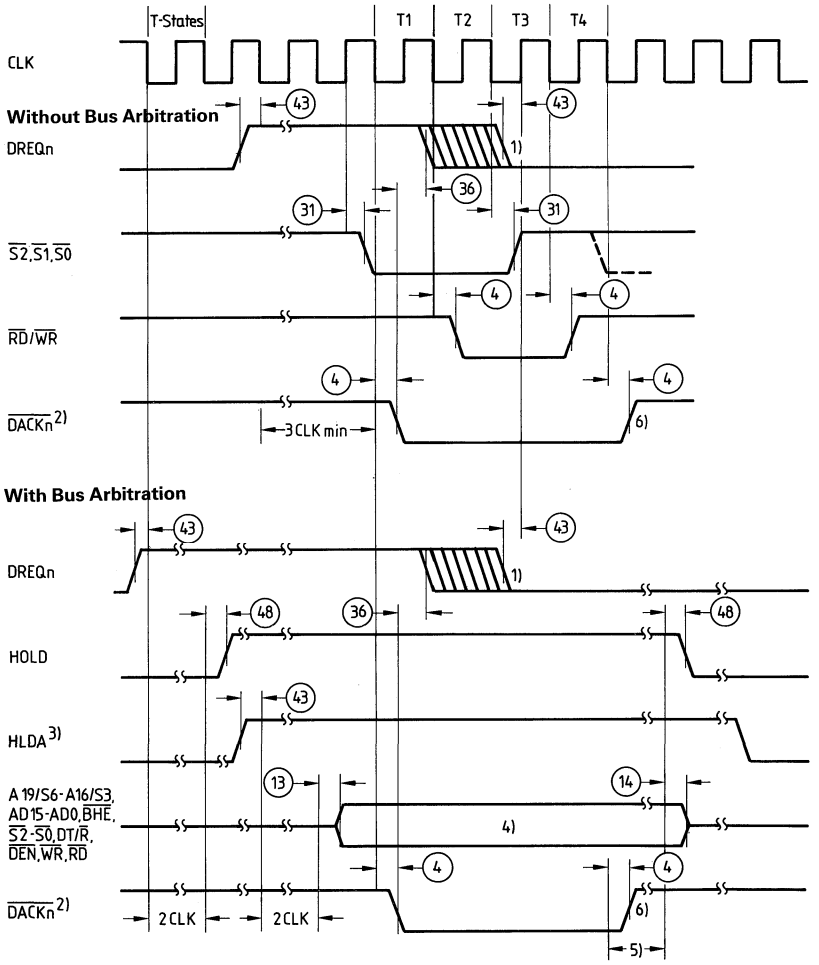


1) Additional wait cycles may be inserted. Status must be valid just prior to T4.

Asynchronous Access (186 mode)



DMA Control (186 mode)



[1] If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.

[2] Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.

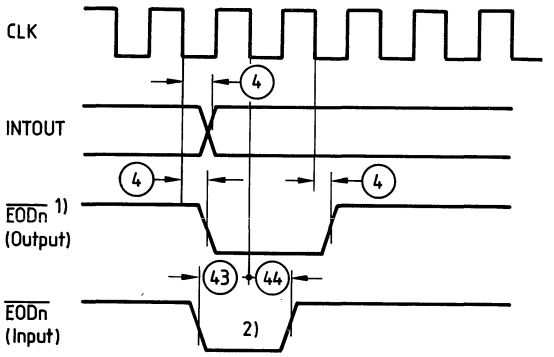
[3] The SAB 82257 can be forced off the bus by driving HLDA inactive (see "Bus Arbitration").

[4] Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycles".

[5] The SAB 82257 may execute additional bus cycles, e.g. for command chaining.

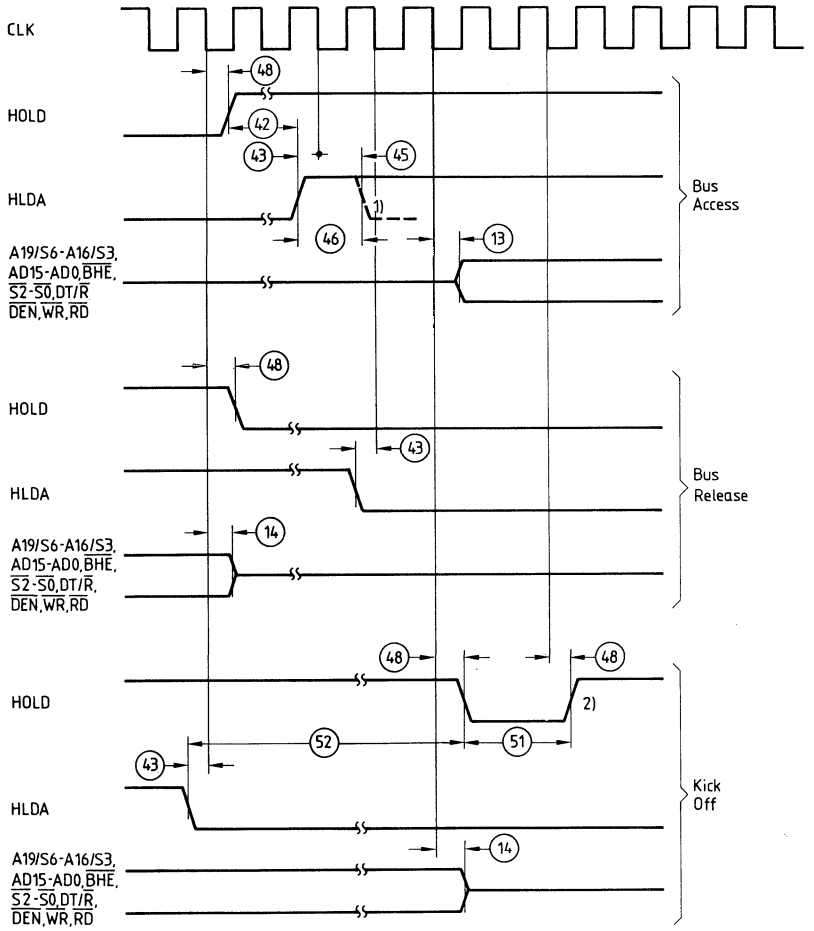
[6] If the SAB 82257 does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn signal can be prolonged by two T-states.

$\overline{\text{EOD}}$/INTOUT Timing (186 mode)



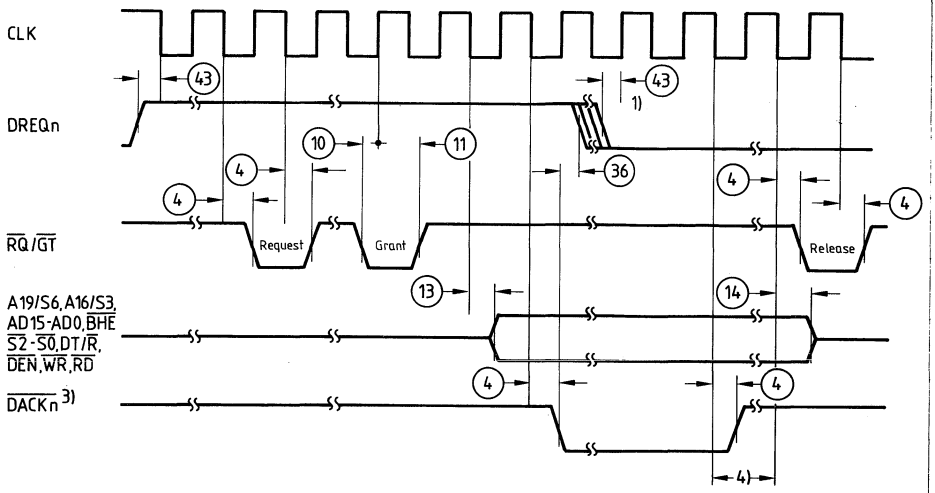
[1] Initiated by type 2 command.
[2] $\overline{\text{EOD}}$ input minimum pulse width is 2CLKs if the signal is asynchronous.

Bus Arbitration (186 mode)



[1] Minimum HLDA high time before kick-off to respond to HOLD signal.
[2] Earliest possible reactivation of HOLD after deactivation of HLDA.

DMA Control with $\overline{RQ}/\overline{GT}$ Protocol (8086 mode)



[1] If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent bus cycles are executed.

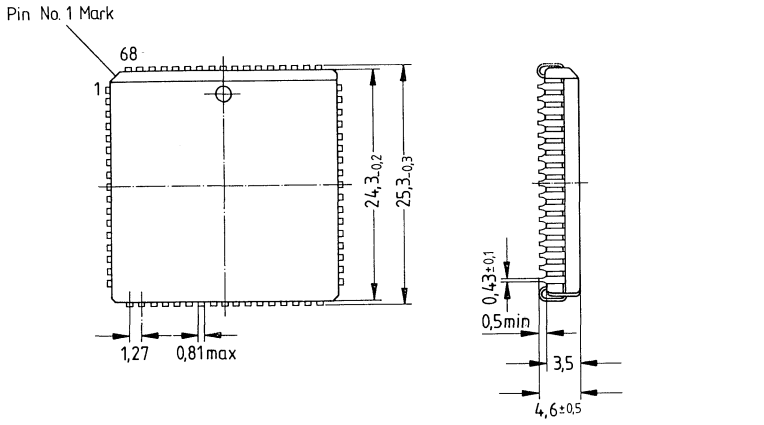
[2] Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycles".

[3] Refers to the highest priority request. Acknowledge of lower priority requests may be delayed by higher priority requests.

[4] The SAB 82257 may execute additional bus cycles, e.g. for command chaining.

Package Outline

Plastic Package, PLCC, 68 pins



Dimensions in mm

Ordering Information

Type	Ordering code	Function
SAB 82257-N	Q67120-P176	High-performance DMA controller, 8 MHz
SAB 82257-6-N	Q67120-P179	High-performance DMA controller, 6 MHz

Preliminary

SAB 82258A
Advanced DMA Controller for 16/32-Bit Microcomputer Systems

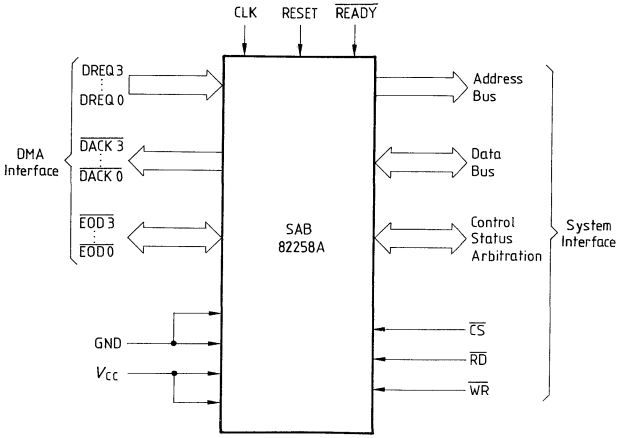
SAB 82258A 8 MHz

- Fully upward-compatible with SAB 82258 (hardware and software)
- Supports 32-bit fly-by transfers
- 4 independent high-speed DMA channels
- Multiplexer channel operation supporting up to 32 subchannels
- Adaptive on-chip bus interface for direct connection to 16/8-bit processors
- Standalone operation for modular systems
- Programmable bus loading
- Transfer rates up to 10 Mbytes/s (10 MHz system)

SAB 82258A-1 10 MHz

- 16 Mbytes addressing range
- 16 Mbytes maximum block size
- Command chaining for automatic processing
- Automatic data chaining (scattering/gathering) for flexible data structures
- "On-the-fly" compare, translate and verify operations
- Single and double cycle transfers
- Automatic assembly/disassembly of data
- Memory-based communication scheme with CPU

Logic Symbol

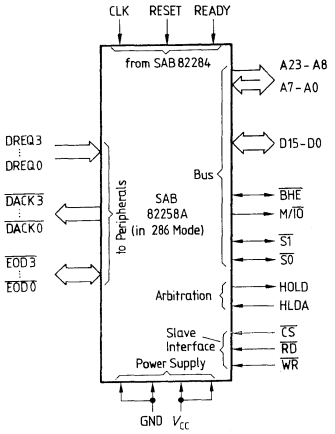


The SAB 82258A is an advanced DMA (direct memory access) controller designed especially for the 16-bit microprocessors SAB 80286 and SAB 8086/186/88/188. In addition, the operation with other processors is supported by the remote mode. The 32-bit fly-by transfer mode supports operation with 32-bit microprocessors (like 80386). The SAB 82258A has 4 independent DMA channels which can transfer data at rates up to 10 Mbytes/second at 10 MHz clock in an SAB 80286 system or up to 5 Mbytes/second at 10 MHz in an SAB 8086/80186 system. Using 32-bit fly-by transfers it can transfer 20 Mbytes/second at 10 MHz. This great bandwidth allows the user to handle very fast data transfer or a large number of concurrent peripherals. The device is fabricated in advanced +5 V N-channel Siemens MYMOS technology and packaged in a 68-pin package.

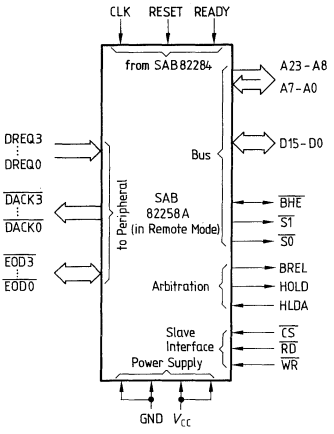
Modes of Operation, Adaptive Bus Interface

The SAB 82258A has been defined to work with all 16-bit processors, i.e. SAB 80286, SAB 80186/188 and SAB 8086/88 without additional support and interface logic. Hence the local buses of above processors are different in signals, functions and timings. The SAB 82258A has an adaptive bus interface to meet the different requirements of these local buses.
As a result of this, a bus compatibility with identical timing is attained with processors SAB 80286, SAB 80186 and SAB 8086. A compatibility with the 8-bit bus versions of these processors SAB 8088 and SAB 80188 is also guaranteed by defining the physical bus width of the SAB 82258A (per software) as 8 bits. The only difference in operation with SAB 8086 or SAB 80186 is that for SAB 8086 the HOLD pin functions as $\overline{RQ}/\overline{GT}$ line (if HLDA is held high on reset).

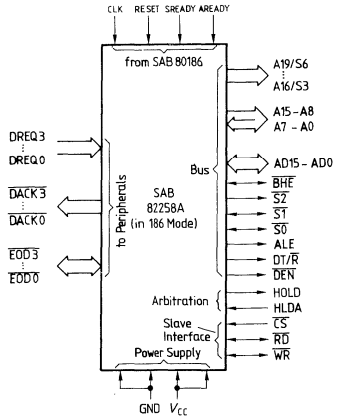
Logic Symbol in 286 Mode



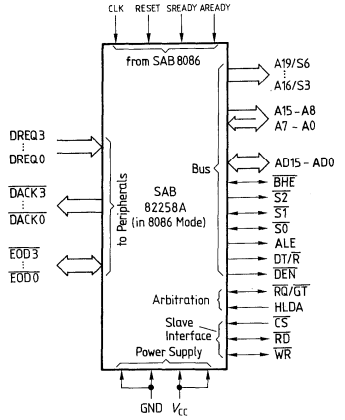
Logic Symbol in Remote Mode



Logic Symbol in 186 Mode



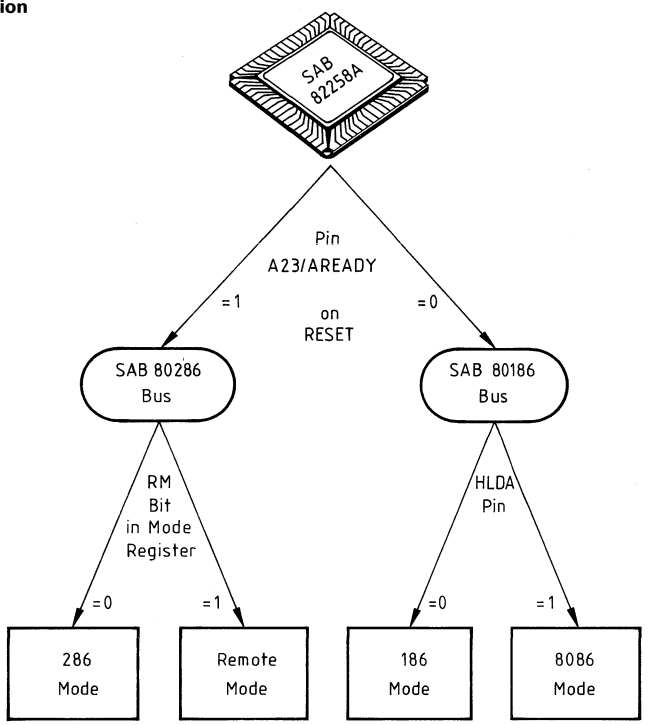
Logic Symbol in 8086 Mode



The SAB 82258A can also be operated in remote or standalone mode, in which case it is not coupled directly to a processor. In remote mode, the SAB 82258A can be operated as sole bus master in a multimaster environment.

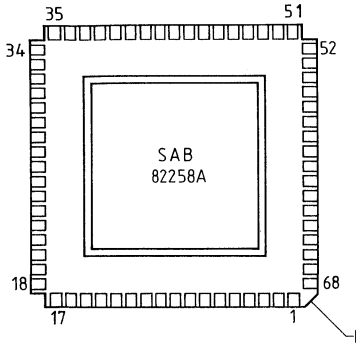
The SAB 82258A is programmed to a specific mode of operation by applying defined logic levels to certain pins during reset and by setting the status of several control bits (see figure below).

Mode Selection

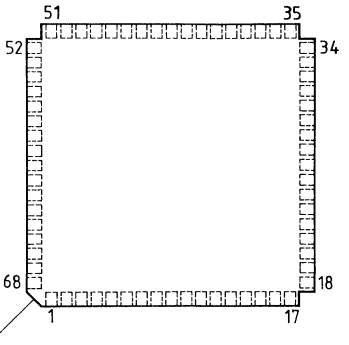


Pin Configuration

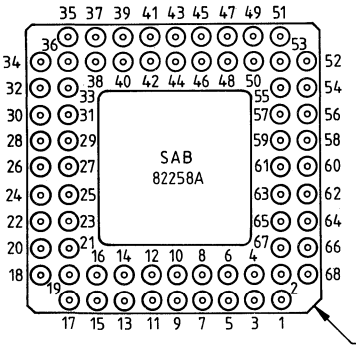
CLCC 68
Pad view



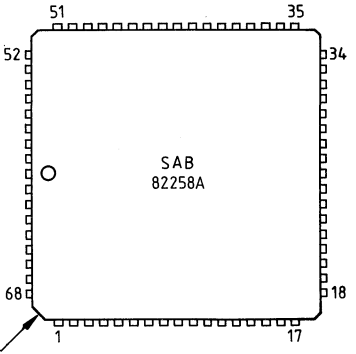
CLCC 68
PC board view



PGA 68
Bottom view



PLCC 68
Top view



Note: The PGA footprint is identical with the CLCC socket and PLCC socket footprints (as viewed from component side of pc board).

Pin Definitions and Functions

Some pins of the SAB 82258A serve for different purposes according to the different modes of bus operation. The table below summarizes the pinouts of the SAB 82258A in the various modes. A detailed description of the general pin functions as well as the mode-specific pin functions is given in the following sections.

Pin	286 Mode		Remote Mode		186/8086 Mode	
	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)
16	HOLD	O	HOLD	O	HOLD or $\overline{RQ}/\overline{GT}$	O (186) I/O (8086)
17	HLDA	I	HLDA	I	HLDA	I
1	$\overline{BHE}$	I/O	$\overline{BHE}$	I/O	$\overline{BHE}$	I/O
14	M/$\overline{IO}$	O	BREL	O	$\overline{S2}$	O
11	$\overline{S1}$	I/O	$\overline{S1}$	O	$\overline{S1}$	I/O
13	$\overline{S0}$	I/O	$\overline{S0}$	O	$\overline{S0}$	I/O
8	$\overline{CS}$	I	$\overline{CS}$	I	$\overline{CS}$	I
2	$\overline{RD}$	I	$\overline{RD}$	I	$\overline{RD}$	I/O
3	$\overline{WR}$	I	$\overline{WR}$	I	$\overline{WR}$	I/O
10	$\overline{READY}$	I	$\overline{READY}$	I	SREADY	I
59	A23	O	A23	O	AREADY	I
58	A22	O	A22	O	ALE	O
57	A21	O	A21	O	DT/$\overline{R}$	O
56	A20	O	A20	O	$\overline{DEN}$	O
55	A19	O	A19	O	A19/S6	O
54	A18	O	A18	O	A18/S5	O
53	A17	O	A17	O	A17/S4	O
52	A16	O	A16	O	A16/S3	O
51	A15	O	A15	O	A15	O
50	A14	O	A14	O	A14	O
49	A13	O	A13	O	A13	O
48	A12	O	A12	O	A12	O
47	A11	O	A11	O	A11	O
46	A10	O	A10	O	A10	O
45	A9	O	A9	O	A9	O
44	A8	O	A8	O	A8	O
42	A7	I/O	A7	I/O	A7	I/O
41	A6	I/O	A6	I/O	A6	I/O
40	A5	I/O	A5	I/O	A5	I/O
39	A4	I/O	A4	I/O	A4	I/O
38	A3	I/O	A3	I/O	A3	I/O
37	A2	I/O	A2	I/O	A2	I/O
36	A1	I/O	A1	I/O	A1	I/O
35	A0	I/O	A0	I/O	A0	I/O

Pin Definitions and Functions (cont'd)

Pin	286 Mode		Remote Mode		186/8086 Mode	
	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)	Symbol	Input (I) Output (O)
18	D15	I/O	D15	I/O	AD15	I/O
20	D14	I/O	D14	I/O	AD14	I/O
22	D13	I/O	D13	I/O	AD13	I/O
24	D12	I/O	D12	I/O	AD12	I/O
27	D11	I/O	D11	I/O	AD11	I/O
29	D10	I/O	D10	I/O	AD10	I/O
31	D9	I/O	D9	I/O	AD9	I/O
33	D8	I/O	D8	I/O	AD8	I/O
19	D7	I/O	D7	I/O	AD7	I/O
21	D6	I/O	D6	I/O	AD6	I/O
23	D5	I/O	D5	I/O	AD5	I/O
25	D4	I/O	D4	I/O	AD4	I/O
28	D3	I/O	D3	I/O	AD3	I/O
30	D2	I/O	D2	I/O	AD2	I/O
32	D1	I/O	D1	I/O	AD1	I/O
34	D0	I/O	D0	I/O	AD0	I/O
7	DREQ0	I	DREQ0	I	DREQ0	I
6	DREQ1	I	DREQ1	I	DREQ1	I
5	DREQ2	I	DREQ2	I	DREQ2	I
4	DREQ3	I	DREQ3	I	DREQ3	I
61	$\overline{\text{DACK0}}$	O	$\overline{\text{DACK0}}$	O	$\overline{\text{DACK0}}$	O
62	$\overline{\text{DACK1}}$	O	$\overline{\text{DACK1}}$	O	$\overline{\text{DACK1}}$	O
63	$\overline{\text{DACK2}}$	O	$\overline{\text{DACK2}}$	O	$\overline{\text{DACK2}}$	O
64	$\overline{\text{DACK3}}$	O	$\overline{\text{DACK3}}$	O	$\overline{\text{DACK3}}$	O
65	$\overline{\text{EOD0}}$	I/O	$\overline{\text{EOD0}}$	I/O	$\overline{\text{EOD0}}$	I/O
66	$\overline{\text{EOD1}}$	I/O	$\overline{\text{EOD1}}$	I/O	$\overline{\text{EOD1}}$	I/O
67	$\overline{\text{EOD2}}$	I/O	$\overline{\text{EOD2}}$	I/O	$\overline{\text{EOD2}}$	I/O
68	$\overline{\text{EOD3}}$	I/O	$\overline{\text{EOD3}}$	I/O	$\overline{\text{EOD3}}$	I/O
15	RESET	I	RESET	I	RESET	I
12	CLK	I	CLK	I	CLK	I
9,43	GND	–	GND	–	GND	–
26,60	V_{CC}	–	V_{CC}	–	V_{CC}	–

Pin Definitions for All Operating Modes

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{BHE}$</td><td>1</td><td>I/O</td><td>$\overline{BUS\ HIGH\ ENABLE}$
Indicates transfer of data on the upper byte of the data bus, D15 to D8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is active low and floats to tristate off when the SAB 82258A does not own the bus.
$\overline{BHE}$ and A0 encodings
<table>
<tr><th>$\overline{BHE}$</th><th>A0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Word transfer (D15–D0)</td></tr>
<tr><td>0</td><td>1</td><td>Byte transfer on upper half of data bus (D15–D8)</td></tr>
<tr><td>1</td><td>0</td><td>Byte transfer on lower half of data bus (D7–D0)</td></tr>
<tr><td>1</td><td>1</td><td>Odd-addressed byte on 8-bit bus (D7–D0)</td></tr>
</table></td></tr>
<tr><td>$\overline{RD}$</td><td>2</td><td>I</td><td>$\overline{READ}$
This command in conjunction with chip select enables reading out of the SAB 82258A register which is addressed by the address lines A7 to A0. This signal can be asynchronous to the SAB 82258A clock.</td></tr>
<tr><td>$\overline{WR}$</td><td>3</td><td>I</td><td>$\overline{WRITE}$
This command is used for writing into SAB 82258A registers. This signal can be asynchronous to the SAB 82258A clock.</td></tr>
<tr><td>DREQ0-
DREQ3</td><td>4-7</td><td>I</td><td>DMA REQUEST (0 TO 3)
These input signals are used for synchronized DMA transfers. DREQ3 has the meaning of I/O request (IOREQ) if channel 3 is a multiplexer channel. These signals can be asynchronous to the SAB 82258A clock.</td></tr>
<tr><td>$\overline{CS}$</td><td>8</td><td>I</td><td>$\overline{CHIP\ SELECT}$
Is used to enable the access of a processor to SAB 82258A registers. This access is additionally controlled either by bus status signals or by the read or write command signals. Chip select can be asynchronous to the SAB 82258A clock.</td></tr>
<tr><td>CLK</td><td>12</td><td>I</td><td>CLOCK
It provides the fundamental timing. In 286 mode and remote mode it must be two times the system clock. It can be directly connected to the SAB 82284 CLK output. It is divided by two to generate the SAB 82258A internal clock. The on-chip divide-by-two circuitry can be synchronized to the external clock generator by a low-to-high transition on the RESET input, or by first high-to-low transition on the status inputs $\overline{S0}$ or $\overline{S1}$ after reset. In 186/8086 mode no internal prescaling is done.</td></tr>
</table>

Pin Definitions for All Operating Modes (cont'd)

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{S0}$, $\overline{S1}$</td><td>11, 13</td><td>I/O</td><td>BUS STATUS LINES (0, 1)
These signals control the support circuits. The beginning of a bus cycle is indicated by $\overline{S1}$ or $\overline{S0}$ or both going active. The termination of a bus cycle is indicated by all status signals going inactive in 186 mode or bus ready signal ($\overline{READY}$) going active in 286 mode. The type of bus cycle is indicated by $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ (in 186 mode) or M/$\overline{IO}$ (in 286 mode). $\overline{S2}$ and M/$\overline{IO}$ have the same meaning but in 186 mode the $\overline{S2}$ signal can be active only when at least one of $\overline{S1}$ or $\overline{S0}$ is active, whereas in 286 mode the M/$\overline{IO}$ signal is valid with the address on the address lines. The SAB 82258A can generate the following bus cycles by activating the status signals (and M/$\overline{IO}$ in 286 mode):
<table>
<tr><th>M/$\overline{IO}$ or $\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Cycle Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Read I/O-vector (for multiplexer channel)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read from I/O space</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write into I/O space</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>No bus cycle, does not occur in 186 mode</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Does not occur</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read from memory space</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write into memory space</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>No bus cycle</td></tr>
</table>
When the SAB 82258A is not the master of the local bus the status signals are used as inputs for detection of synchronous accesses to the SAB 82258A. The following table shows the bus status and $\overline{CS}$, signals and their interpretation by the SAB 82258.
<table>
<tr><th>$\overline{CS}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Description</th></tr>
<tr><td>1</td><td>X</td><td>X</td><td>SAB 82258A is not selected (no action)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No SAB 82258A access (no action)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read from an SAB 82258A register</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write into an SAB 82258A register</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>No bus cycle (note 1)</td></tr>
</table>
Note 1: SAB 82258A is selected but no synchronous access is activated. In this case the SAB 82258A monitors $\overline{RD}$ and $\overline{WR}$ signals for detection of an asynchronous access.</td></tr>
<tr><td>RESET</td><td>15</td><td>I</td><td>SYSTEM RESET
An activation of the reset signal forces the SAB 82258A to the initial state. The reset signal must be synchronous to CLK.</td></tr>
</table>

Pin Definitions for All Operating Modes (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{DACK0}$-$\overline{DACK3}$	61–64	O	$\overline{DMA\ ACKNOWLEDGE}$ (0 TO 3) Acknowledges the requests on the related DREQn signal. It is activated when the requested transfer(s) is (are) performed. If the channel 3 is a multiplexer channel the signal $\overline{DACK3}$ has the meaning of I/O acknowledge ($\overline{IOACK}$).
$\overline{EOD0}$-$\overline{EOD3}$	65–68	I/O	$\overline{END\ OF\ DMA}$ (0 TO 3) These signals are implemented as open drain output drivers with a high impedance pullup resistor and thus can be used as bidirectional lines. As **outputs** the signals are activated for two system clock cycles at the end of the DMA transfer of the corresponding channel (if enabled) or they are activated under program control (EOD output or interrupt output). If the signals are held internally high but forced to low by external circuitry, they act as "End of DMA" **inputs**. The current transfer is aborted and the SAB 82258A continues with the next command. Additionally, a special function is possible with the $\overline{EOD2}$ pin: this pin can also be used as common interrupt signal for all 4 channels. In this mode this signal is not an open drain output but a pushpull output (output only). The other $\overline{EOD}$ pins may be used as $\overline{EOD}$ outputs/inputs as described above.
V_{CC}	26,60		POWER SUPPLY (+5 V)
GND	9,43		GROUND (0 V)

Pin Definitions for 286 Mode and Remote Mode

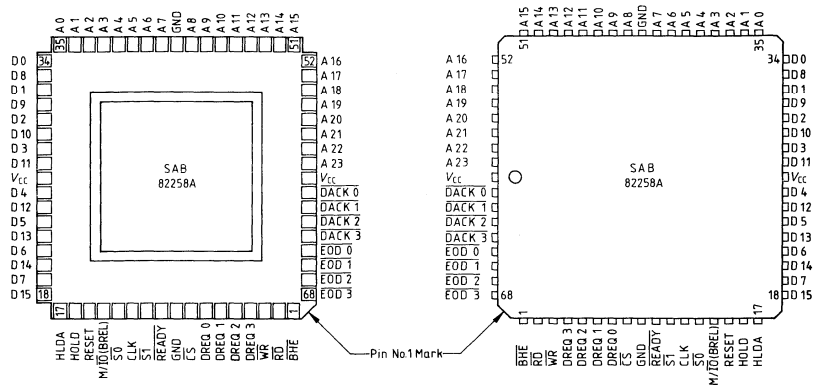
In 286 mode the SAB 82258A bus signals and bus timings are the same as for the SAB 80286 processor. Additional features of the SAB 82258A require a slight change in pin definitions. The processor can access internal registers of the SAB 82258A. Therefore the bus signals must support these accesses. This means that some of the bus control signals must be bidirectional and some additional bus control signals are necessary. All additional pins and their functions are listed below.

In **remote mode** most of the bus signals are the same as in 286 mode. Pin 14 (M/$\overline{IO}$) serves as BREL output. The HOLD/HLDA arbitration in remote mode is used only for system bus accesses, the resident bus is accessed directly.
The $\overline{CS}$ input additionally requests access to the local bus of the SAB 82258A. These accesses are enabled through the BREL output after the SAB 82258A has released the bus.

Pin Configuration in 286 Mode and Remote Mode

Component Pad View – As viewed from underside of component when mounted on the board (Example: CLCC 68)

PC Board View – As viewed from the component side of the pc board (Example: PLCC 68)



Pin Definitions for 286 Mode and Remote Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{READY}}$	10	I	$\overline{\text{BUS READY}}$ Terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{\text{READY}}$ low. $\overline{\text{READY}}$ is an active low synchronous input requiring setup and hold times relative to the system clock to be met for correct operation.
M/$\overline{\text{IO}}$	14 (286 mode)	O	MEMORY/ $\overline{\text{I/O}}$ SELECT In 286 mode, pin 14 is used to distinguish between memory and I/O space addresses.
BREL	14 (remote mode)	O	BUS RELEASE In remote mode pin 14 is used to indicate when the SAB 82258A has released the control of the local bus.
HOLD	16	O	BUS HOLD REQUEST When true, indicates a request for control of the local bus (286 mode) or the system bus (remote mode). When the SAB 82258A relinquishes the bus it drops the HOLD output. HOLD is connected to the bus arbiter in remote mode.
HLDA	17	I	BUS HOLD ACKNOWLEDGE When true, indicates that the SAB 82258A can acquire the control of the bus. When it goes low SAB 82258A must relinquish the bus at the end of its current cycle. HLDA can be asynchronous to the SAB 82258A clock. HLDA is connected to the bus arbiter in remote mode.
D0-D15	18-25, 27-34	I/O	DATA BUS (0 TO 15) This is the bidirectional 16-bit data bus. For use with an 8-bit bus, only the lower 8 data lines D7-D0 are relevant.
A0-A7	35-42	I/O	ADDRESS BUS (0 TO 7) The lower 8 address lines for DMA transfers. They are also used to input the register address when the processor accesses an SAB 82258A register.
A8-A23	44-59	O	ADDRESS BUS (8 TO 23) Higher address outputs.

Pin Definitions for 186 Mode and 8086 Mode

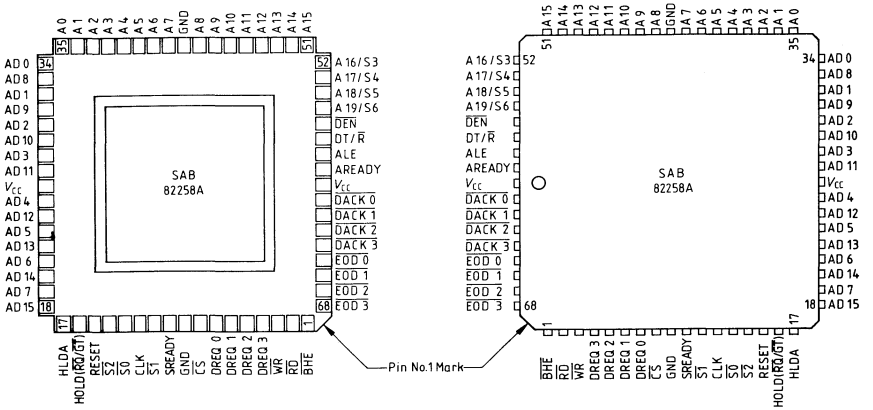
In 186 mode and 8086 mode the SAB 82258A multiplexes the address with data and additional status lines.
Pins A0 to A15 retain their original function while pins A20 to A23 serve for different purposes (not used for address in 186/8086 mode).

The $\overline{RD}$ and $\overline{WR}$ lines are additionally used as outputs in 186/8086 mode to support minimum mode systems.
Note that the HLDA input can be used to force the SAB 82258A off the bus in 8086 mode, even though the arbitration is done via the $\overline{RQ}/\overline{GT}$ line!

Pin Configuration in 186 Mode and 8086 Mode

Component Pad View – As viewed from underside of component when mounted on the board (Example: CLCC 68)

PC Board View – As viewed from the component side of the pc board (Example: PLCC 68)



Pin Definitions for 186 Mode and 8086 Mode (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
ALE	58	O	ADDRESS LATCH ENABLE This signal provides a strobe to separate the address information on the multiplexed AD lines.
$\overline{DEN}$	56	O	$\overline{DATA\ ENABLE}$ This signal is used for enabling the data transceiver.
DT/$\overline{R}$	57	O	DATA TRANSMIT/$\overline{RECEIVE}$ This signal controls the direction of the data transceivers. When low, data is transferred to the SAB 82258A, when high the ADMA places data onto the data bus.
$\overline{S2}$	14	O	$\overline{STATUS\ LINE\ 2}$ Signal as for SAB 186/8086/88 processors (see also $\overline{S1}$, $\overline{S0}$ description in 286 mode).
AREADY	59	I	ASYNCHRONOUS READY The rising edge of this signal is internally synchronized, the falling edge must be synchronous to CLK. During reset this signal must be low for entering the 186 mode.
SREADY	10	I	SYNCHRONOUS READY This signal must be synchronized externally. The use of this pin permits a relaxed system-timing specification by eliminating the clock phase which is required for resolving the signal level when using the AREADY input.
CLK	12	I	SYSTEM CLOCK This is the input for the one time system clock. No internal prescaling is done.
AD0–AD15	18–25 27–34	I/O	ADDRESS/DATA BUS (0 TO 15) Lower address and data information is multiplexed on pin AD0 to AD 15. Additionally the demultiplexed address information is available on address pin A0 to A15.
A0–A7 A8–A15	35–42 44–51	I/O O	
A16/S3–A19/S6	52, 55	O	ADDRESS BUS (16 TO 19) / STATUS LINES (3 TO 6) The higher address bits are multiplexed with additional status information.
HLDA	17	I	BUS HOLD ACKNOWLEDGE When true, indicates that the SAB 82258A can acquire the control of the bus. When it goes low the SAB 82258A must relinquish the bus at the end of its current bus cycle. HLDA can be asynchronous to the SAB 82258A clock. In 8086 mode, HLDA can be used to force the SAB 82258A off the bus.
HOLD	16 (186 mode)	O	BUS HOLD REQUEST When true, indicates a request for control of the bus. When the SAB 82258A relinquishes the bus, it drops the HOLD output.
$\overline{RG/GT}$	16	I/O	$\overline{REQUEST/GRANT}$ In 8086 mode the HOLD output acts as $\overline{REQUEST/GRANT}$ line. The $\overline{REQUEST/GRANT}$ protocol implements a one-line communication dialog required to arbitrate the use of the system bus normally done via HOLD/HLDA. The $\overline{RG/GT}$ signal is active low and has an internal pullup resistor.

Functional Description

General

The SAB 82258A is an advanced general-purpose DMA controller especially tailored for efficient high-speed data transfers on an SAB 80286 as well as on an SAB 80186/188 or SAB 8086/88 bus.
It supports two basic operating modes:

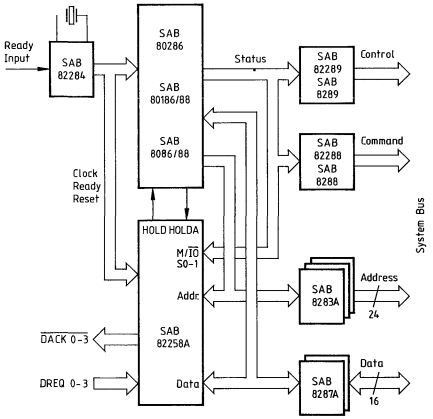
– local mode (tightly coupled to a processor) and
– remote mode (loosely coupled to a processor).

In the first case the SAB 82258A is directly coupled to the CPU and uses the same system support/ control devices as the CPU (see figure a) below). This mode is possible with the above-mentioned processors.

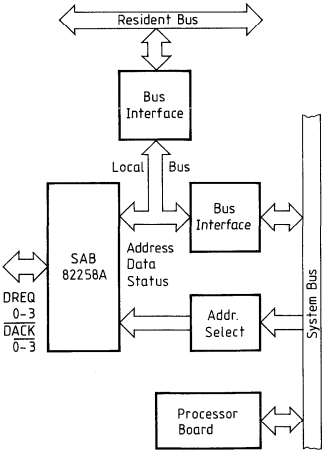
As a second basic operating mode a remote (standalone) mode is supported (see figure b) below). Here the SAB 82258A has his own sets of bus interface circuits and thus can dispose of its own local bus. This allows the DMA controller to work in parallel with the main CPU and therefore overall system performance could be increased. Besides, this mode is very useful for the design of modular systems and allows connecting the SAB 82258A to any other processor via the system bus independent of the processor's unique local bus.

Basic ADMA Operating Modes

a) Local Mode



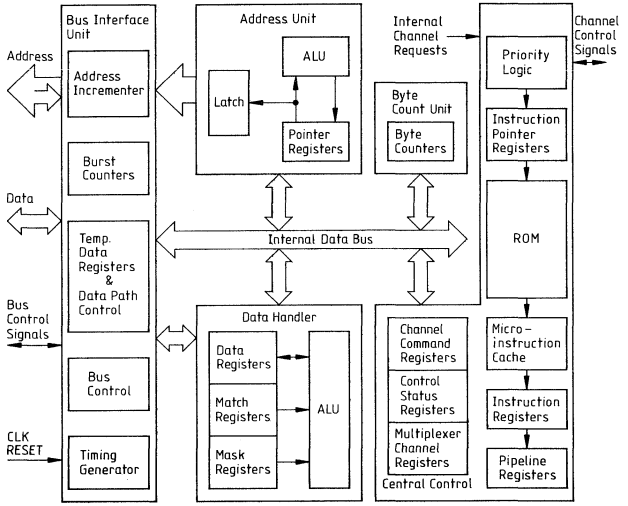
b) Remote Mode



The SAB 82258A has four independent DMA channels that can transfer up to 10 Mbytes/s in the single cycle mode (2 clocks/transfer). In the 2-cycle transfer mode the maximum rate is 5 Mbytes/s. Switching between channels induces no time penalty. Thus the overall maximum transfer rate of 10 Mbytes/s is also valid for multiple channel operation.

This fast operation is possible because of the pipelined architecture of the SAB 82258A that allows the different function units to work in parallel. The maximum transfer rate can be doubled to 20 Mbytes/s (in a 10 MHz system), if the ADMA executes 32-bit fly-by transfers.

Block Diagram of SAB 82258A



The ADMA supports two address spaces, memory space and I/O space, each with a maximum address range of 16 Mbytes. In addition, the maximum block length (byte count) is also 16 Mbytes to support applications where large blocks of data have to be transferred (e.g. graphics).

As source or as destination, four parameters can be selected independently:

- address space (memory or I/O)
- physical bus width (8 bits or 16 bits),
- logical bus width (same as physical bus width or 8 bits on a 16-bit physical bus)
  and
- transfer direction (increasing, decreasing, fixed pointer or constant value).

If the physical bus width of source or destination does not meet the logical bus width an automatic byte/word assembly (word/byte disassembly) takes place if this minimizes the necessary transfers. The same is true if the logical bus widths of source and destination are different.
Transfers between different address spaces can be performed within one cycle or in two cycles, transfers within one address space can be performed only in two cycles.

The transfers can be executed free running or externally synchronized via DREQ where source or destination synchronization is possible.

In summary, this very symmetrical operation of the SAB 82258A gives the user a great amount of design flexibility.

Adaptive Bus Interface

As shown in the figure on page 3, the SAB 82258A bus interface has two basic timing modes: the 286 mode and the 186 mode. In 286 mode the SAB 82258A is directly coupled to an SAB 80286, in 186 mode to an SAB 80186 or SAB 80188. For each of these two modes a slightly different variation exists:

- For the 286 mode, the remote mode, where the ADMA operates as a bus master on the system bus without being directly coupled to a processor. In this mode the SAB 82258A can dispose of its own local bus and the communication with the main processor is done via the system bus. To enable access to ADMA registers by the main processor, the SAB 82258A must release its local bus. This "local bus arbitration" in remote mode is done via the $\overline{CS}$ and BREL lines.
- For the 186 mode the variation is the 8086 mode where the SAB 82258A supports the $\overline{RQ}/\overline{GT}$ protocol and thus can be directly coupled to an SAB 8086 or SAB 8088.

Memory-Based Communication

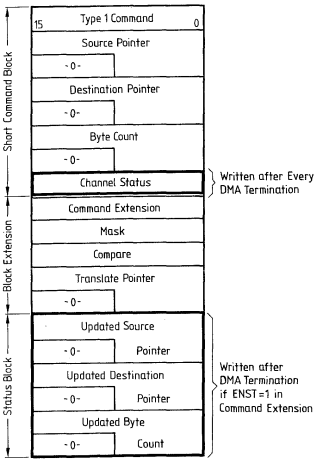
The normal communication between the ADMA and the processor is memory-based. This means that all necessary data for a transfer is contained in a command block in memory accessible for CPU and SAB 82258A (see figure on next page). To start the transfer the CPU loads one of the command pointer registers of the SAB 82258A with the address of the command block and then gives a "start channel command". Getting the command the SAB 82258A loads the entire command block from memory into its on-chip channel registers and executes it.
On completing the operation, channel status information is written back by the SAB 82258A into the channel status word contained in the command block in memory. If desired the actual contents of the channel registers, i.e. source pointer, destination pointer and byte count is transferred into the channel status block. The channel status block immediately follows the command block in memory (see figure on next page).

Command Chaining

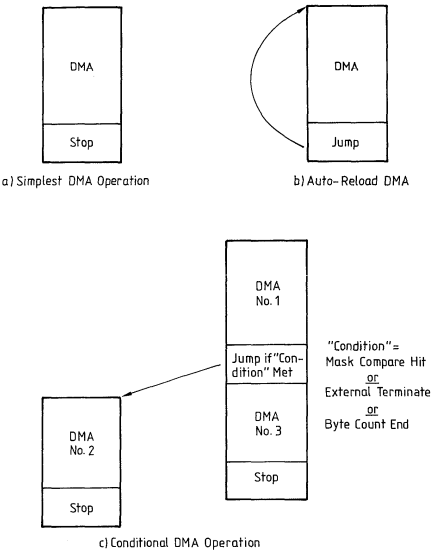
Command blocks for any channel can be chained for sequential execution (see next figure). When the SAB 82258A has completed the execution of a command, it automatically increments the command pointer, and starts to fetch and execute the next command block until a stop command is found. As a result a chain of command blocks can be executed by the ADMA without any CPU intervention. Due to conditional and unconditional STOP and JUMP commands, quite complex sequences of DMA can be executed by the SAB 82258A.

Memory-Based Communication and Command Chaining

Memory-Based Communication



Command Chaining



Data Chaining

Data chaining permits an automatic, dynamic linking of data blocks scattered in memory. There are two types: list and linked-list data chaining.

If for a DMA the source blocks are to be dynamically linked during DMA it is called source chaining and the effect is that of gathering data blocks and sending them out effectively as one block.

If one source block is dynamically broken up into multiple destination blocks, it is called destination chaining. This results in scattering of a block.

This dynamic linking and unlinking of data blocks makes the logical sequencing of data independent of its physical sequencing in memory.

In the case of linked list chaining (see figure a on following page) each data block has a descriptor containing information on position of data block in memory, length of data block, and a pointer to the next descriptor.

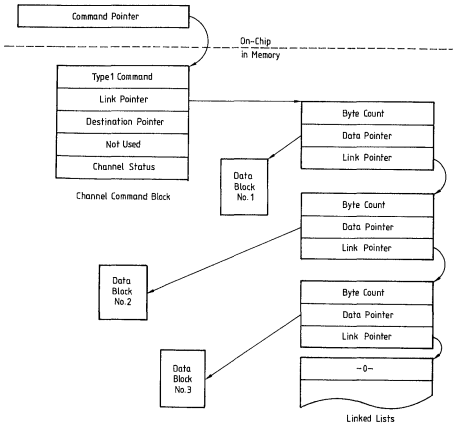
During data transfer the data block 1 is sent out first, then 2 and so on till a 0 is encountered in the byte count field.

The second type of data chaining is list chaining (see figure b on following page).

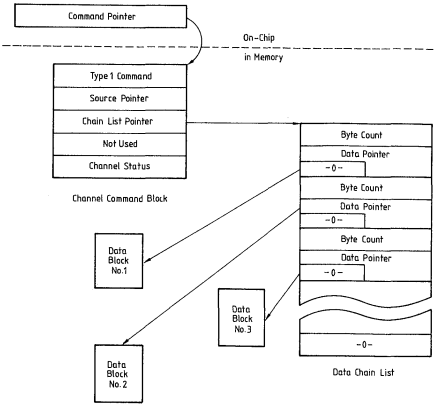
Unlike linked list chaining, here the data block descriptors are continuous in a block and thus determine the sequence of data blocks. The flexibility lost in terms of predefined sequence is gained in terms of linking time.

Data Chaining

a) Linked List Chaining



b) List Chaining



"On-The-Fly" Operations

A normal DMA controller blindly transfers data from source to destination without looking at the data. In case of the ADMA on-the-fly operations are executed during the DMA transfer and allow inspection and/or operation on the transferred data. There are three possible on-the-fly operations:

- mask/compare,
- translate and
- verify

During a mask/compare operation each byte/word transferred is compared to a given pattern. One or more bits can be masked and thus do not contribute to the result of the compare operation. The result can be used by subsequent conditional stop or jump operations.

For translate operation the byte (no word possible) that is fetched from source is added to a translate pointer to build the effective source pointer. The byte pointed to by this pointer is then fetched and sent out to the destination. Of course, a mask/compare operation is possible on the byte sent out.

The verify operation is a type of block compare operation to compare each byte/word of a data read from a peripheral with the one in a data block in the memory. There are three options:

1. Verify with no termination on mismatch (2-cycle transfer only)
2. Verify with termination on mismatch (2-cycle transfer only).
3. Verify and save (single cycle transfer only). Here an actual transfer with compare takes place. The transfer is not stopped on mismatch.

Multiplexer Channel

When programmed to multiplexer mode, channel 3 (supported by a multiplexer logic) can be used to service up to 32 subchannel request lines (see figure below and on next page). Thus it is ideally suited to service a large number of comparatively slow equipment like CRT terminals, line printers, etc. Since multiple subchannels are processed with the resource of one DMA channel, the overhead of subchannel switching, of course, decreases the total effective throughput on the multiplexer channel.

To allow efficient control even of the subchannels, a separate command pointer for each subchannel is provided within the multiplexer table. Thus an individual subchannel program (command chain) can be used for each subchannel.

Different transfer modes are provided for subchannels:

Byte/word multiplex:
One byte or word is transferred per request. Updating the pointers is done within the actual command block.

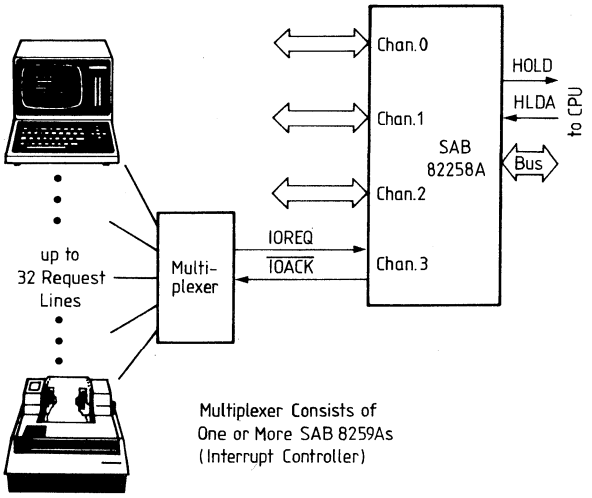
Single transfer:
Similar to byte/word multiplex, but with execution of command chaining after each transfer.

Block multiplex:
I/O request initiates execution of a complete command block, i.e. the complete data block specified is transferred. This allows maximum transfer rates (2-cycle transfers) also for subchannels.

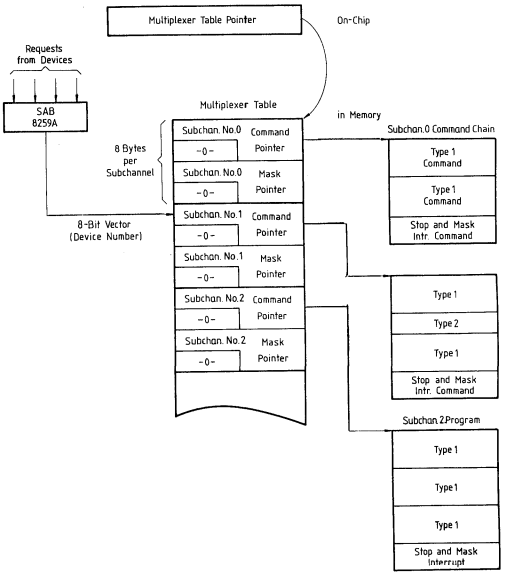
A type 2 command in a subchannel program can issue an interrupt, whereby the multiplexer channel interrupt vector register (MIVR) provides the corresponding subchannel number for the CPU.

A subchannel program is terminated by a stop and mask command which automatically masks the corresponding request line within the SAB 8259A thus blocking this subchannel until it is enabled again by the CPU.

Multiplexer Channel



Structure of Multiplexer Table



The mask pointer is the address of the appropriate SAB 8259A mask register.

32-Bit Fly-by Transfers

The 32-bit transfer enable bit TR32 (bit 6 of the channel command register extension CCRX) allows the address pointers and byte counters to be modified not only by 1 or 2, but also by 4 in order to count 32-bit double words. Therefore, the SAB 82258A can control 32-bit transfers in single-cycle mode. In this mode, data flows past the DMA controller rather than through it. All features that use the data assembly registers (two-cycle mode, compare, verify, etc.), should be avoided, because the 16-bit data port can access only one half of a 32-bit data bus. Addresses and byte counts must be aligned to double-word boundaries (i.e. multiples of 4) in order to ensure proper operation. Also the effective transfer width (logical and physical bus width) must be programmed to 16 bits. As the external control signals do not allow to distinguish 32-bit fly-by transfers from 16-bit transfers, the transfer mode of a channel must be predefined.

Note:
If the SAB 82258A is to operate in a system with a true 32-bit address bus, the upper address byte (A31 to A24) must be provided by an external page register, as the ADMA's address bus is still 24 bits wide.

Operating the SAB 82258A

Reset

When activating the reset input, the SAB 82258A is forced into its initial state. All channels and bus activities are stopped, tristate lines are tristated and the others enter the inactive state.
While the reset input is active, line A23/AREADY and HLDA must be forced to the appropriate levels to select the desired bus interface mode (see figures on page 3, 40 and 52).
After deactivating reset the inactive state is maintained, in addition the state of the SAB 82258A registers is as follows:

- general mode register, general burst register, general delay register, general status register and the four channel status registers are set to zero,
- the vector-not-valid bit of the multiplexer interrupt vector register is set to 1,
- all other registers and bits are undefined.

Note that the general mode register (GMR) should be loaded first to select the mode of operation before any other activity is started on the ADMA.

DMA Interface

The DMA interface consists of three lines:

- DREQ – DMA request,
- $\overline{\text{DACK}}$ – DMA acknowledge and
- $\overline{\text{EOD}}$ – end of DMA

The first two lines work as request and acknowledge lines to control synchronized DMA transfers as known from conventional DMA controllers.

A special feature of the SAB 82258A are the bidirectional $\overline{\text{EOD}}$ lines. Firstly they can be used as inputs to receive an asynchronous external terminate signal to terminate a running DMA. Secondly, as an output, they can be used to send out a pulse which interrupts the CPU and/or signals to the peripheral a specific status (e.g. transfer aborted, or end of a block, or send/receive next block ...).

The $\overline{\text{EOD}}$ output signal can be generated synchronously to a transfer (during the last transfer) or asynchronously to the transfers by a specific command.

In addition the $\overline{\text{EOD}}$ output of channel 2 can be used as a collective interrupt output for all DMA channels while the other three retain their normal function.

Slave Interface

The slave interface is used to access the SAB 82258A internal registers. Although nearly all of the communication between CPU and ADMA is done via memory-based data blocks, some direct accesses to ADMA registers are necessary. For example during the initialization phase the general mode register must be written, or to start a channel the command pointer register and the general command register must be loaded. Also during the debugging phase it is of great benefit to have access to all of the SAB 82258A internal registers.

The slave interface is enabled by the $\overline{\text{CS}}$ input and consists of the following lines:

- $\overline{\text{S0}}$, $\overline{\text{S1}}$ – status lines (inputs)
- $\overline{\text{RD}}$, $\overline{\text{WR}}$ – control lines (inputs)
- A0–A7 – register address (inputs)
- D0–D15 – data lines (inputs/outputs) and
- AD0–AD15 – address/data lines (inputs/outputs) for synchronous access in 186 mode

Note, that all of these lines are outputs if the SAB 82258A is an active bus master.

In 186 mode and 286 mode two types of accesses are possible:

- Synchronous access by means of the status lines. Processor and SAB 82258A are directly coupled and must use the same clock.
- Asynchronous access by using the control lines $\overline{\text{RD}}$ and $\overline{\text{WR}}$ (processor and ADMA may have different clocks).

In all modes except the synchronous access in 186 mode the register address must be supplied on address pins A0 to A7. Using synchronous access in 186 mode the address information is expected at address/data lines AD0 to AD7.

In remote mode only the asynchronous access is possible because the SAB 82258A first has to release its local bus to enable the register access. On receiving an access request (activation of $\overline{\text{CS}}$ input) the SAB 82258A releases its local bus as soon as possible and signals this by activating the BREL line. Now the CPU can accomplish its access.

Bus Arbitration

To arbitrate access to the bus between the ADMA and the processor, the signals HOLD and HLDA serve for communication. Normally the ADMA competes for the bus via HOLD, the processor grants access to the bus via HLDA. The HLDA signal can also be deactivated in order to force the ADMA off the bus for a certain reason (kick off). After reactivation of HLDA, the ADMA will again get control of the bus.
In 8086 mode this communication is done by pulses via a single $\overline{\text{RQ}}/\overline{\text{GT}}$ line which uses the HOLD pin. In this case normally the HLDA input has no

function. Nevertheless, even in 8086 mode the HLDA input can be used for kick-off. This provides some kind of additional bus arbitration.

Register Set

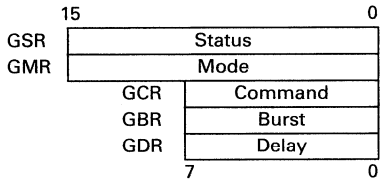
The following figure shows the user visible registers of the SAB 82258A. A set of 5 registers, called the general registers, is used for all the 4 channels. The mode register is being written to first after reset and it describes the SAB 82258A environment – bus widths, priorities, etc. The general command register (GCR) is used to start and stop the DMA transfer on different channels. The general status register (GSR) shows the status of all the 4 channels; if the channel is running, if interrupt is pending, etc. General burst register (GBR) and general delay register (GDR) are used to specify the bus load which is permissible for the SAB 82258A.

There is a set of channel registers for each of the 4 channels. Most channel registers serve as cache registers and need to be accessed only for debugging. During normal operation they are loaded automatically by the SAB 82258A (see next paragraph).

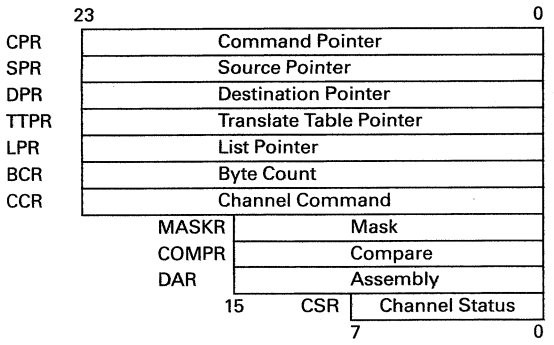
The layout of register addresses is shown in the figure on the next page. All register addresses are even. Locations not designated in that figure are reserved and should not be used.

SAB 82258A Register Set

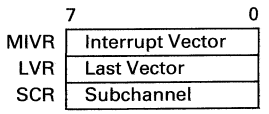
General Registers



Channel Registers (4 sets; 1 per channel)



Multiplexer Channel Registers



Register Address Arrangement

Address Bits 0–5	Address Bits 7, 6 00	01	10	11
0	GCR			
2	SCR			
4	GSR			
6				
8	GMR			
A	GBR			
C	GDR			
E				
10	CSR 0	CSR 1	CSR 2	CSR 3
12	DAR 0	DAR 1	DAR 2	DAR 3
14	MASKR 0	MASKR 1	MASKR 2	MASKR 3
16	COMPR 0	COMPR 1	COMPR 2	COMPR 3
18				MIVR
1A				LVR
1C				
1E				
20	CPR L0	CPR L1	CPR L2	CPR L3
22	CPR H0	CPR H1	CPR H2	CPR H3
24	SPR L0	SPR L1	SPR L2	SPR L3
26	SPR H0	SPR H1	SPR H2	SPR H3
28	DPR L0	DPR L1	DPR L2	DPR L3
2A	DPR H0	DPR H1	DPR H2	DPR H3
2C	TTPR L0	TTPR L1	TTPR L2	TTPR L3
2E	TTPR H0	TTPR H1	TTPR H2	TTPR H3
30	LPR L0	LPR L1	LPR L2	LPR L3/MTPR L
32	LPR H0	LPR H1	LPR H2	LPR H3/MTPR H
34				
36				
38	BCR L0	BCR L1	BCR L2	BCR L3
3A	BCR H0	BCR H1	BCR H2	BCR H3
3C	CCR L0	CCR L1	CCR L2	CCR L3
3E	CCR H0	CCR H1	CCR H2	CCR H3

GCR = General Command Register
SCR = Subchannel Register
GSR = General Status Register
GMR = General Mode Register
GBR = General Burst Register
GDR = General Delay Register
CSR = Channel Status Register
DAR = Data Assembly Register
MASKR = Mask Register
COMPR = Compare Register
MIVR = Multiplexer Interrupt Vector Register
LVR = Last Vector Register
CPR = Command Pointer Register
SPR = Source Pointer Register
DPR = Destination Pointer Register
TTPR = Translate Table Pointer Register
LPR = List Pointer Register
MTPR = Multiplexer Table Pointer Register
BCR = Byte Count Register
CCR = Channel Command Register

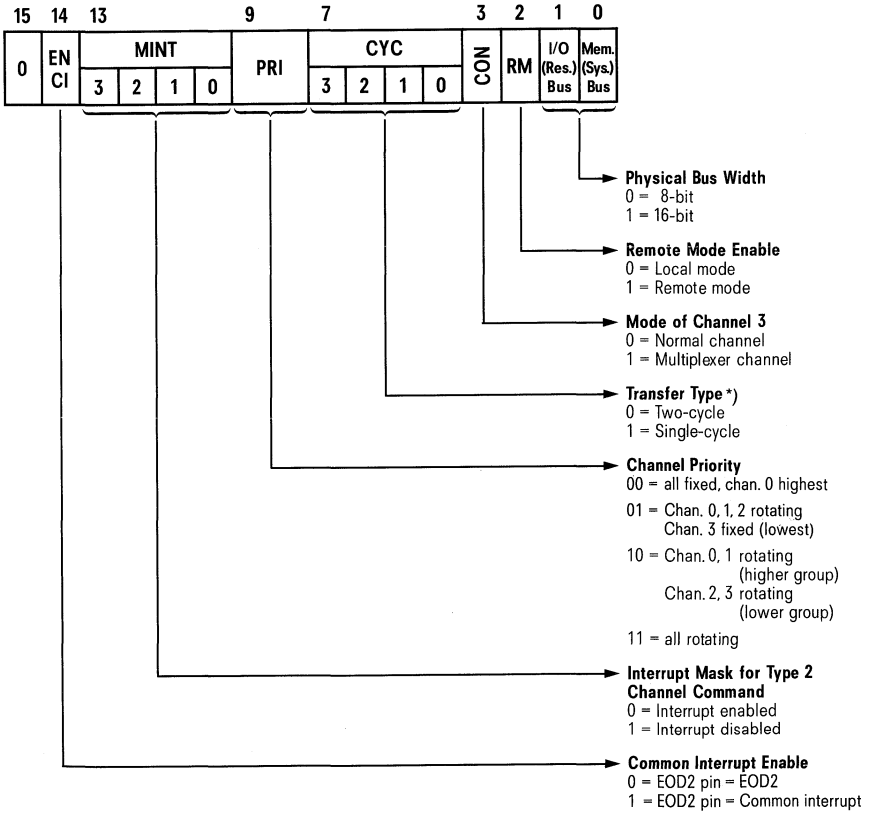
Register Description

General Mode Register

In the general mode register GMR (figure below) the system wide parameters are specified.

This register should be programmed first after reset; with an 8-bit bus program low byte first.

General Mode Register (GMR)

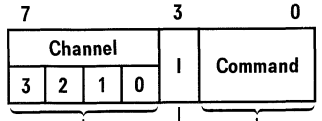


*) On multiplexer channel CYC3 identifies the associated control space for the multiplexer matrix. (CYC3 = 0/1: SAB 8259A in I/O / memory space)

General Command Register

Individual channels are started and stopped by a command written to the general command register GCR (figure below). The GCR is directly loaded by the CPU.

General Command Register (GCR)



Channel Command

000 = NOP	
001 = CONTINUE	Channel(s) after it has been stopped by the STOP command
010 = START	Channel(s) = Command block at system/memory space
011 = START	Channel(s) = Command block at resident I/O space
100 = STOP	Channel(s)
101 = START	Subchannel (number in SCR)
110 = STOP	Subchannel (number in SCR)
111 = HALT	Single-step channel(s): Start execution and stop before next command block will be loaded

Interrupt Command

0 = NOP
1 = Clear interrupt(s) of channel(s)

Channel Select

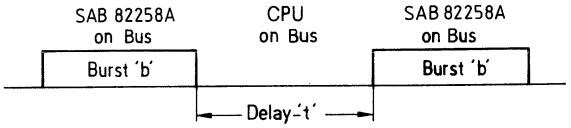
General Burst and Delay Register

It is possible to restrict the bus load generated by the SAB 82258A on the CPU bus by programming the burst and the delay register. The bus load is defined by the formula given in figure a) below. The factor b (burst) is programmed in the general burst register GBR, t (delay time) in the general delay register GDR (see figures b and c).

Since the SAB 82258A can also execute locked bus cycles, the maximum burst length consists of b+3 (8-bit bus) or b+2 (16-bit bus) bus cycles. GBR and GDR must be directly loaded by the CPU. Loading GBR with 0 leads to no bus load limitations for the SAB 82258A (default after reset).

General Burst and Delay Register

a) Bus Loading

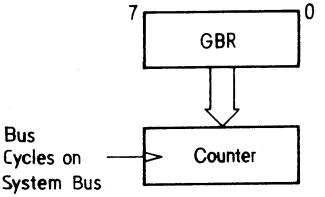


$$\text{Bus Load Due to SAB 82258A} = \frac{b}{b+t}$$

b) General Burst Register (GBR) - to Program 'b'

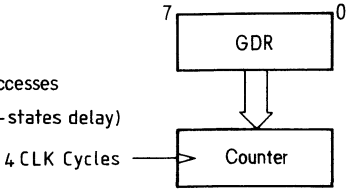
Determines Max. Number of Contiguous Bus Cycles from SAB 82258A

If GBR=0, No Limit



c) General Delay Register (GDR) - to Program 't'

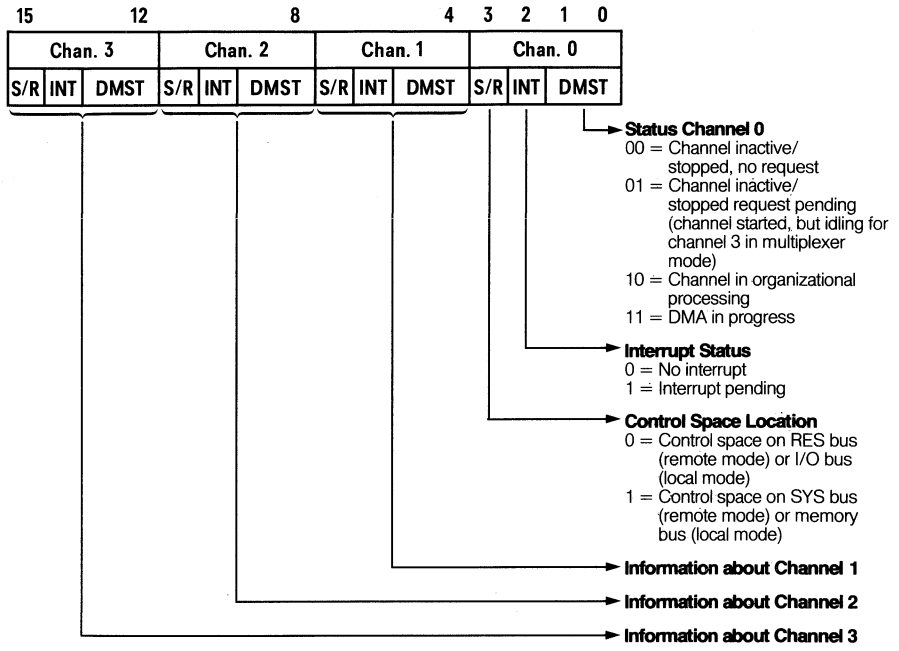
Determines Min. Number of Clock Cycles Between Burst Accesses (default after reset=0, i.e. 4 T-states delay)



General Status Register

The general status register GSR (figure below) shows the current states of all the channels.

General Status Register (GSR)



Channel Commands

The channel commands are contained in the channel command block. Up to 22 bits are used to specify the command. There are two types of channel commands:

- Type 1: for data movement
- Type 2: for command chaining control

The command block for a type 1 command is in general 26 bytes long (see figure on page 17).

For certain type 1 transfers which, for example, do not use on-the-fly match, translate or verify feature, the command is only 16 bits long and only a short command block is necessary (see figure on page 17).

The type 1 command fields (see figures on page 29 and 30) contain information on:

a. Bus width of source and destination
b. If source and/or destination address should be incremented or decremented or kept constant during the transfer
c. If source/destination is in memory or I/O space (local mode) or in system or resident space (remote mode)
d. If data chaining (list or linked-list) is to be performed
e. If the data transfer is synchronized (source or destination)
f. If an on-the-fly match operation and/or translate operation has to be performed
g. If a verify operation has to be performed
h. If 32-bit fly-by transfers are to be executed.

Type 2 command blocks are 6 bytes long (see figure on page 31) of which the first 2 bytes form the command and the rest is either a relative displacement or an absolute address for the JUMP operation. There are two basic type 2 commands (see figure on page 31):

a. JUMP – conditional and non-conditional
b. STOP – conditional and non-conditional

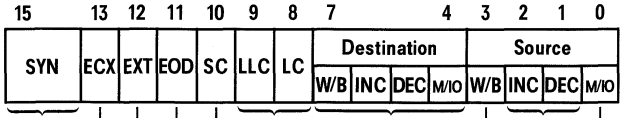
The conditional case tests for either of the 4 condition bits which are altered at the termination of any DMA operation:

- Termination due to byte count end
- Termination due to mask-compare
- Termination due to external terminate
- Verify operation resulting in mismatch.

It is thus possible to JUMP or STOP further execution of commands based on any of these conditions and optionally generate $\overline{\text{EOD}}$ or interrupt signal.

The combination of type 1 and 2 commands gives the SAB 82258A a high degree of "programmability". It can thus execute quite complex algorithms with a fairly low demand for CPU service.

Type 1 (DMA) Channel Command



Source Description Associated Space
0 = I/O or resident
1 = Memory or system

Source Pointer
00 = Pointer not modified
01 = Decrement pointer
10 = Increment pointer
11 = No pointer (constant value)

Logical Bus Width
0 = 8-bit
1 = 16-bit

Destination Description
Same as source description

Data Chaining

LLC	LC	
0	0	No chaining
0	1	List chaining
1	0	Linked list chaining
1	1	Not allowed

Select Chaining
0 = Destination data chaining
1 = Source data chaining

For MUX Channel:
Transfer Chaining
0 = Transfer is synchronized
1 = Transfer not synchronized

Enable $\overline{\text{EOD}}$ Output

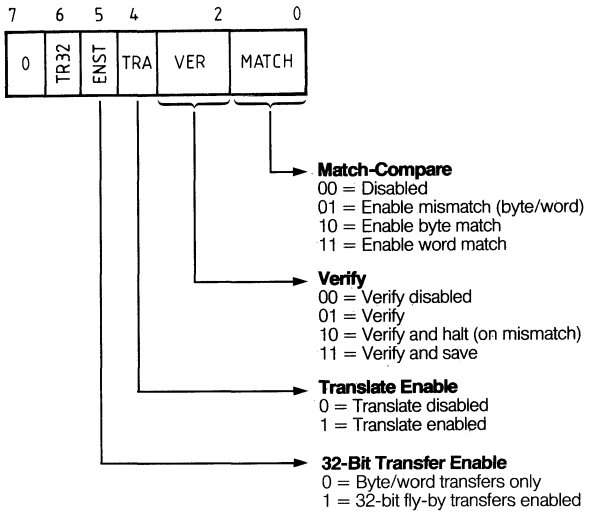
Enable External Terminate Input

Channel Command Block Length
0 = Short
1 = Long (with command extension)

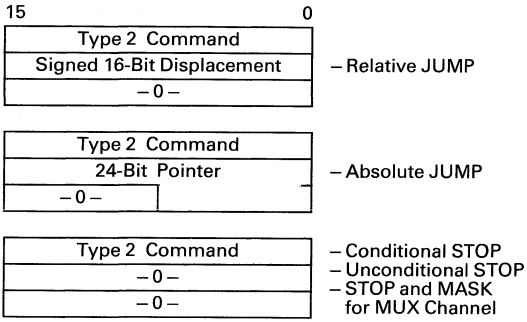
Synchronization
00 = Not valid (type 2 command)
01 = Source synchronization
10 = Destination synchronization
11 = No synchronization (free running)

For Multiplexer Channel
00 = Not valid (type 2 command)
01 = Byte/word multiplex operation
10 = Single transfer operation
11 = Block multiplex operation

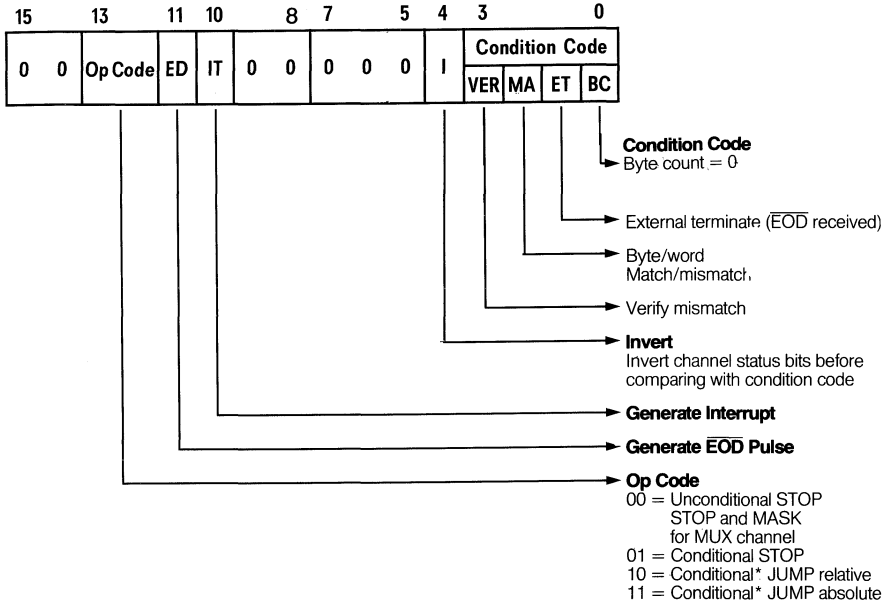
Type 1 Channel Command Extension



Type 2 Command Blocks (for command chaining control)



Type 2 Command Format

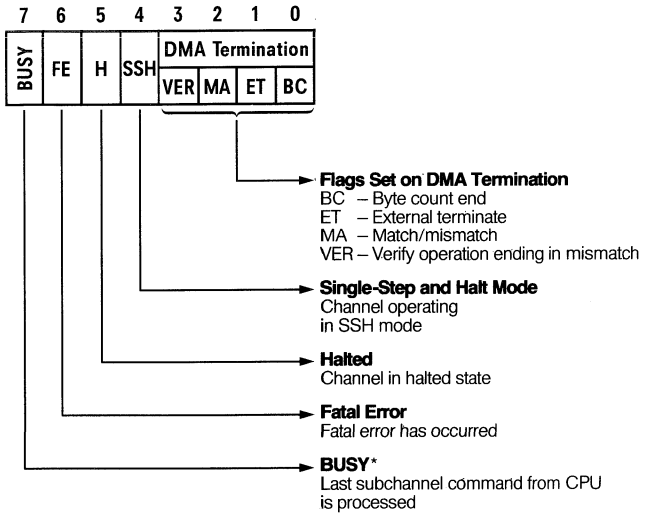


*) Unconditional JUMP when all condition code bits are set 1.

Channel Status Register

For each channel there is a channel status register (see figure below). This register shows the current state of the appropriate channel.

Channel Status Register



*) Valid only for channel 3 in multiplexer mode. In all other cases 0 is returned.

Multiplexer Channel Registers

These registers are valid only for channel 3 if programmed as multiplexer channel.

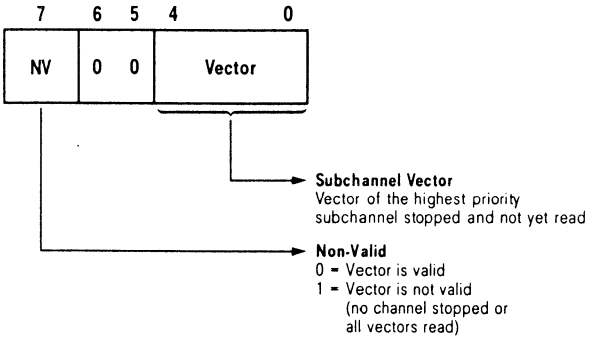
Multiplexer Table Pointer Register (MTPR)

This 24-bit register is used to reference the multiplexer table in memory (see figure on page 20). It must be loaded by the CPU. Physically the list pointer register is used, since data chaining is not allowed for multiplexer channel.

Multiplexer Interrupt Vector Register

This 8-bit register is read by the CPU to determine which subchannels are stopped. The vectors of the stopped subchannels are output on subsequent read operations in the order of their priority (0 has highest priority).

Multiplexer Interrupt Vector Register (MIVR)



Last Vector Register (LVR)

This 8-bit register holds the last vector read by the SAB 82258A (from SAB 8259A). In case of a stop caused by a fatal error on channel 3, LVR determines the failing subchannel.

Subchannel Register

This 8-bit register must be loaded by the CPU with the desired subchannel number before a subchannel command is written into GCR.

Timings

The bus timings in 286 and remote mode are identical to that for SAB 80286, in the 186 and 8086 mode the timings are identical to that for SAB 80186. For exact timings see timing diagrams of AC Characteristics.

Asynchronous control inputs are specified with setup and hold times which are only important to determine whether the SAB 82258A responds to the signal in the current cycle or the next cycle.

The following pages hold two sections of ac characteristics and waveforms. The first section refers to 286 mode and remote mode, the second one to 186 mode and 8086 mode.

Absolute Maximum Ratings

Temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−0.5 to +7V
Power dissipation	3.6W

Note:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics [1]

T_A = 0 to 70°C; T_C = 0 to 100°C; V_{CC} = +5V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
V_{IL}	Input low voltage (except CLK)	−0.5	+0.8	V	–
V_{IH}	Input high voltage (except CLK)	2.0	V_{CC}+0.5	V	–
V_{OL}	Output low voltage	–	0.45	V	I_{OL} = 3.0 mA
V_{OH}	Output high voltage	2.4	–	V	I_{OH} = −400 µA
I_{CC}	Power supply current	–	450	mA	T_A = 25°C, all outputs open
I_{LI}	Input leakage current				
	$\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, M/$\overline{IO}$	–	−200	µA	0 V ≤ V_{IN} ≤ V_{CC}
	HOLD ($\overline{RQ}$/$\overline{GT}$ mode), $\overline{EOD}$	–	−1.5	mA	0 V ≤ V_{IN} ≤ V_{CC}
	A23 (AREADY), A21 [2]	–	−1.5	mA	0 V ≤ V_{IN} ≤ V_{CC}
	other pins	–	±10	µA	0 V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output leakage current	–	±10	µA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CL}	Clock input low voltage	−0.5	+0.6	V	–
V_{CH}	Clock input high voltage	3.8	V_{CC}+1.0	V	–
C_{IN}	Capacitance of inputs (except CLK)	–	10	pF	f_C = 1 MHz
C_{IO}	Capacitance of I/O or outputs	–	20	pF	f_C = 1 MHz
C_{CLK}	Capacitance of CLK input	–	12	pF	f_C = 1 MHz

[1] Clock must be applied.
[2] This specification is valid only during RESET.

AC Characteristics SAB 82258A (286 mode)

T_A = 0 to 70°C; T_C = 0 to 100°C; V_{CC} = +5V ±10%
Any output timing is measured at 1.5V.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_1	CLK cycle period	62	250	ns	–
t_2	CLK low time	15	230	ns	at 1.0 V
t_3	CLK high time	20	235	ns	at 3.6 V
t_4	Address/control output delay	–	60	ns	C_L = 100 pF
t_5	Status output delay	–	40	ns	C_L = 100 pF
t_6	Sync data setup time	10	–	ns	–
t_7	Sync data hold time	5	–	ns	–
t_8	Sync $\overline{\text{READY}}$ setup time	38	–	ns	–
t_9	Sync $\overline{\text{READY}}$ hold time	25	–	ns	–
t_{10}	Sync control input setup time	20	–	ns	–
t_{11}	Sync control/address input hold time	20	–	ns	–
t_{12}	Sync address setup time	2.5	–	ns	–
t_{13}	Data/control output delay	–	50	ns	C_L = 100 pF
t_{14}	Data/control float delay	–	50	ns	–
t_{15}	$\overline{\text{BHE}}$ setup time	60	–	ns	–
t_{16}	Write command width	4CLK+40	–	ns	–
t_{17}	Async data setup time	2CLK+30	–	ns	–
t_{18}	Async address setup time	20	–	ns	–
t_{19}	Async data access time	–	5CLK+70	ns	–

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{28}	Mode select setup time	2CLK+20	–	ns	–
t_{29}	Mode select hold time	0	–	ns	–
t_{33}	Command recovery time	4CLK+40	–	ns	–
t_{34}	CLK rise time	–	15	ns	1.0 to 3.6V
t_{35}	CLK fall time	–	15	ns	3.6 to 1.0V
t_{36}	DREQ inactive after $\overline{\text{DACK}}$ active	0	–	ns	–
t_{37}	$\overline{\text{CS}}$ active response time	–	22CLK +80	ns	[1]
t_{39}	$\overline{\text{CS}}$ active after BREL inactive	0	–	ns	–
t_{42}	HOLD active to HLDA active	0	–	ns	–
t_{43}	Async input setup time	20	–	ns	[2]
t_{44}	Async input hold time	20	–	ns	[2]
t_{47}	Async HLDA high time	2CLK+40	–	ns	[3]
t_{49}	HOLD output low time	4CLK–50	–	ns	–
t_{50}	HLDA low to HOLD low delay	–	22CLK +70	ns	[1]
t_{53}	Read command width	t_{19}	–	ns	–
t_{54}	Async access setup time	20	–	ns	–
t_{55}	Async access hold time	20	–	ns	–
t_{56}	$\overline{\text{CS}}$ hold time	40	–	ns	–

[1] This maximum value refers to active MUX channel. If the MUX channel is not used, the maximum value is reduced by 6 CLKs!
If wait states are inserted, the maximum value has to be extended by the time required for the wait states for 3 bus cycles.

[2] These specifications are given for testing purposes only to assure recognition at a specific clock edge.

[3] This timing is valid if the signal is not synchronous, i.e. does not meet the specified setup and hold times.

AC Characteristics SAB 82258A-1 (286 mode)

T_A = 0 to 55°C; T_C = 0 to 85°C; V_{CC} = +5V ±5%
Any output timing is measured at 1.5V.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_1	CLK cycle period	50	250	ns	–
t_2	CLK low time	12	234	ns	at 1.0 V
t_3	CLK high time	16	238	ns	at 3.6 V
t_4	Address/control output delay	–	47	ns	C_L = 100 pF
t_5	Status output delay	–	28	ns	C_L = 100 pF
t_6	Sync data setup time	8	–	ns	–
t_7	Sync data hold time	5	–	ns	–
t_8	Sync $\overline{\text{READY}}$ setup time	26	–	ns	–
t_9	Sync $\overline{\text{READY}}$ hold time	25	–	ns	–
t_{10}	Sync control input setup time	20	–	ns	–
t_{11}	Sync control/address input hold time	20	–	ns	–
t_{12}	Sync address setup time	2.5	–	ns	–
t_{13}	Data/control output delay	–	40	ns	C_L = 100 pF
t_{14}	Data/control float delay	–	47	ns	–
t_{15}	$\overline{\text{BHE}}$ setup time	45	–	ns	–
t_{16}	Write command width	4CLK+40	–	ns	–
t_{17}	Async data setup time	2CLK+30	–	ns	–
t_{18}	Async address setup time	20	–	ns	–
t_{19}	Async data access time	–	5CLK+60	ns	–

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{28}	Mode select setup time	2CLK+20	–	ns	–
t_{29}	Mode select hold time	0	–	ns	–
t_{33}	Command recovery time	4CLK+40	–	ns	–
t_{34}	CLK rise time	–	8	ns	1.0 to 3.6V
t_{35}	CLK fall time	–	8	ns	3.6 to 1.0V
t_{36}	DREQ inactive after $\overline{\text{DACK}}$ active	0	–	ns	–
t_{37}	$\overline{\text{CS}}$ active response time	–	22CLK +70	ns	[1]
t_{39}	$\overline{\text{CS}}$ active after BREL inactive	0	–	ns	–
t_{42}	HOLD active to HLDA active	0	–	ns	–
t_{43}	Async input setup time	20	–	ns	[2]
t_{44}	Async input hold time	20	–	ns	[2]
t_{47}	Async HLDA high time	2CLK+40	–	ns	[3]
t_{49}	HOLD output low time	4CLK–40	–	ns	–
t_{50}	HLDA low to HOLD low delay	–	22CLK +60	ns	[1]
t_{53}	Read command width	t_{19}	–	ns	–
t_{54}	Async access setup time	20	–	ns	–
t_{55}	Async access hold time	20	–	ns	–
t_{56}	$\overline{\text{CS}}$ hold time	40	–	ns	–

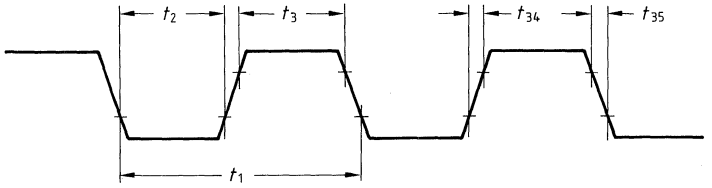
[1] This maximum value refers to active MUX channel. If the MUX channel is not used, the maximum value is reduced by 6 CLKs!
If wait states are inserted, the maximum value has to be extended by the time required for the wait states for 3 bus cycles.

[2] These specifications are given for testing purposes only to assure recognition at a specific clock edge.

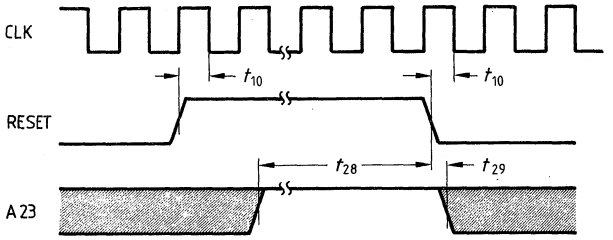
[3] This timing is valid if the signal is not synchronous, i.e. does not meet the specified setup and hold times.

Waveforms

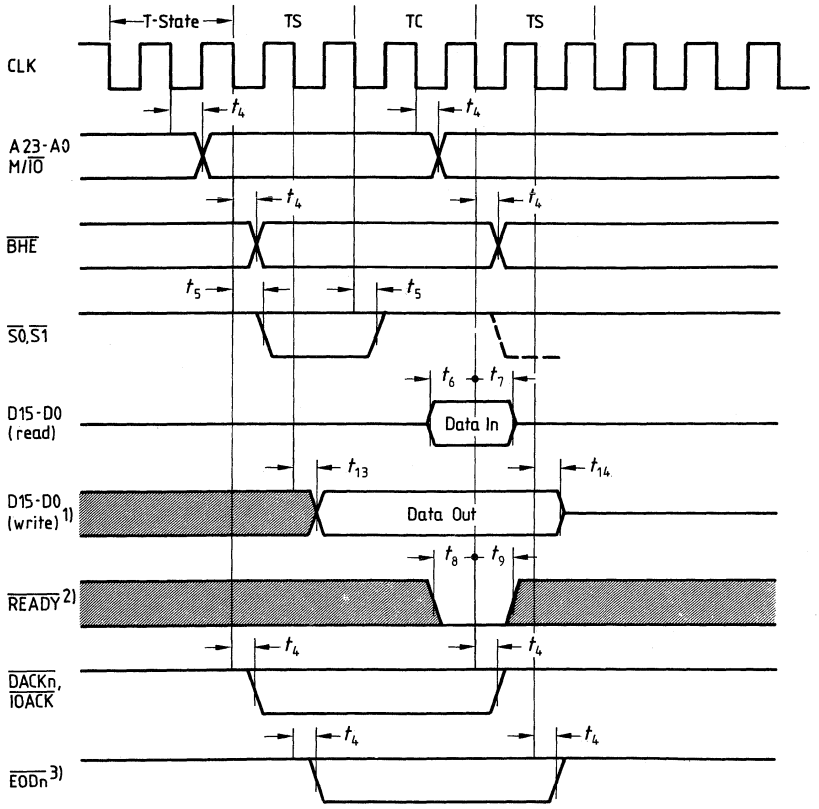
Clock Signal (286 mode)



Mode Selection on RESET (286 mode)



Major Timing for Active Bus Cycles (286 mode)

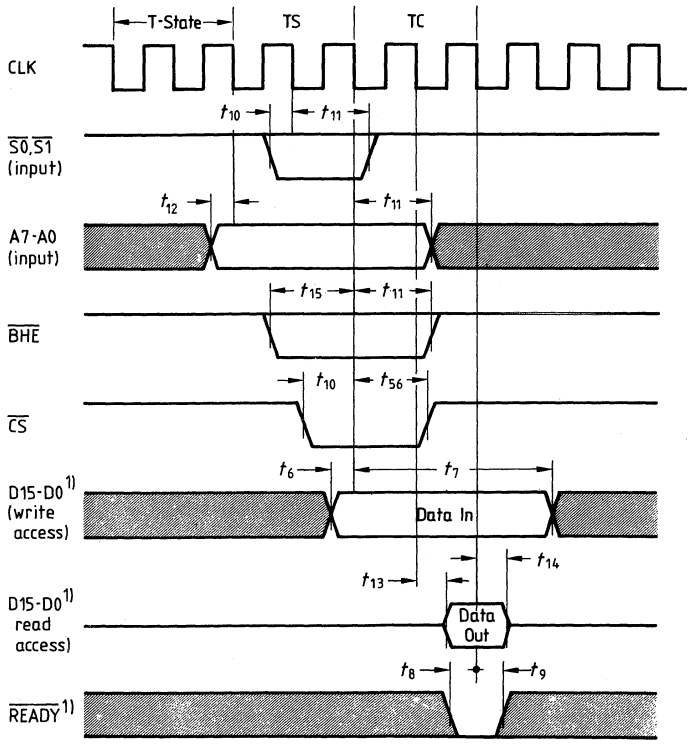


[1] If executing a single cycle transfer, D15 to D0 float like during read cycles!

[2] TC will be repeated if $\overline{\text{READY}}$ is inactive at the sampling point (end of current TC).

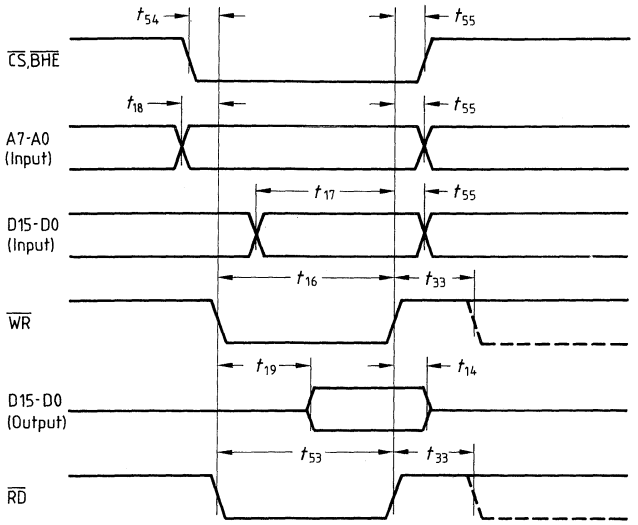
[3] Initiated by terminal count.

Synchronous Access (286 mode)

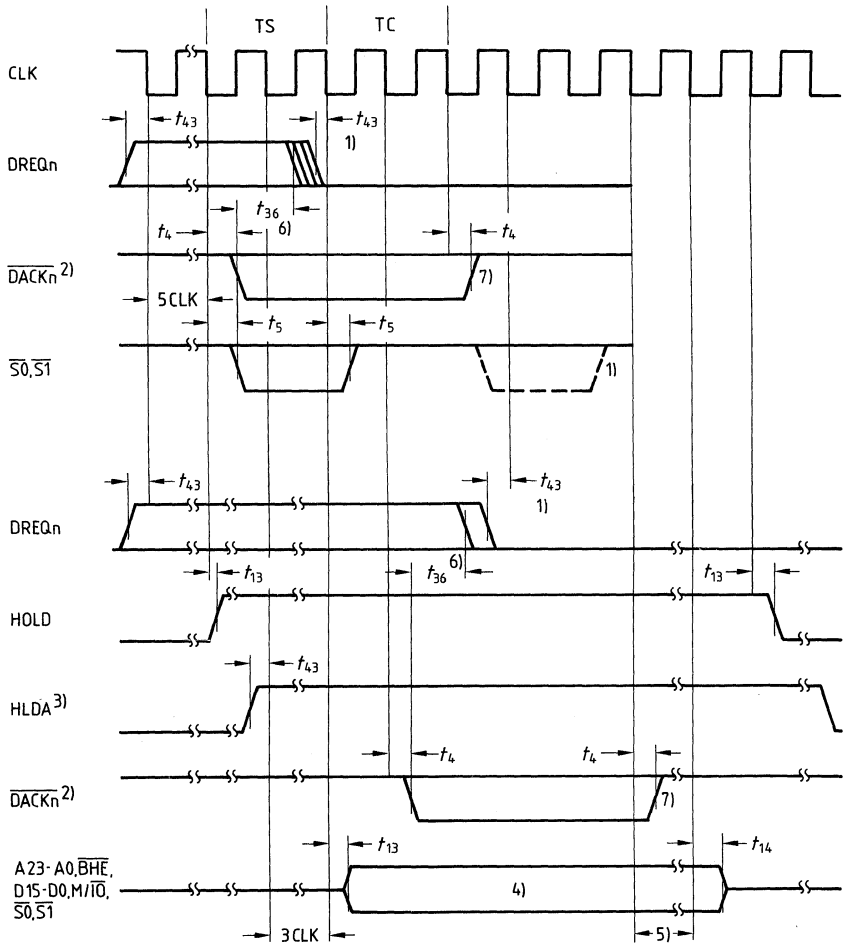


[1] The processor will repeat TC, if READY is not active at the sampling point (end of current TC). The SAB 82258 will output data until the end of the repeated TC (read access) or sample the data bus again at the beginning of the repeated TC (write access).

Asynchronous Access (286 mode)



DMA Control (286 mode)



[1] If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfers will be executed.

[2] Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.

[3] The SAB 82258A can be forced off the bus by driving HLDA inactive (see "Bus Arbitration").

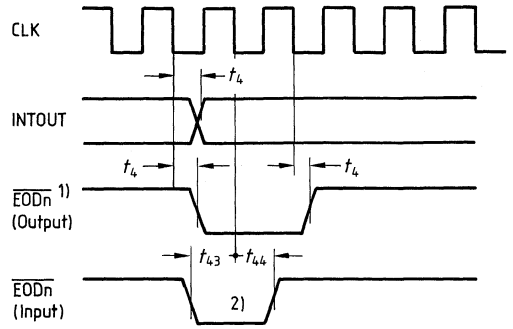
[4] Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycles".

[5] The SAB 82258A may execute additional bus cycles, e.g. for command chaining.

[6] Minimum time to execute bus cycle.

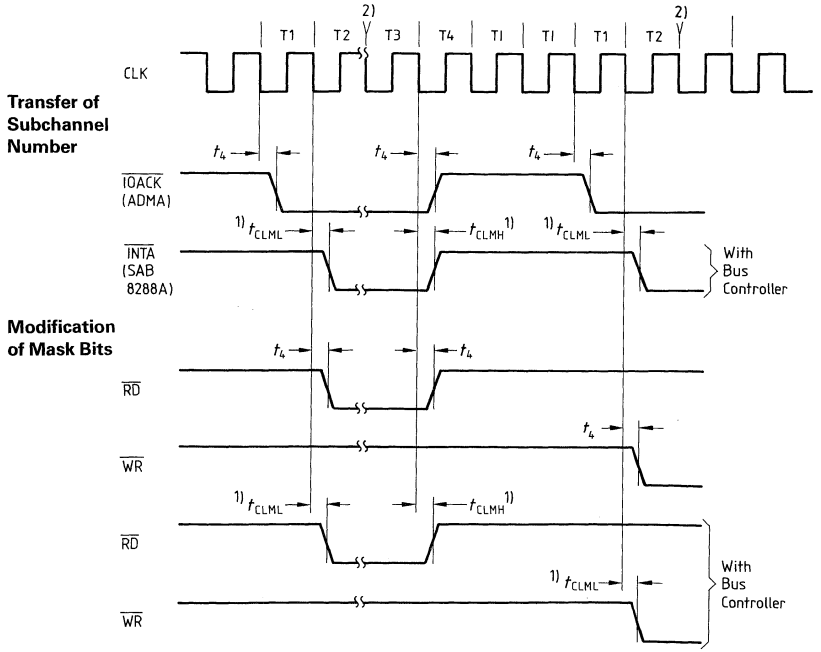
[7] If the SAB 82258A does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the DACKn signal can be prolonged by two T-states.

$\overline{EOD}$/INTOUT Timing (286 mode)



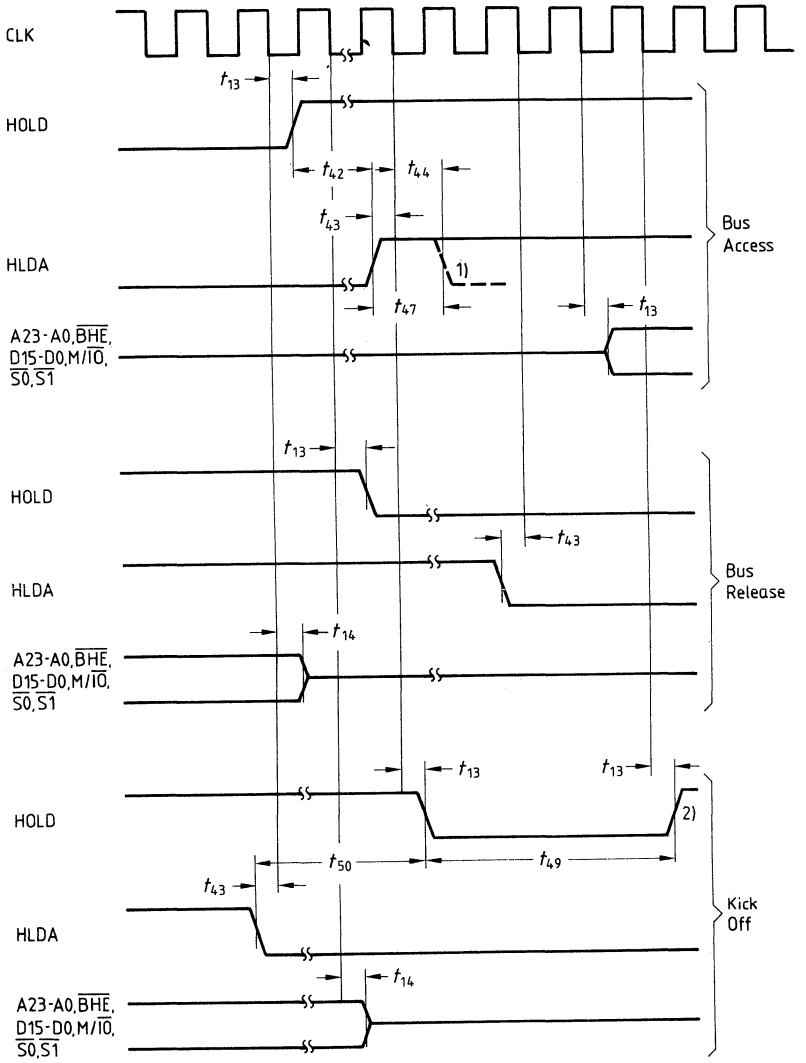
1) Initiated by type 2 command.
2) $\overline{EOD}$ input minimum pulse width is 3 CLKs if the signal is asynchronous.

Access to SAB 8259A (286 mode)



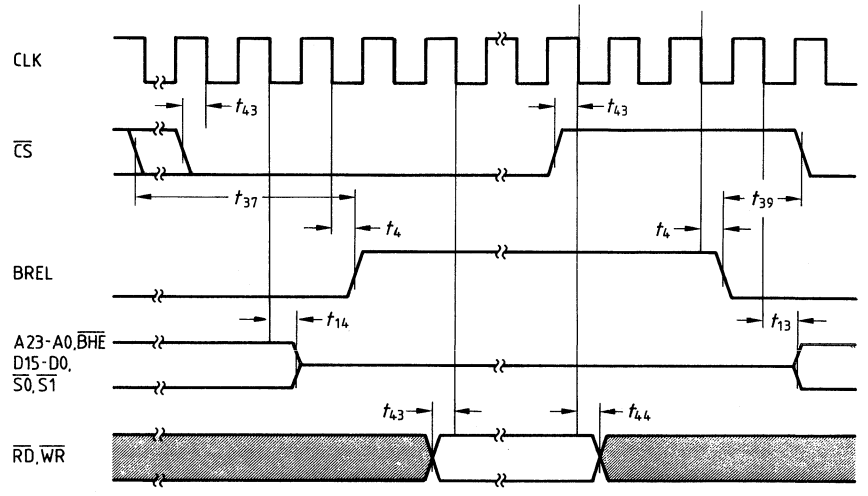
1) These timings are SAB 82288 timings!
2) Additional wait states may be inserted.

Bus Arbitration (286 mode)



1) Minimum HLDA high time before kick-off to respond to HOLD signal.
2) Earliest possible reactivation of HOLD after deactivation of HLDA.

Access in Remote Mode



AC Characteristics SAB 82258A (186 mode)

T_A = 0 to 70°C; T_C = 0 to 100°C; V_{CC} = +5V ±10%
Any output timing is measured at 1.5V.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_4	Control output delay	–	60	ns	–
t_6	Sync address/data setup time	10	–	ns	–
t_7	Sync data hold time	5	–	ns	–
t_{10}	Sync control input setup time	20	–	ns	–
t_{11}	Sync control/address input hold time	20	–	ns	–
t_{13}	Data/control delay	–	50	ns	C_L = 100 pF
t_{14}	Data float delay	–	50	ns	–
t_{16}	Write command width	2CLK+40	–	ns	–
t_{17}	Async data setup time	CLK+30	–	ns	–
t_{18}	Async address setup time	20	–	ns	–
t_{19}	Async data access time	–	2CLK $+t_{22}$+70	ns	–
t_{20}	CLK cycle period	125	500	ns	–
t_{21}	CLK low time	55	–	ns	at 1.5V
t_{22}	CLK high time	55	–	ns	at 1.5V
t_{23}	CLK rise time	–	15	ns	1.0 to 3.5V
t_{24}	CLK fall time	–	15	ns	3.5 to 1.0V
t_{25}	AREADY active setup time	20	–	ns	[2]
t_{26}	AREADY hold time	15	–	ns	[2]
t_{27}	AREADY inactive setup time	35	–	ns	–

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{28}	Mode select setup time	2CLK+20	–	ns	–
t_{29}	Mode select hold time	0	–	ns	–
t_{30}	Address/data output delay	10	50	ns	C_L = 20 to 200 pF
t_{31}	Status output delay	10	55	ns	–
t_{32}	Float delay	10	50	ns	–
t_{33}	Command recovery time	2CLK+40	–	ns	–
t_{36}	DREQ inactive after $\overline{\text{DACK}}$ active	0	–	ns	–
t_{38}	ALE output delay	–	40	ns	–
t_{40}	Address/control input hold time	10	–	ns	–
t_{41}	Address input setup time	10	–	ns	–
t_{42}	HOLD active to HLDA active	0	–	ns	–
t_{43}	Async control input setup time	20	–	ns	[2]
t_{44}	Async control input hold time	20	–	ns	[2]
t_{45}	HLDA hold time	10	–	ns	–
t_{46}	Async HLDA high time	CLK+40	–	ns	[3]
t_{48}	HOLD output delay	5	70	ns	–
t_{51}	HOLD output low time	2CLK−70	–	ns	–
t_{52}	HLDA low to HOLD low delay	–	15CLK +90	ns	[1]
t_{54}	Async access setup time	20	–	ns	–
t_{55}	Async access hold time	20	–	ns	–
t_{57}	SREADY hold time	15	–	ns	–
t_{58}	Status setup time	35	–	ns	–

[1] This maximum value refers to active MUX channel. If the MUX channel is not used, the maximum value is reduced by 3 CLKs!
If wait states are inserted, the maximum value has to be extended by the time required for the wait states for 2 bus cycles.

[2] These specifications are given for testing purposes only to assure recognition at a specific clock edge.

[3] This timing is valid, if the signal is not synchronous, i.e. does not meet the specified setup and hold times.

AC Characteristics SAB 82258A-1 (186 mode)

T_A = 0 to 55°C; T_C = 0 to 85°C; V_{CC} = +5V ±5%
Any output timing is measured at 1.5V.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_4	Control output delay	–	56	ns	–
t_6	Sync address/data setup time	10	–	ns	–
t_7	Sync data hold time	5	–	ns	–
t_{10}	Sync control input setup time	20	–	ns	–
t_{11}	Sync control/address input hold time	20	–	ns	–
t_{13}	Data/control delay	–	40	ns	C_L = 100 pF
t_{14}	Data float delay	–	40	ns	–
t_{16}	Write command width	2CLK+40	–	ns	–
t_{17}	Async data setup time	CLK+30	–	ns	–
t_{18}	Async address setup time	20	–	ns	–
t_{19}	Async data access time	–	2CLK $+t_{22}$+60	ns	–
t_{20}	CLK cycle period	100	500	ns	–
t_{21}	CLK low time	44	–	ns	at 1.5V
t_{22}	CLK high time	44	–	ns	at 1.5V
t_{23}	CLK rise time	–	12	ns	1.0 to 3.5V
t_{24}	CLK fall time	–	12	ns	3.5 to 1.0V
t_{25}	AREADY active setup time	15	–	ns	2)
t_{26}	AREADY hold time	15	–	ns	2)
t_{27}	AREADY inactive setup time	25	–	ns	–

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{28}	Mode select setup time	2CLK+20	–	ns	–
t_{29}	Mode select hold time	0	–	ns	–
t_{30}	Address/data output delay	10	40	ns	C_L = 20 to 200 pF
t_{31}	Status output delay	10	45	ns	–
t_{32}	Float delay	10	40	ns	–
t_{33}	Command recovery time	2CLK+40	–	ns	–
t_{36}	DREQ inactive after $\overline{\text{DACK}}$ active	0	–	ns	–
t_{38}	ALE output delay	–	35	ns	–
t_{40}	Address/control input hold time	10	–	ns	–
t_{41}	Address input setup time	10	–	ns	–
t_{42}	HOLD active to HLDA active	0	–	ns	–
t_{43}	Async control input setup time	20	–	ns	[2]
t_{44}	Async control input hold time	20	–	ns	[2]
t_{45}	HLDA hold time	5	–	ns	–
t_{46}	Async HLDA high time	CLK+40	–	ns	[3]
t_{48}	HOLD output delay	5	60	ns	–
t_{51}	HOLD output low time	2CLK−60	–	ns	–
t_{52}	HLDA low to HOLD low delay	–	15CLK +80	ns	[1]
t_{54}	Async access setup time	20	–	ns	–
t_{55}	Async access hold time	20	–	ns	–
t_{57}	SREADY hold time	15	–	ns	–
t_{58}	Status setup time	35	–	ns	–

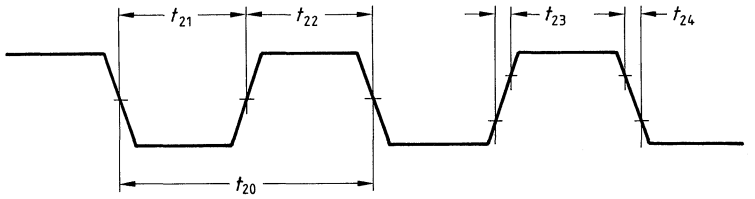
[1] This maximum value refers to active MUX channel. If the MUX channel is not used, the maximum value is reduced by 3 CLKs!
If wait states are inserted, the maximum value has to be extended by the time required for the wait states for 2 bus cycles.

[2] These specifications are given for testing purposes only to assure recognition at a specific clock edge.

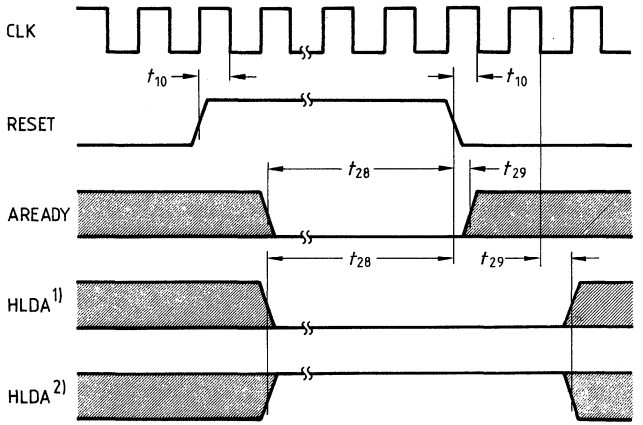
[3] This timing is valid, if the signal is not synchronous, i.e. does not meet the specified setup and hold times.

Waveforms

Clock Signal (186 mode)

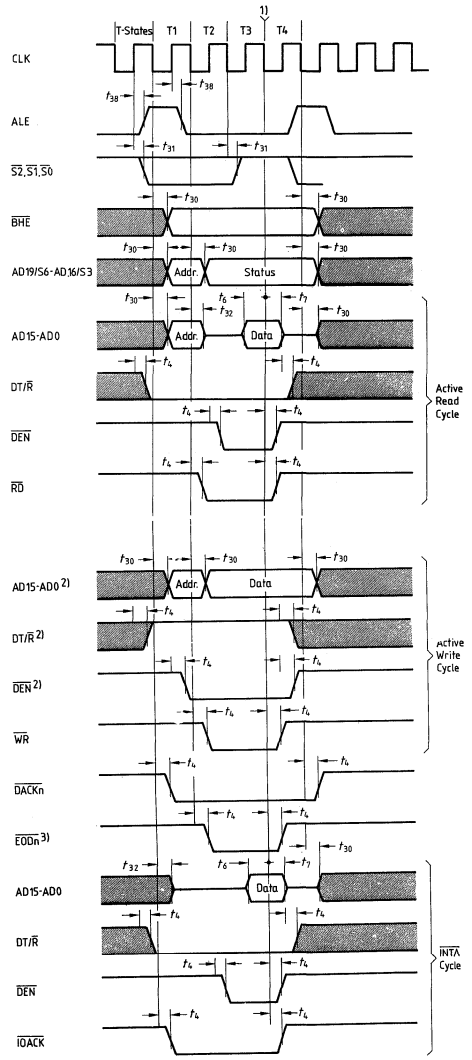


Mode Selection on RESET (186 mode)



1) To operate in 186 mode with HOLD/HLDA protocol.
2) To operate in 8086 mode with $\overline{RQ}/\overline{GT}$ protocol.

Major Timing for Active Bus Cycles (186 mode)

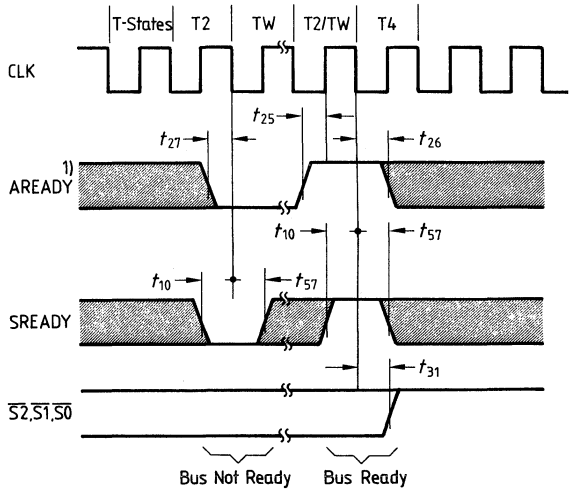


1) A wait state is inserted after T3 or TW, whenever the bus is not ready at the beginning of T3 or TW (see "Bus Cycle Termination"). The status must be valid just prior to T4.

2) For a single-cycle transfer the timing of AD15-AD0, DT/$\overline{R}$ and $\overline{DEN}$ is identical to a read cycle. AD15-AD0 will float as during a read cycle.

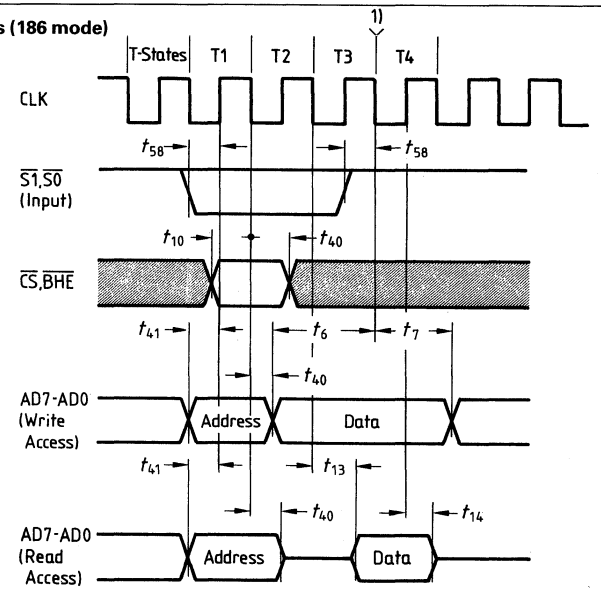
3) Initiated by terminal count.

Bus Cycle Termination (186 mode)



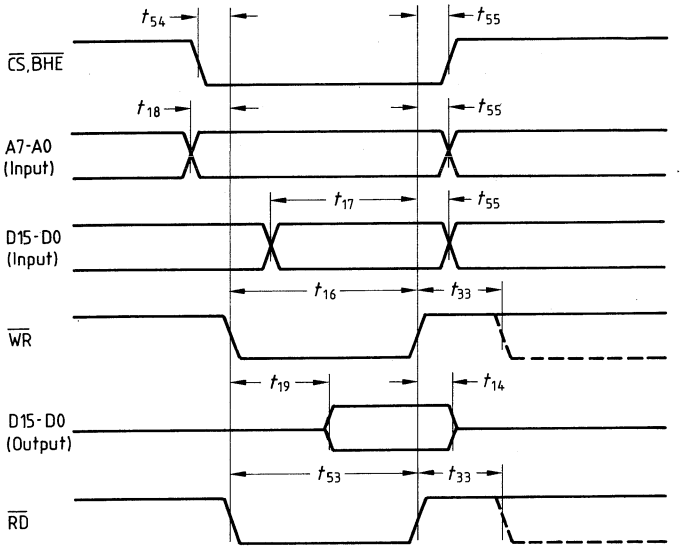
[1] Only the rising edge of AREADY is synchronized internally to CLK. The falling edge must be synchronized externally.

Synchronous Access (186 mode)

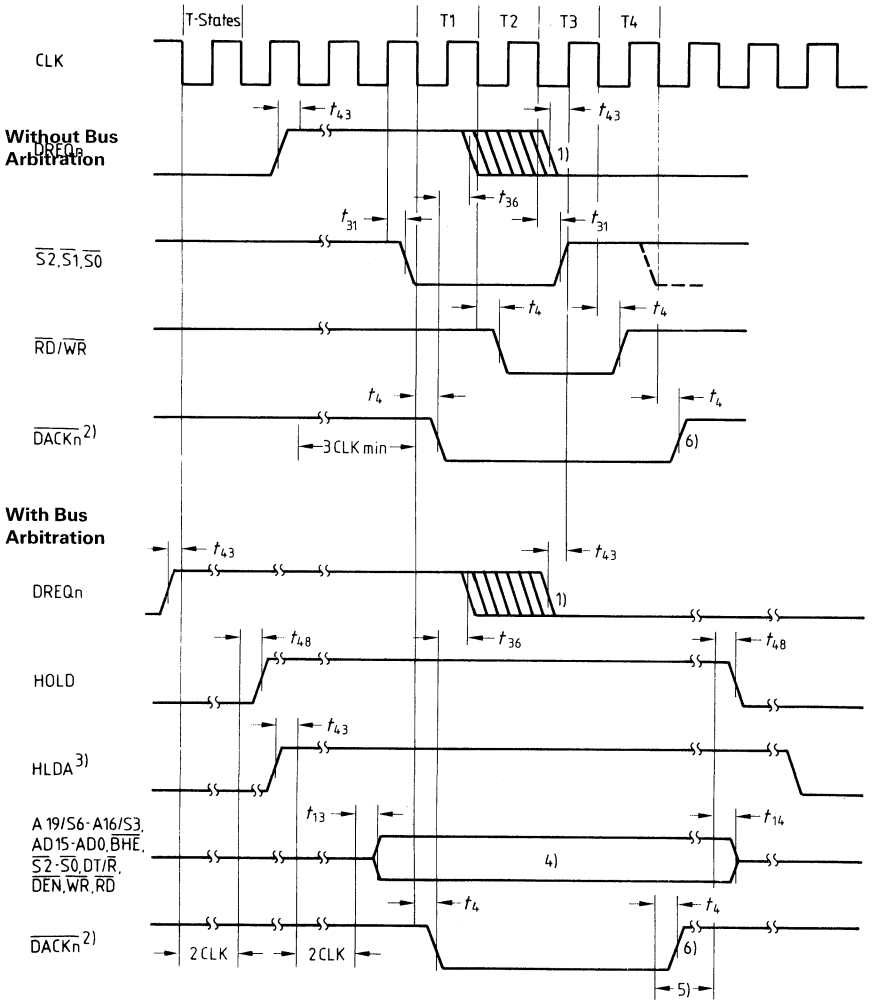


[1] Additional wait cycles may be inserted. Status must be valid just prior to T4.

Asynchronous Access (186 mode)



DMA Control (186 mode)



[1] If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent transfer will be executed.

[2] Refers to the highest priority request. Acknowledging of lower priority requests may be delayed by the execution of higher priority requests.

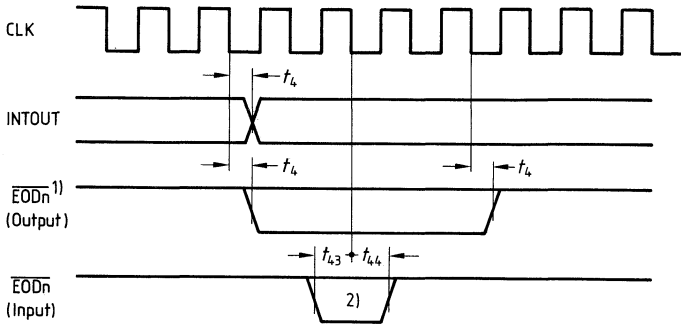
[3] The SAB 82258A can be forced off the bus by driving HLDA inactive (see "Bus Arbitration").

[4] Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycles".

[5] The SAB 82258A may execute additional bus cycles, e.g. for command chaining.

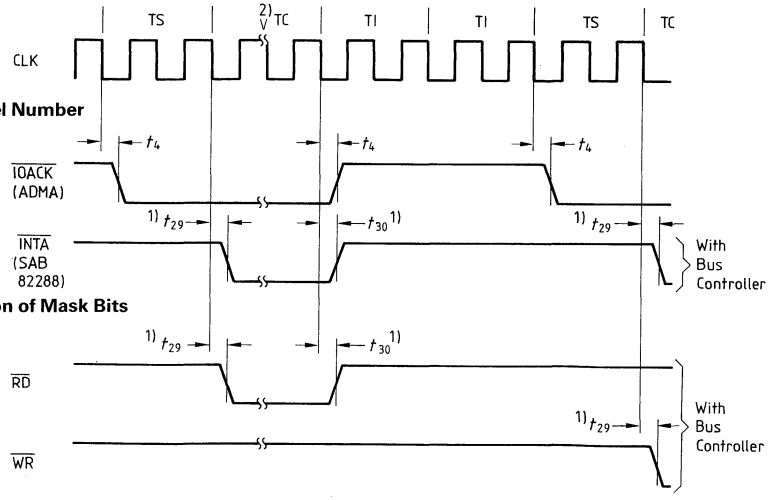
[6] If the SAB 82258A does not perform subsequent bus cycles after this DMA cycle (transfer on another channel or organizational processing), the $\overline{DACKn}$ signal can be prolonged by two T-states.

$\overline{\text{EOD}}$/INTOUT Timing (186 mode)



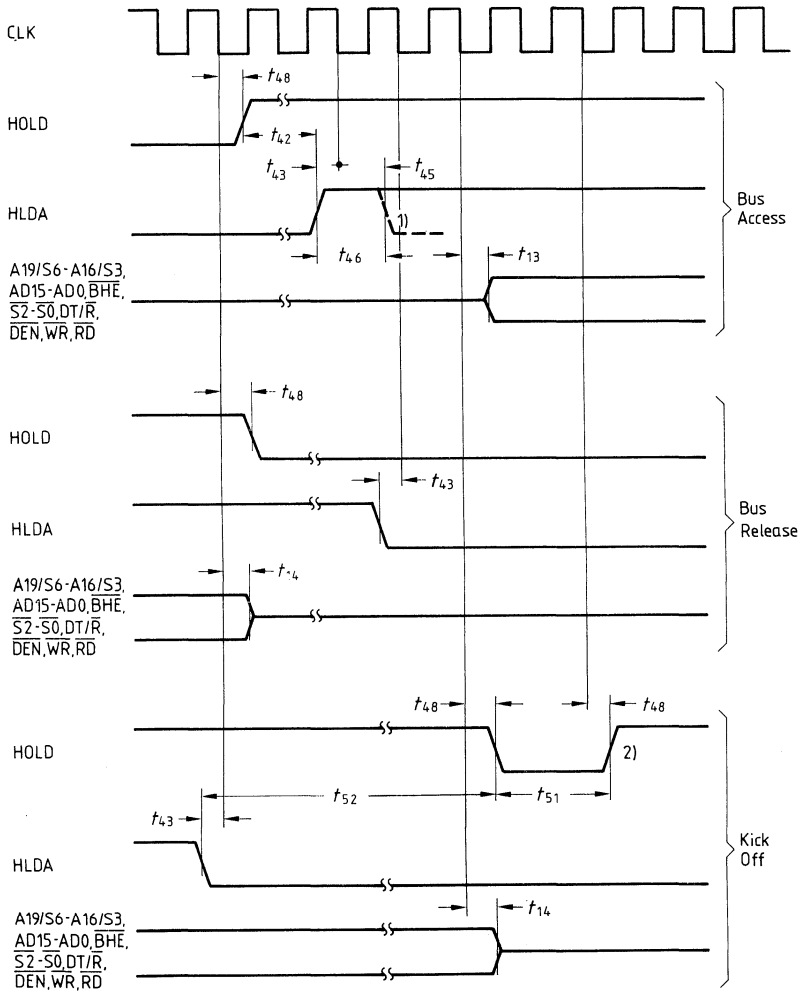
1) Initiated by type 2 command.
2) $\overline{\text{EOD}}$ input minimum pulse width is 2CLKs if the signal is asynchronous.

Access to SAB 8259A (186 mode)



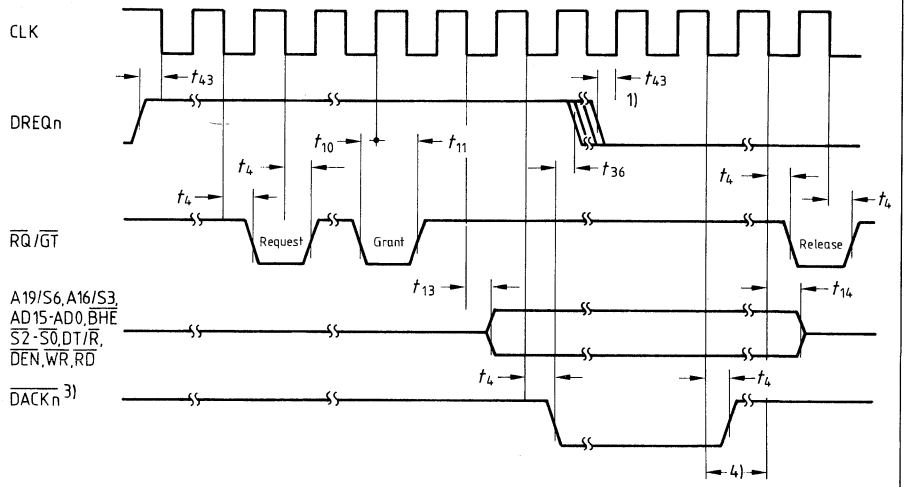
1) These timings are SAB 8288A timings!
2) Additional wait states may be inserted.

Bus Arbitration (186 mode)



[1] Minimum HLDA high time before kick-off to respond to HOLD signal.
[2] Earliest possible reactivation of HOLD after deactivation of HLDA.

DMA Control with $\overline{RQ}/\overline{GT}$ Protocol (8086 mode)



1) If the trailing edge of DREQn is received later, a continuous request is assumed and subsequent bus cycles are executed.

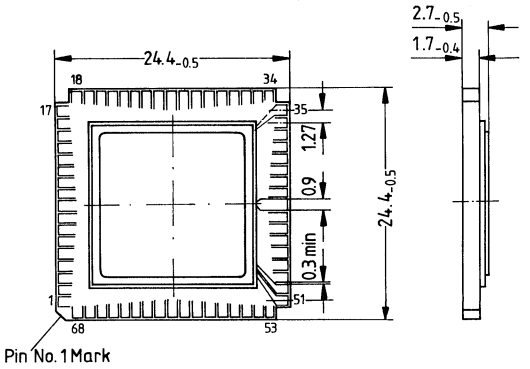
2) Signals driven active. For exact timing refer to "Major Timing for Active Bus Cycles".

3) Refers to the highest priority request. Acknowledge of lower priority requests may be delayed by higher priority requests.

4) The SAB 82258A may execute additional bus cycles, e.g. for command chaining.

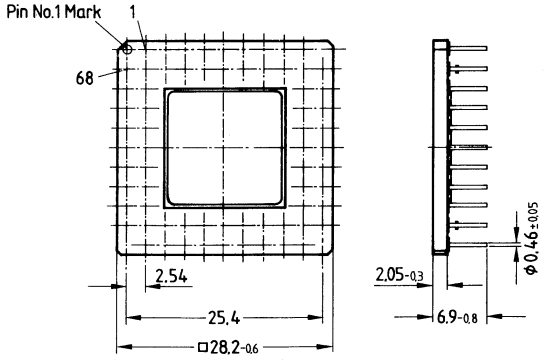
Package Outlines

Ceramic Package, C-CC-68
(chip carrier)



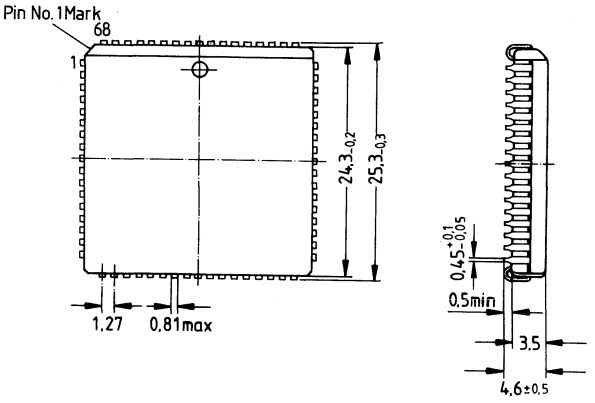
Dimensions in mm

Ceramic Package, C-PGA-68
(pin grid array)



Dimensions in mm

Plastic Package, PL-CC-68 (SMD)
(chip carrier)



Dimensions in mm

Ordering Information

Type	Ordering code	Function
SAB 82258A-R	Q67120-P250	Advanced DMA controller, 8 MHz (C-CC-68)
SAB 82258A-1-R	Q67120-P249	Advanced DMA controller, 10 MHz (C-CC-68)
SAB 82258A-A	Q67120-P248	Advanced DMA controller, 8 MHz (C-PGA-68)
SAB 82258A-1-A	Q67120-P247	Advanced DMA controller, 10 MHz (C-PGA-68)
SAB 82258A-N	Q67120-P246	Advanced DMA controller, 8 MHz (PL-CC-68)
SAB 82258A-1-N	Q67120-P245	Advanced DMA controller, 10 MHz (PL-CC-68)

Preliminary

SAB 82284 Clock Generator and Ready Interface for SAB 80286 Processors

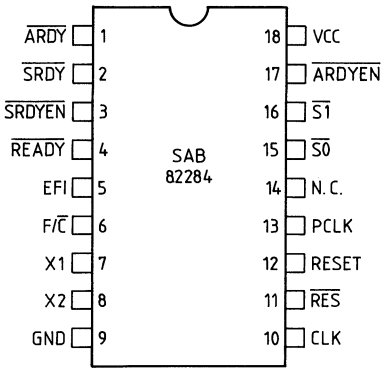
SAB 82284 up to 16 MHz

- Generates system clock for SAB 80286 processors
- Uses crystal or TTL signal for frequency source
- Provides local $\overline{\text{READY}}$ and multimaster system bus $\overline{\text{READY}}$ synchronization

SAB 82284-1 up to 20 MHz

- 18-pin package
- Single +5 V power supply
- Generates system reset output from Schmitt-trigger input

Pin Configuration



Pin Names

CLK	System Clock
F/$\overline{\text{C}}$	Frequency/Crystal Select
X1, X2	Crystal In
EFI	External Frequency In
PCLK	Peripheral Clock
$\overline{\text{ARDYEN}}$	Asynchronous Ready Enable
$\overline{\text{ARDY}}$	Asynchronous Ready
$\overline{\text{SRDYEN}}$	Synchronous Ready Enable
$\overline{\text{SRDY}}$	Synchronous Ready
$\overline{\text{READY}}$	Bus Cycle Termination
$\overline{\text{S0}}$, $\overline{\text{S1}}$	Status
RESET	Reset
$\overline{\text{RES}}$	Reset In
VCC	Power supply (+5V)
GND	Ground (0V)

The SAB 82284 is a bipolar clock generator/driver which provides clock signals for SAB 80286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

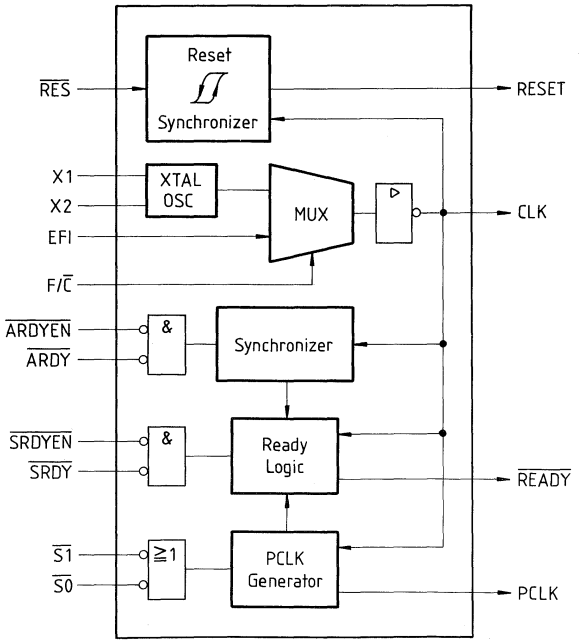
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{ARDY}}$	1	I	ASYNCHRONOUS READY is an active low input used to terminate the current bus cycle. The $\overline{\text{ARDY}}$ input is qualified by $\overline{\text{ARDYEN}}$. Inputs to ARDY may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
$\overline{\text{SRDY}}$	2	I	SYNCHRONOUS READY is an active low input used to terminate the current bus cycle. The $\overline{\text{SRDY}}$ input is qualified by the $\overline{\text{SRDYEN}}$ input. Setup and hold times must be satisfied for proper operation.
$\overline{\text{SRDYEN}}$	3	I	SYNCHRONOUS READY ENABLE is an active low input which qualifies $\overline{\text{SRDY}}$. $\overline{\text{SRDYEN}}$ selects $\overline{\text{SRDY}}$ as the source for $\overline{\text{READY}}$ to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.
$\overline{\text{READY}}$	4	O	READY is an active low output which signals the current bus cycle is to be completed. The $\overline{\text{SRDY}}$, $\overline{\text{SRDYEN}}$, $\overline{\text{ARDY}}$, $\overline{\text{ARDYEN}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$ and $\overline{\text{RES}}$ inputs control $\overline{\text{READY}}$ as explained later in the $\overline{\text{READY}}$ generator section. $\overline{\text{READY}}$ is an open collector output requiring an external pullup resistor.
EFI	5	I	EXTERNAL FREQUENCY IN drives CLK when the F/$\overline{\text{C}}$ input is strapped high. The EFI input frequency must be twice the desired internal processor clock frequency.
F/$\overline{\text{C}}$	6	I	FREQUENCY/CRYSTAL SELECT is a strapping option to select the source for the CLK output. When F/$\overline{\text{C}}$ is strapped low, the internal crystal oscillator drives CLK. When F/$\overline{\text{C}}$ is strapped high, the EFI input drives the CLK output.
X1, X2	7, 8	I	CRYSTAL IN are the pins to which a parallel resonant fundamental mode crystal is attached for the internal oscillator. When F/$\overline{\text{C}}$ is low, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.
CLK	10	O	SYSTEM CLOCK is the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and MOS level inputs.
$\overline{\text{RES}}$	11	I	RESET IN is an active low input which generates the system reset signal RESET. Signals to $\overline{\text{RES}}$ may be applied asynchronously to CLK. A Schmitt-trigger input is provided on $\overline{\text{RES}}$, so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
RESET	12	O	RESET is an active high output which is derived from the $\overline{\text{RES}}$ input. RESET is used to force the system into an initial state. When RESET is active, $\overline{\text{READY}}$ will be active (low).

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
PCLK	13	O	PERIPHERAL CLOCK is an output which provides a 50% duty cycle clock with 1/2 the frequency of CLK. PCLK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
$\overline{S0}$, $\overline{S1}$	15, 16	I	STATUS inputs prepare the SAB 82284 for a subsequent bus cycle. $\overline{S0}$ and $\overline{S1}$ synchronize PCLK to the internal processor clock and control $\overline{READY}$. These inputs have pullup resistors to keep them high if nothing is driving them. Setup and hold times must be satisfied for proper operation.
$\overline{ARDYEN}$	17	I	ASYNCHRONOUS READY ENABLE is an active low input which qualifies the $\overline{ARDY}$ input. $\overline{ARDYEN}$ selects $\overline{ARDY}$ as the source of ready for the current bus cycle. Inputs to $\overline{ARDYEN}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
VCC	18	–	POWER SUPPLY (+5 V)
GND	9	–	GROUND (0 V)

Block Diagram



Functional Description

Introduction

The SAB 82284 generates the clock, ready, and reset signals required for SAB 80286 processors and support components. The SAB 82284 is packaged in an 18-pin DIP package and contains a crystal-controlled oscillator, MOS clock generator, peripheral clock generator, Multibus ready synchronization logic, and system reset generation logic.

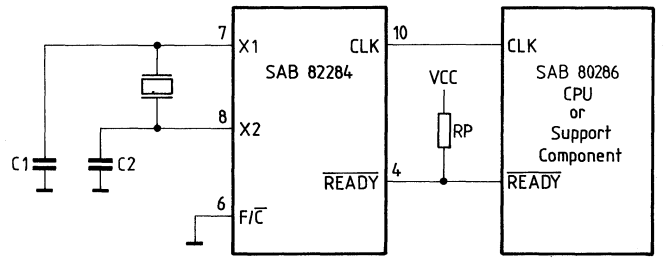
Clock generator

The CLK output provides the basic timing control for an SAB 80286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the F/$\overline{C}$ strapping option. When F/$\overline{C}$ is low, the crystal oscillator drives the CLK output. When F/$\overline{C}$ is high, the EFI input drives the CLK output. The SAB 82284 provides a second clock output (PCLK) for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and TTL output drive characteristics. PCLK is normally synchronized to the internal processor clock. After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its high time beyond one system clock (see waveforms). PCLK is forced high whenever either $\overline{S0}$ or $\overline{S1}$ were active (low) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are high.
Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

Oscillator

The oscillator circuit of the SAB 82284 is a linear Pierce oscillator which requires an external, parallel, resonant, fundamental-mode crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32 pF.
X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in the figure below. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10pF between the X1 and X2 pins.
Decouple VCC and GND as close to the SAB 82284 as possible.

Recommended Crystal and $\overline{\text{READY}}$ Connections
(for RP see note 6 of ac characteristics)



Crystal Loading Table

Crystal Frequency	C1 Capacitance	C2 Capacitance
2 to 8MHz	60pF	40pF
8 to 20MHz	25pF	15pF

Reset Operation

The reset logic provides the RESET output to force the system into a known initial state. When the $\overline{RES}$ input is active (low), the RESET output becomes active (high). $\overline{RES}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the $\overline{RES}$ input introduces a one or two CLK delay before affecting the RESET output.

At power up, a system does not have a stable VCC and CLK. To prevent spurious activity, $\overline{RES}$ should be asserted until VCC and CLK stabilize at their operating values. SAB 80286 processors and support components also require their RESET inputs be high a minimum number of CLK cycles. An RC network, as shown below, will keep $\overline{RES}$ low long enough to satisfy both needs.

A Schmitt-trigger input with hysteresis on $\overline{RES}$ assures a single transition of RESET with an RC circuit on $\overline{RES}$. The hysteresis separates the input voltage level at which the circuit output switches from high to low from the input voltage level at which the circuit output switches from low to high. The $\overline{RES}$ high to low input transition voltage is lower than the $\overline{RES}$ low to high input transition voltage. As long as the slope of the $\overline{RES}$ input voltage remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input transition voltage, the RESET output will make a single transition.

Ready Operation

The SAB 82284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous ($\overline{SRDY}$) or asynchronous ready ($\overline{ARDY}$) source may be used. Each ready input has an enable ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

The figure on synchronous ready mode illustrates the operation of $\overline{SRDY}$ and $\overline{SRDYEN}$. These inputs are sampled on the falling edge of CLK when $\overline{S1}$ and $\overline{S0}$ are inactive and PCLK is high. $\overline{READY}$ is forced active when both $\overline{SRDY}$ and $\overline{SRDYEN}$ are sampled as low.

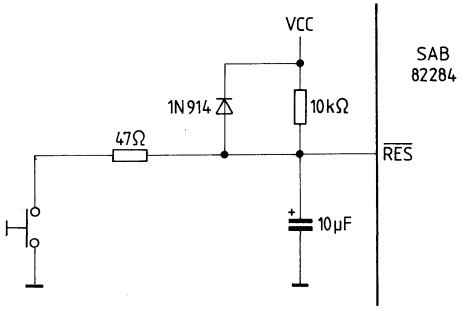
The figure on asynchronous ready mode shows the operation of $\overline{ARDY}$ and $\overline{ARDYEN}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is high. If the synchronizer resolved both the $\overline{ARDY}$ and $\overline{ARDYEN}$ inputs to have been active (low), $\overline{READY}$ becomes active (low) and the $\overline{SRDY}$ and $\overline{SRDYEN}$ inputs are ignored.

$\overline{READY}$ remains active until either $\overline{S1}$ or $\overline{S0}$ is sampled low, or the ready inputs are sampled as inactive.

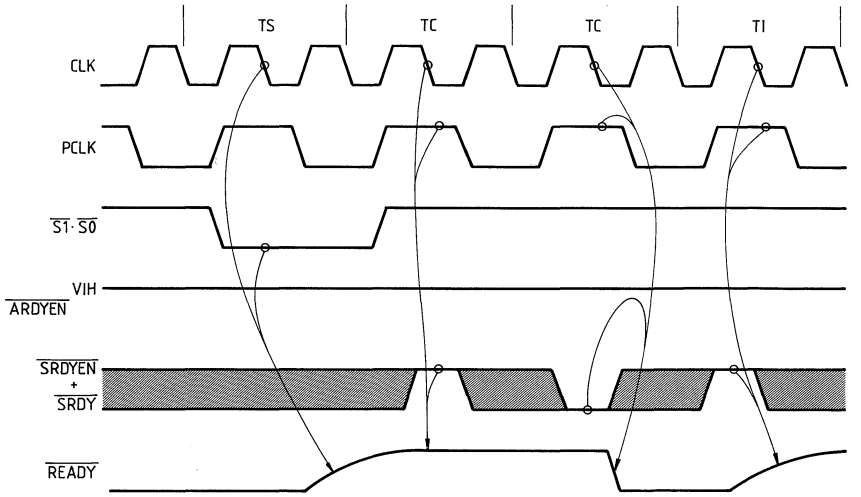
$\overline{READY}$ is enabled (low), if either $\overline{SRDY}$ + $\overline{SRDYEN}$ = 0 or $\overline{ARDY}$ + $\overline{ARDYEN}$ = 0 when sampled by the SAB 82284 $\overline{READY}$ generation logic. $\overline{READY}$ will remain active for at least two CLK cycles.

The $\overline{READY}$ output has an open-collector driver allowing other ready circuits to be wire-ORed with it. The $\overline{READY}$ signal of an SAB 80286 system requires an external pullup resistor (see Note 6 of AC Characteristics). To force the $\overline{READY}$ signal inactive (high) at the start of a bus cycle, the $\overline{READY}$ output floats when either $\overline{S1}$ or $\overline{S0}$ are sampled low at the falling edge of CLK. Two system clock periods are allowed for the pullup resistor to pull the $\overline{READY}$ signal to VIH. When RESET is active, $\overline{READY}$ is forced active one CLK later (see waveforms).

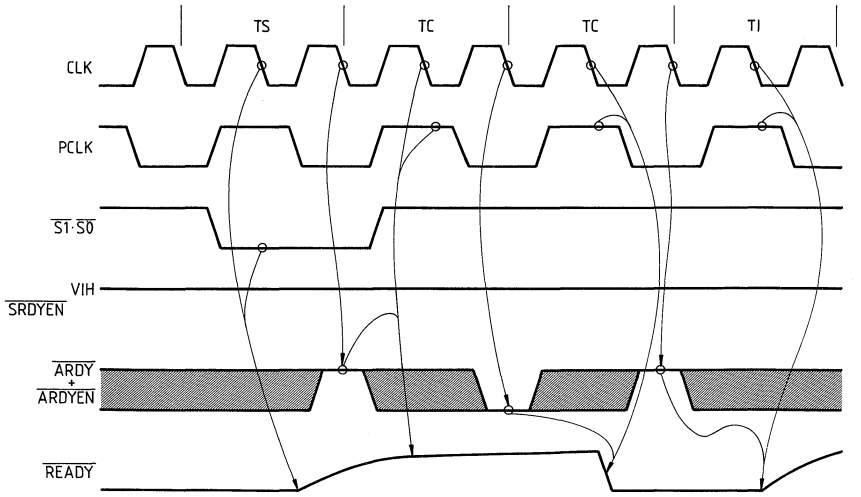
Typical RC $\overline{RES}$ Timing Circuit



Synchronous Ready Operation



Asynchronous Ready Operation



Absolute Maximum Ratings [1)]

Temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
All output and supply voltages	−0.5 to +7V
All input voltages	−1.0 to +5.5V
Power dissipation	1 W

DC Characteristics

TA = 0 to 70°C, VCC = 5 V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
IF	Forward input current	–	−0.5	mA	VF = 0.45V
IR	Reverse input current	–	50	µA	VR = VCC
VC	Input forward clamp voltage	–	−1.0	V	IC = −5mA
ICC	Power supply current	–	145	mA	–
VIL	Input low voltage	–	0.8	V	–
VIH	Input high voltage	2.0	–	V	–
VOL, VCL	Output low voltage	–	0.45	V	IOL = 5mA (8.5 mA at $\overline{\text{READY}}$)
VCH	CLK output high voltage	4.0	–	V	IOH = −1mA
VOH	Output high voltage	2.4	–	V	IOH = −1mA
VIHR	$\overline{\text{RES}}$ input high voltage	2.6	–	V	–
VIHR – VILR	$\overline{\text{RES}}$ input hysteresis	0.25	–	V	–
CI	Input capacitance	–	10	pF	fC = 1 MHz

[1)] Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics SAB 82284

TA = 0 to 70°C, VCC = 5V ±10%
AC timings are referenced to 0.8 and 2.0V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
T1	EFI to CLK delay	–	30	ns	at 1.5V 1)
T2	EFI low time	22	–	ns	at 1.5V 1) 2)
T3	EFI high time	30	–	ns	at 1.5V 1) 2)
T4	CLK period	62	500	ns	–
T5	CLK low time	15	–	ns	at 1.0V 1) 2) 3) 4)
T6	CLK high time	25	–	ns	at 3.6V 1) 2) 3) 4)
T7	CLK rise time	–	10	ns	from 1.0V to 3.6V 1)
T8	CLK fall time	–	10	ns	from 3.6V to 1.0V 1)
T9	Status setup time	22.5	–	ns	1)
T10	Status hold time	1	–	ns	1)
T11	$\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ setup time	15	–	ns	1)
T12	$\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ hold time	0	–	ns	1)
T13	$\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ setup time	0	–	ns	1) 5)
T14	$\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ hold time	30	–	ns	1) 5)
T15	$\overline{\text{RES}}$ setup time	20	–	ns	1) 5)
T16	$\overline{\text{RES}}$ hold time	10	–	ns	1) 5)
T17	$\overline{\text{READY}}$ inactive delay	5	–	ns	at 0.8V 6)
T18	$\overline{\text{READY}}$ active delay	0	24	ns	at 0.8V 6)
T19	PCLK delay	0	45	ns	7)
T20	RESET delay	5	34	ns	7)
T21	PCLK low time	T4–20	–	ns	at 0.6V 7) 8)
T22	PCLK high time	T4–20	–	ns	at 2.0V 7) 8)

For notes refer to page 10.

AC Characteristics SAB 82284-1

TA = 0 to 70°C, VCC = 5 V ±10%
AC timings are referenced to 0.8 and 2.0V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
T1	EFI to CLK delay	–	30	ns	at 1.5 V [1]
T2	EFI low time	25	–	ns	at 1.5 V [1] [2]
T3	EFI high time	25	–	ns	at 1.5 V [1] [2]
T4	CLK period	50	500	ns	–
T5	CLK low time	12	–	ns	at 1.0 V [1] [2] [3] [4]
T6	CLK high time	16	–	ns	at 3.6 V [1] [2] [3] [4]
T7	CLK rise time	–	8	ns	from 1.0 V to 3.6 V [1]
T8	CLK fall time	–	8	ns	from 3.6 V to 1.0 V [1]
T9	Status setup time	20	–	ns	[1]
T10	Status hold time	1	–	ns	[1]
T11	$\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ setup time	15	–	ns	[1]
T12	$\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ hold time	0	–	ns	[1]
T13	$\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ setup time	0	–	ns	[1] [5]
T14	$\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ hold time	30	–	ns	[1] [5]
T15	$\overline{\text{RES}}$ setup time	20	–	ns	[1] [5]
T16	$\overline{\text{RES}}$ hold time	10	–	ns	[1] [5]
T17	$\overline{\text{READY}}$ inactive delay	5	–	ns	at 0.8 V [6]
T18	$\overline{\text{READY}}$ active delay	0	24	ns	at 0.8 V [6]
T19	PCLK delay	0	35	ns	[7]
T20	RESET delay	5	27	ns	[7]
T21	PCLK low time	T4–20	–	ns	at 0.6 V [7] [8]
T22	PCLK high time	T4–20	–	ns	at 2.0 V [7] [8]

For notes refer to page 10.

Notes referring to AC Characteristics:

1) CLK loading: CL = 150 pF.
The SAB 82284's X1 and X2 inputs are designed primarily for parallel resonant crystals. Serial resonant crystals may oscillate up to 0.01% faster than their rated frequencies, when used with the SAB 82284. For either type capacitive loading should be according to the crystal loading table.

2) At CLK frequencies above 12 MHz, CLK high and low times are guaranteed only when using a crystal with recommended capacitive loading (see table), not when driving the component from EFI input.

3) With either the internal oscillator and recommended crystal and load or with the EFI input meeting specifications T2 and T3. The values from the crystal loading table are ± 5 pF and include all stray capacitances. Decouple VCC and GND as close to the SAB 82284 as possible.

4) When using a crystal (with recommended load) appropriate for speed of the SAB 80286, CLK output low and high times are guaranteed to meet the SAB 80286 requirements.

5) This is an asynchronous input. The specification is given for testing purposes only, to assure recognition at a specific clock edge.

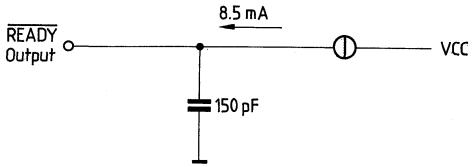
6) $\overline{\text{READY}}$ loading: CL = 150 pF, pullup resistor RP, with RP = 910 Ω.

7) PCLK and RESET loading: CL = 75 pF. PCLK output with 750 Ω pullup resistor.

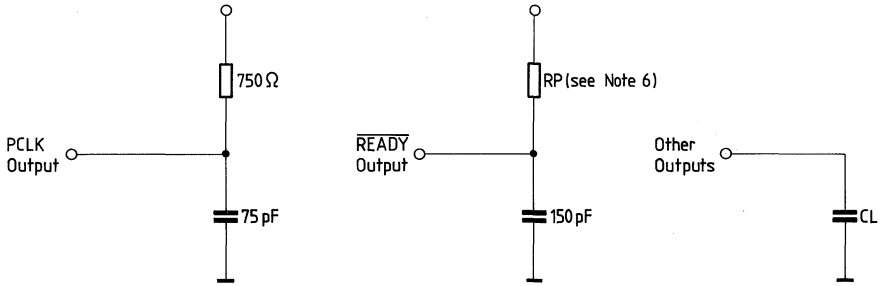
8) T4 refers to any allowable CLK period.

Testing Waveforms

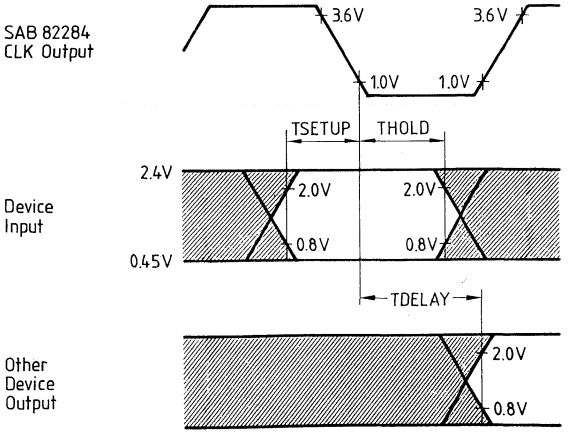
DC Test Loadings



AC Test Loadings

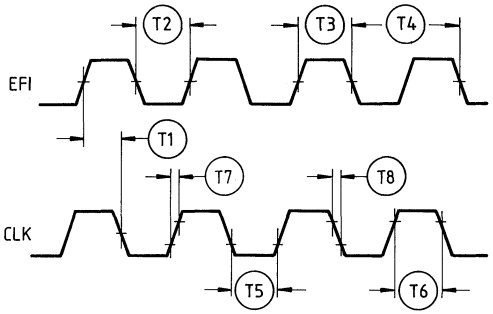


Setup, Hold and Delay Time Measurement – General



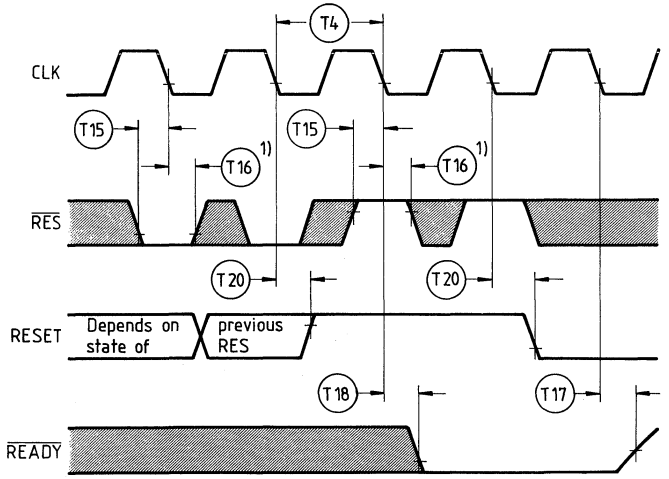
Waveforms

CLK versus EFI



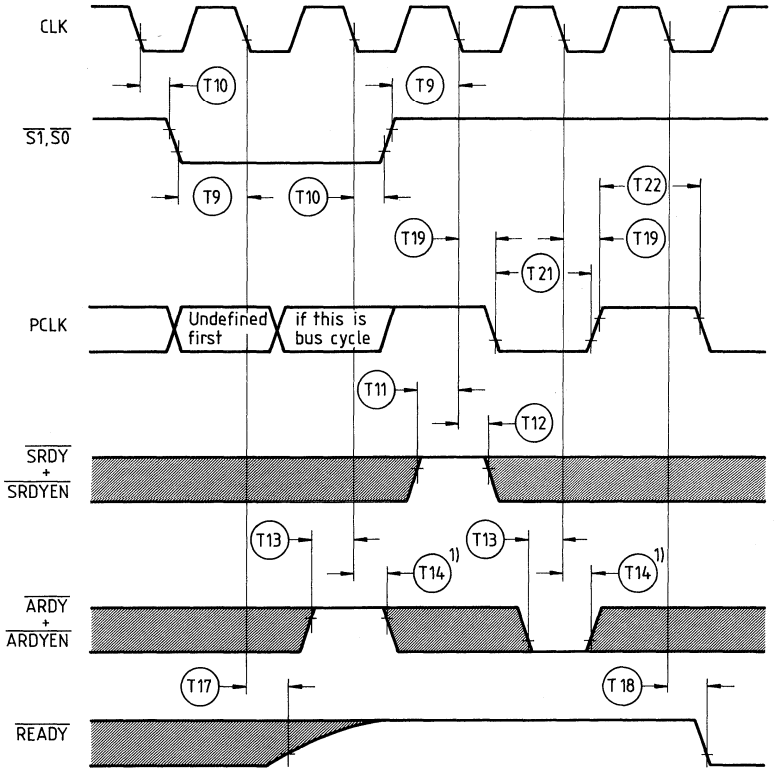
The EFI input low and high times as shown are required to guarantee the CLK low and high times shown.

RESET and $\overline{\text{READY}}$ Timing versus $\overline{\text{RES}}$ with $\overline{\text{S1}}$ and $\overline{\text{S0}}$ High



[1] This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
[2] One or two CLK cycles depending on PCLK phase.

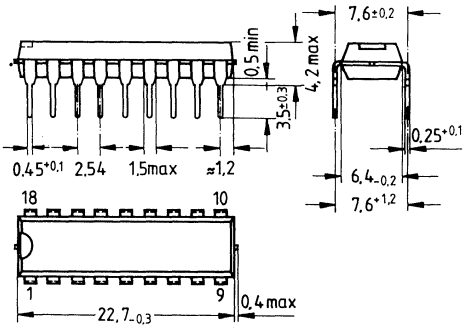
$\overline{\text{READY}}$ and PCLK Timing with $\overline{\text{RES}}$ High



[1] This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

Package Outlines

18-Pin Plastic Package, P-DIP



Dimensions in mm

Ordering Information

Type	Description	Ordering code
SAB 82284-P	Clock generator (plastic package) up to 16 MHz	Q67020-Y162
SAB 82284-1-P	Clock generator (plastic package) up to 20 MHz	Q67020-Y167

SAB 82C284 Clock Generator and Ready Interface for SAB 80286 Processors

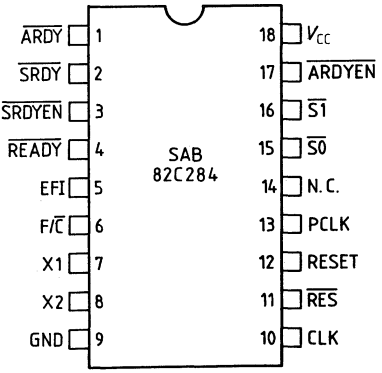
SAB 82C284-1 up to 20 MHz

- Generates system clock for SAB 80286 processors
- Uses crystal or TTL signal for frequency source
- Provides local $\overline{\text{READY}}$ and multimaster system bus $\overline{\text{READY}}$ synchronization

SAB 82C284-12 up to 25 MHz

- 18-pin plastic package, P-DIP-18
- Single +5 V power supply
- Generates system reset output from Schmitt-trigger input

Pin Configuration



Pin Names

CLK	System Clock
F/$\overline{C}$	Frequency/Crystal Select
X1, X2	Crystal In
EFI	External Frequency In
PCLK	Peripheral Clock
$\overline{\text{ARDYEN}}$	Asynchronous Ready Enable
$\overline{\text{ARDY}}$	Asynchronous Ready
$\overline{\text{SRDYEN}}$	Synchronous Ready Enable
$\overline{\text{SRDY}}$	Synchronous Ready
$\overline{\text{READY}}$	Bus Cycle Termination
$\overline{\text{S0}}$, $\overline{\text{S1}}$	Status
RESET	Reset
$\overline{\text{RES}}$	Reset In
V_{CC}	Power supply (+5V)
GND	Ground (0V)

The SAB 82C284 is a CMOS clock generator/driver which provides clock signals for SAB 80286 processors and support components. It also contains logic to supply $\overline{\text{READY}}$ to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

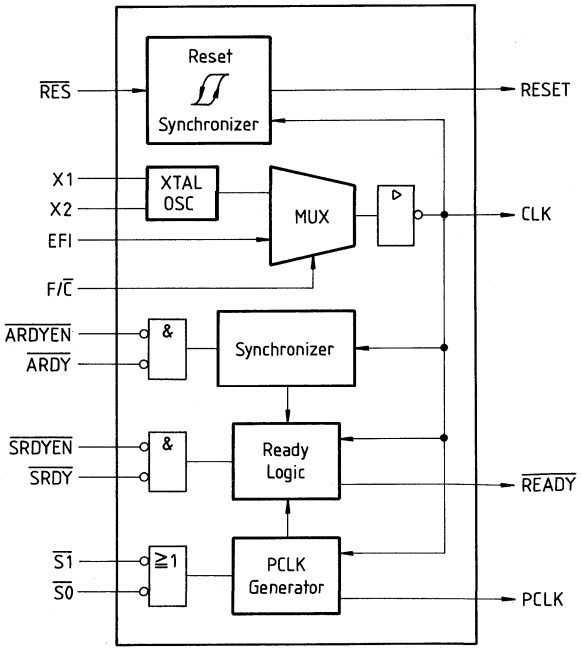
Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{ARDY}}$	1	I	**ASYNCHRONOUS READY** is an active low input used to terminate the current bus cycle. The $\overline{\text{ARDY}}$ input is qualified by $\overline{\text{ARDYEN}}$. Inputs to $\overline{\text{ARDY}}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
$\overline{\text{SRDY}}$	2	I	**SYNCHRONOUS READY** is an active low input used to terminate the current bus cycle. The $\overline{\text{SRDY}}$ input is qualified by the $\overline{\text{SRDYEN}}$ input. Setup and hold times must be satisfied for proper operation.
$\overline{\text{SRDYEN}}$	3	I	**SYNCHRONOUS READY ENABLE** is an active low input which qualifies $\overline{\text{SRDY}}$. $\overline{\text{SRDYEN}}$ selects $\overline{\text{SRDY}}$ as the source for $\overline{\text{READY}}$ to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.
$\overline{\text{READY}}$	4	O	**READY** is an active low output which signals the current bus cycle to be completed. The $\overline{\text{SRDY}}$, $\overline{\text{SRDYEN}}$, $\overline{\text{ARDY}}$, $\overline{\text{ARDYEN}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$ and $\overline{\text{RES}}$ inputs control $\overline{\text{READY}}$ as explained later in the $\overline{\text{READY}}$ generator section. $\overline{\text{READY}}$ is an open collector output requiring an external pullup resistor.
EFI	5	I	**EXTERNAL FREQUENCY IN** drives CLK when the F/$\overline{\text{C}}$ input is strapped high. The EFI input frequency must be twice the desired internal processor clock frequency.
F/$\overline{\text{C}}$	6	I	**FREQUENCY/CRYSTAL SELECT** is a strapping option to select the source for the CLK output. When F/$\overline{\text{C}}$ is strapped low, the internal crystal oscillator drives CLK. When F/$\overline{\text{C}}$ is strapped high, the EFI input drives the CLK output.
X1, X2	7, 8	I	**CRYSTAL IN** are the pins to which a parallel resonant fundamental mode crystal is attached for the internal oscillator. When F/$\overline{\text{C}}$ is low, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.
CLK	10	O	**SYSTEM CLOCK** is the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and MOS level inputs.
$\overline{\text{RES}}$	11	I	**RESET IN** is an active low input which generates the system reset signal RESET. Signals to $\overline{\text{RES}}$ may be applied asynchronously to CLK. A Schmitt-trigger input is provided on $\overline{\text{RES}}$, so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
RESET	12	O	**RESET** is an active high output which is derived from the $\overline{\text{RES}}$ input. RESET is used to force the system into an initial state. When RESET is active, $\overline{\text{READY}}$ will be active low.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
PCLK	13	O	**PERIPHERAL CLOCK** is an output which provides a 50% duty cycle clock with 1/2 the frequency of CLK. PCLK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
$\overline{S0}$, $\overline{S1}$	15,16	I	**STATUS** inputs prepare the SAB 82C284 for a subsequent bus cycle. $\overline{S0}$ and $\overline{S1}$ synchronize PCLK to the internal processor clock and control $\overline{READY}$. These inputs have pullup resistors to keep them high if nothing is driving them. Setup and hold times must be satisfied for proper operation.
$\overline{ARDYEN}$	17	I	**ASYNCHRONOUS READY ENABLE** is an active low input which qualifies the $\overline{ARDY}$ input. $\overline{ARDYEN}$ selects $\overline{ARDY}$ as the source of ready for the current bus cycle. Inputs to $\overline{ARDYEN}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
V_{CC}	18	–	**POWER SUPPLY** (+5 V)
GND	9	–	**GROUND** (0 V)

Block Diagram



Functional Description

Introduction

The SAB 82C284 generates the clock, ready, and reset signals required for SAB 80286 processors and support components. The SAB 82C284 is packaged in an 18-pin P-DIP package and contains a crystal-controlled oscillator, CMOS clock generator, peripheral clock generator, Multibus ready synchronization logic, and system reset generation logic.

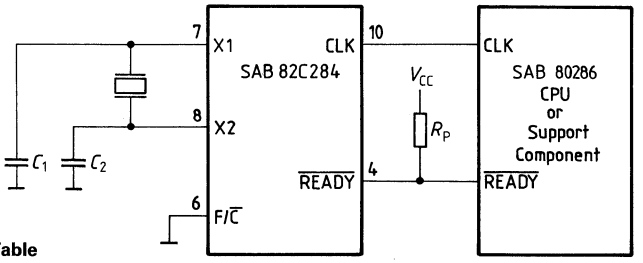
Clock generator

The CLK output provides the basic timing control for an SAB 80286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the F/$\overline{C}$ strapping option. When F/$\overline{C}$ is low, the crystal oscillator drives the CLK output. When F/$\overline{C}$ is high, the EFI input drives the CLK output. The SAB 82C284 provides a second clock output (PCLK) for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and TTL output drive characteristics. PCLK is normally synchronized to the internal processor clock. After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its high time beyond one system clock (see waveforms). PCLK is forced high whenever either $\overline{S0}$ or $\overline{S1}$ were active low for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are high.
Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

Oscillator

The oscillator circuit of the SAB 82C284 is a linear Pierce oscillator which requires an external, parallel, resonant, fundamental-mode crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32 pF.
X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in the figure below. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10 pF between the X1 and X2 pins.
Decouple V_{CC} and GND as close to the SAB 82C284 as possible.

Recommended Crystal and $\overline{\text{READY}}$ Connections
(For RP see Note 6 of AC Characteristics)



Crystal Loading Table

$C_1 = 22$ pF

$C_2 = 15$ pF

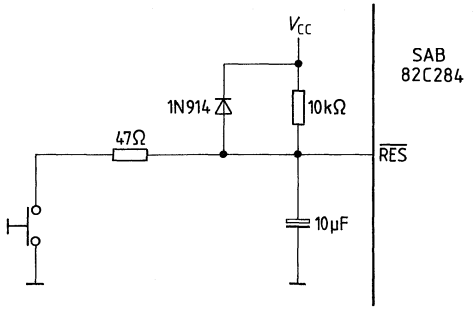
Reset Operation

The reset logic provides the RESET output to force the system into a known initial state. When the $\overline{RES}$ input is active low, the RESET output becomes active high. $\overline{RES}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the $\overline{RES}$ input introduces a one or two CLK delay before affecting the RESET output.
At power up, a system has no stable V_{CC} and CLK. To prevent spurious activity, $\overline{RES}$ should be asserted until V_{CC} and CLK have stabilized at their operating values. SAB 80286 processors and support components also require their RESET inputs be high for a minimum number of CLK cycles. An RC network, as shown below, will keep $\overline{RES}$ low long enough to satisfy both needs.
A Schmitt-trigger input with hysteresis on $\overline{RES}$ assures a single transition of RESET with an RC circuit on $\overline{RES}$. The hysteresis separates the input voltage level at which the circuit output switches from high to low from the input voltage level at which the circuit output switches from low to high. The $\overline{RES}$ high-to-low input transition voltage is lower than the $\overline{RES}$ low-to-high input transition voltage. As long as the slope of the $\overline{RES}$ input voltage remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input transition voltage, the RESET output will make a single transition.

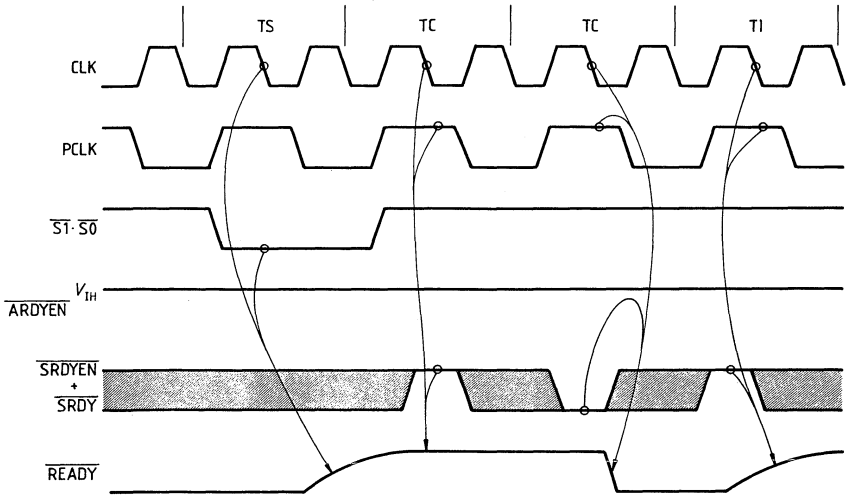
Ready Operation

The SAB 82C284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous ($\overline{SRDY}$) or asynchronous ready ($\overline{ARDY}$) source may be used. Each ready input has an enable ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.
The figure on synchronous ready mode illustrates the operation of $\overline{SRDY}$ and $\overline{SRDYEN}$. These inputs are sampled on the falling edge of CLK when $\overline{S1}$ and $\overline{S0}$ are inactive and PCLK is high. $\overline{READY}$ is forced active when both $\overline{SRDY}$ and $\overline{SRDYEN}$ are sampled as low.
The figure on asynchronous ready mode shows the operation of $\overline{ARDY}$ and $\overline{ARDYEN}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is high. If the synchronizer resolved both the $\overline{ARDY}$ and $\overline{ARDYEN}$ inputs to have been active low, $\overline{READY}$ becomes active low and the $\overline{SRDY}$ and $\overline{SRDYEN}$ inputs are ignored.
$\overline{READY}$ remains active until either $\overline{S1}$ or $\overline{S0}$ is sampled low, or the ready inputs are sampled as inactive.
$\overline{READY}$ is enabled low, if either $\overline{SRDY}$ + $\overline{SRDYEN}$ = 0 or $\overline{ARDY}$ + $\overline{ARDYEN}$ = 0 when sampled by the SAB 82C284 $\overline{READY}$ generation logic. $\overline{READY}$ will remain active for at least two CLK cycles.
The $\overline{READY}$ output has an open-collector driver allowing other ready circuits to be wire-ORed with it. The $\overline{READY}$ signal of an SAB 80286 system requires an external pullup resistor (see Note 6 of AC Characteristics). To force the $\overline{READY}$ signal inactive high at the start of a bus cycle, the $\overline{READY}$ output floats when either $\overline{S1}$ or $\overline{S0}$ are sampled low at the falling edge of CLK. Two system clock periods are allowed for the pullup resistor to pull the $\overline{READY}$ signal to V_{IH}. When RESET is active, $\overline{READY}$ is forced active one CLK later (see waveforms).

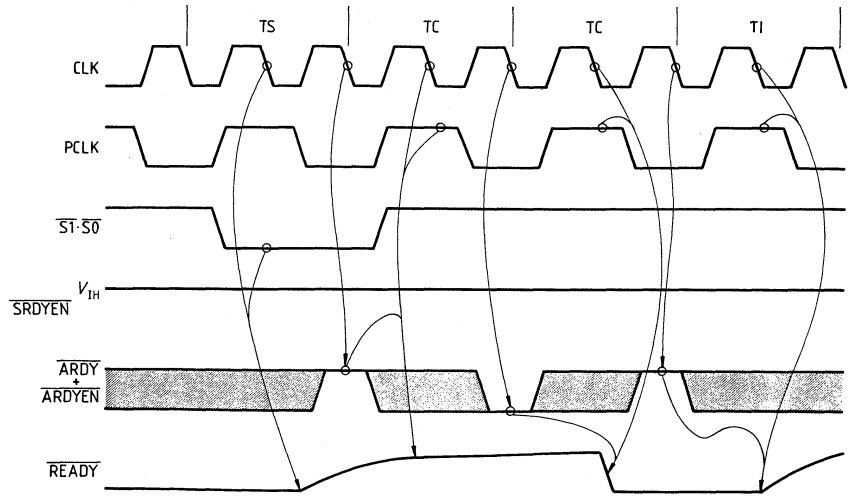
Typical RC $\overline{RES}$ Timing Circuit



Synchronous Ready Operation



Asynchronous Ready Operation



Absolute Maximum Ratings

Temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
All output and supply voltages	−0.5 to +7V
All input voltages	−1.0 to +5.5V
Power dissipation	1 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ±10%

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Forward input current ($\overline{S0}$, $\overline{S1}$)	I_F	–	−0.5	mA	V_F = 0.45V
Input leakage current (all others)	I_{LI}	–	±10	µA	0V ≤ V_{IN} ≤ V_{CC}
Power supply current	I_{CC}	–	75	mA	@ 25 MHz
Input low voltage	V_{IL}	–	0.8	V	–
Input high voltage	V_{IH}	2.0	–	V	–
Output low voltage	V_{OL}, V_{CL}	–	0.45	V	I_{OL} = 5mA (9mA at $\overline{READY}$)
CLK output high voltage	V_{CH}	4.0	–	V	I_{OH} = −1mA
Output high voltage	V_{OH}	2.4	–	V	I_{OH} = −1mA
$\overline{RES}$ input high voltage	V_{IHR}	2.6	–	V	–
$\overline{RES}$ input hysteresis	$V_{IHR} - V_{ILR}$	0.25	–	V	–
Input capacitance	C_I	–	10	pF	f_C = 1 MHz

Capacitance

T_A = 25°C, V_{CC} = GND = 0 V, f_c = 1 MHz

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
Input capacitance	C_I	–	10	pF	Unsampled pins returned to GND

Note: Not 100% tested, guaranteed by design characterization.

AC Characteristics SAB 82C284-12

T_A = 0 to 70°C, V_{CC} = 5V±10%
AC timings are referenced to 0.8 and 2.0V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
EFI to CLK delay	t_1	–	25	ns	at 1.5V 1)
EFI low time	t_2	18	–	ns	at 1.5 V 1)
EFI high time	t_3	18	–	ns	at 1.5V 1)
CLK period	t_4	40	500	ns	–
CLK low time	t_5	11	–	ns	at 1.0 V 1) 3) 4)
CLK high time	t_6	13	–	ns	at 3.6 V 1) 3) 4)
CLK rise time	t_7	–	8	ns	from 1.0 V to 3.6 V 1)
CLK fall time	t_8	–	8	ns	from 3.6 V to 1.0 V 1)
Status setup time	t_9	18	–	ns	1)
Status hold time	t_{10}	3	–	ns	1)
$\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ setup time	t_{11}	15	–	ns	1)
$\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ hold time	t_{12}	2	–	ns	1)
$\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ setup time	t_{13}	0	–	ns	1) 5)
$\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ hold time	t_{14}	25	–	ns	1) 5)
$\overline{\text{RES}}$ setup time	t_{15}	18	–	ns	1) 5)
$\overline{\text{RES}}$ hold time	t_{16}	8	–	ns	1) 5)
$\overline{\text{READY}}$ inactive delay	t_{17}	5	–	ns	at 0.8 V 6)
$\overline{\text{READY}}$ active delay	t_{18}	0	18	ns	at 0.8 V 6)
PCLK delay	t_{19}	0	23	ns	7)
RESET delay	t_{20}	3	22	ns	7)
PCLK low time	t_{21}	t_4–20	–	ns	at 0.6 V 7) 8)
PCLK high time	t_{22}	t_4–20	–	ns	at 2.0 V 7) 8)

For notes refer to page 10.

AC Characteristics SAB 82C284-1

T_A = 0 to 70°C, V_{CC} = 5 V±10%
AC timings are referenced to 0.8 and 2.0 V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Parameter	Symbol	Limit values		Unit	Test conditions
		min.	max.		
EFI to CLK delay	t_1	–	30	ns	at 1.5 V 1)
EFI low time	t_2	25	–	ns	at 1.5 V 1)
EFI high time	t_3	25	–	ns	at 1.5 V 1)
CLK period	t_4	50	500	ns	–
CLK low time	t_5	12	–	ns	at 1.0 V 1) 2) 3)
CLK high time	t_6	16	–	ns	at 3.6 V 1) 2) 3)
CLK rise time	t_7	–	8	ns	from 1.0 V to 3.6 V 1)
CLK fall time	t_8	–	8	ns	from 3.6 V to 1.0 V 1)
Status setup time	t_9	20	–	ns	1)
Status hold time	t_{10}	1	–	ns	1)
$\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ setup time	t_{11}	15	–	ns	1)
$\overline{\text{SRDY}}$ + $\overline{\text{SRDYEN}}$ hold time	t_{12}	2	–	ns	1)
$\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ setup time	t_{13}	0	–	ns	1) 4)
$\overline{\text{ARDY}}$ + $\overline{\text{ARDYEN}}$ hold time	t_{14}	30	–	ns	1) 4)
$\overline{\text{RES}}$ setup time	t_{15}	20	–	ns	1) 4)
$\overline{\text{RES}}$ hold time	t_{16}	10	–	ns	1) 4)
$\overline{\text{READY}}$ inactive delay	t_{17}	5	–	ns	at 0.8 V 5)
$\overline{\text{READY}}$ active delay	t_{18}	0	24	ns	at 0.8 V 5)
PCLK delay	t_{19}	0	35	ns	6)
RESET delay	t_{20}	5	27	ns	6)
PCLK low time	t_{21}	t_4–20	–	ns	at 0.6 V 6) 7)
PCLK high time	t_{22}	t_4–20	–	ns	at 2.0 V 6) 7)

For notes refer to page 10.

Notes referring to AC Characteristics:

1) CLK loading: $C_L = 150$ pF.
The SAB 82C284's X1 and X2 inputs are designed primarily for parallel resonant crystals. Serial resonant crystals may oscillate up to 0.01% faster than their rated frequencies, when used with the SAB 82C284. For either type capacitive loading should be according to the recommendation.

2) With either the internal oscillator and recommended crystal and load or with the EFI input meeting specifications t_2 and t_3. The values from the crystal loading table are ± 5 pF and include all stray capacitances. Decouple V_{CC} and GND as close to the SAB 82C284 as possible.

3) When using a crystal (with recommended load) appropriate for speed of the SAB 80286, CLK output low and high times are guaranteed to meet the SAB 80286 requirements.

4) This is an asynchronous input. The specification is given for testing purposes only to assure recognition at a specific clock edge.

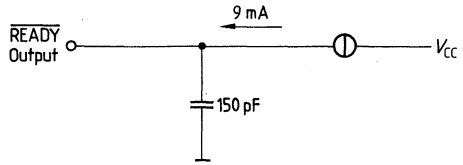
5) $\overline{\text{READY}}$ loading: $C_L = 150$ pF, pullup resistor $R_P = 910\ \Omega$.

6) PCLK and RESET loading: $C_L = 75$ pF. PCLK output with $750\ \Omega$ pullup resistor.

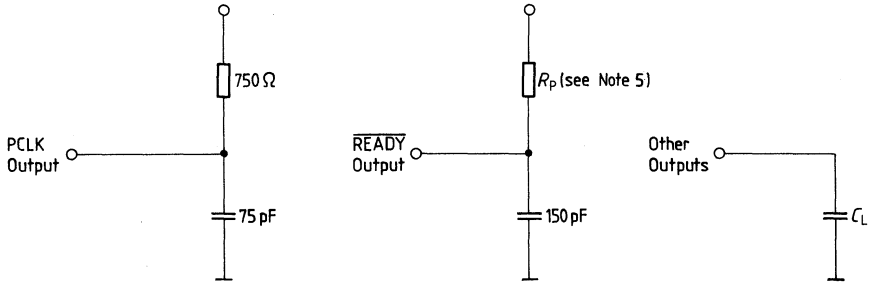
7) t_4 refers to any allowable CLK period.

Testing Waveforms

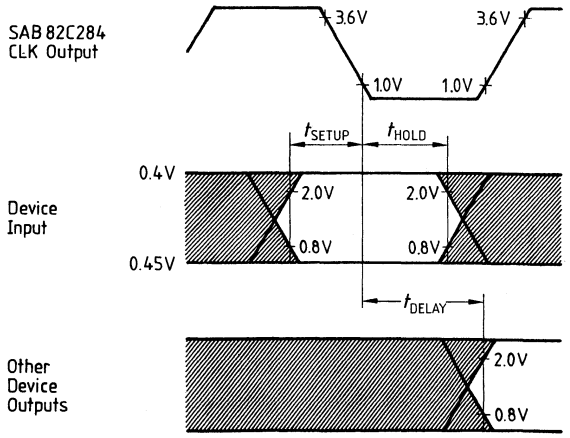
DC Test Loadings



AC Test Loadings

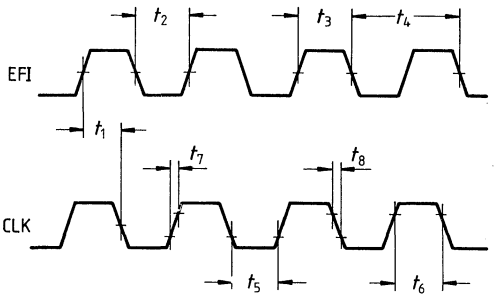


Setup, Hold and Delay Time Measurement – General



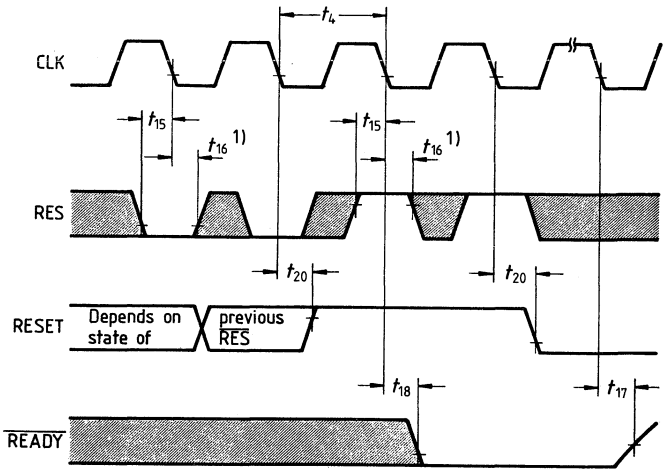
Waveforms

CLK versus EFI



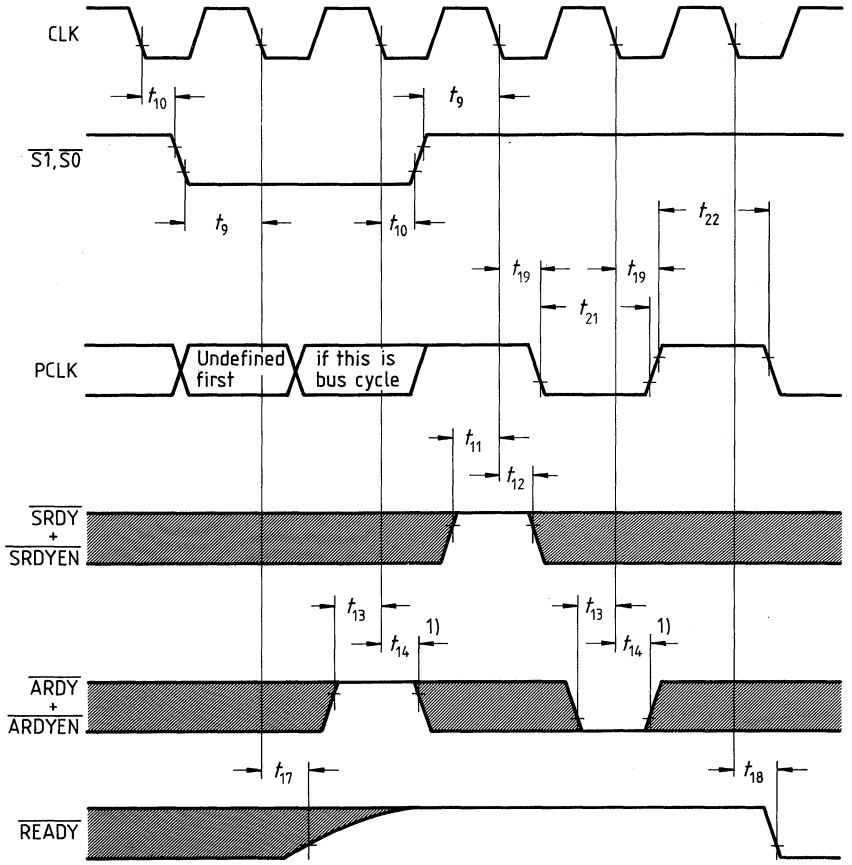
The EFI input low and high times as shown are required to guarantee the CLK low and high times shown.

RESET and READY Timing versus RES with S1 and S0 High



1) This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.
2) One or two CLK cycles depending on PCLK phase.

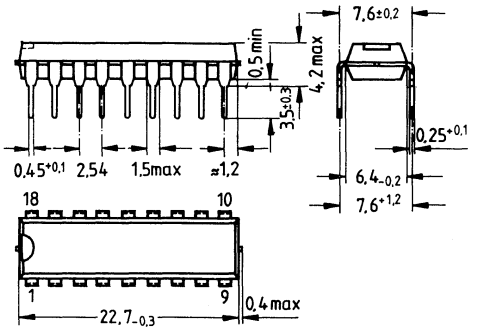
$\overline{\text{READY}}$ and PCLK Timing with $\overline{\text{RES}}$ High



[1] This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

Package Outlines

18-Pin Plastic Package, P-DIP-18



Dimensions in mm

Ordering Information

Type	Ordering code	Description
SAB 82C284-1-P	Q67120-P261	Clock generator (plastic package) up to 20 MHz
SAB 82C284-12-P	Q67120-P262	Clock generator (plastic package) up to 25 MHz

Preliminary

SAB 82288 Bus Controller for SAB 80286 Processors

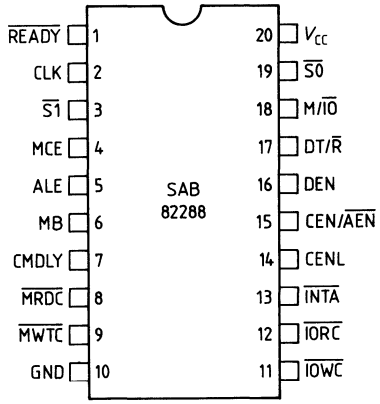
SAB 82288-6 up to 12 MHz
SAB 82288 up to 16 MHz

- Provides commands and control for local and system bus
- Offers wide flexibility in system configurations
- Flexible command timing

SAB 82288-1 up to 20 MHz

- Optimal Multibus ™-compatible timing
- Control drivers with 16 mA I_{OL} and tristate command drivers with 32 mA I_{OL}
- Single +5 V supply

Pin Configuration



Pin Names

CLK	System Clock
$\overline{S0}$, $\overline{S1}$	Bus Cycle Status
M/$\overline{IO}$	Memory or I/O Select
MB	Multibus Mode Select
CENL	Command Enable Latched
CMDLY	Command Delay
$\overline{READY}$	Bus Cycle Termination
CEN/$\overline{AEN}$	Command Enable/Address Enable
ALE	Address Latch Enable
MCE	Master Cascade Enable
DEN	Data Enable
DT/$\overline{R}$	Data Transmit/Receive
$\overline{IOWC}$	I/O Write Command
$\overline{IORC}$	I/O Read Command
$\overline{MWTC}$	Memory Write Command
$\overline{MRDC}$	Memory Read Command
$\overline{INTA}$	Interrupt Acknowledge
V_{CC}	Power supply (+5 V)
GND	Ground (0 V)

The SAB 82288 bus controller is a 20-pin MYMOS component for use in SAB 80286 microsystems. The bus controller provides command and control outputs with flexible timing options. Separate command outputs are used for memory and I/O devices. The data bus is controlled with separate data enable and direction control signals. Two modes of operation are possible: Multibus-compatible bus cycles, and high-speed bus cycles.

Multibus ™ is a trademark of Intel Corporation.

Pin Definitions and Functions

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{\text{READY}}$</td><td>1</td><td>I</td><td>$\overline{\text{READY}}$ indicates the end of the current bus cycle. $\overline{\text{READY}}$ is an active low input. Multibus mode requires at least one wait state to allow the command outputs to become active. $\overline{\text{READY}}$ must be low during reset, to force the SAB 82288 into the idle state. Setup and hold times must be met for proper operation.</td></tr>
<tr><td>CLK</td><td>2</td><td>I</td><td>SYSTEM CLOCK provides the basic timing control for the SAB 82288 in an SAB 80286 microsystem. Its frequency is twice the internal processor clock frequency. The falling edge of this input signal establishes when inputs are sampled and control outputs change.</td></tr>
<tr><td>$\overline{\text{S0}}$, $\overline{\text{S1}}$</td><td>3, 19</td><td>I</td><td>BUS CYCLE STATUS starts a bus cycle and, along with M/$\overline{\text{IO}}$, defines the type of bus cycle. These inputs are active low. A bus cycle is started when either $\overline{\text{S1}}$ or $\overline{\text{S0}}$ is sampled low at the falling edge of CLK. These inputs have pullup resistors sufficient to hold them high when nothing drives them. Setup and hold times must be met for proper operation.
<table>
<tr><th colspan="4">SAB 80286 bus cycle status definition</th></tr>
<tr><th>M/$\overline{\text{IO}}$</th><th>$\overline{\text{S1}}$</th><th>$\overline{\text{S0}}$</th><th>Type of bus cycle</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>I/O read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I/O write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>None; idle</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Halt or shutdown</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Memory read</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Memory write</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>None; idle</td></tr>
</table></td></tr>
<tr><td>MCE</td><td>4</td><td>O</td><td>MASTER CASCADE ENABLE signals that a cascade address from a master SAB 8259A interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. This control output is active high. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.</td></tr>
<tr><td>ALE</td><td>5</td><td>O</td><td>ADDRESS LATCH ENABLE controls the address latches used to hold an address stable during a bus cycle. This control output is active high. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.</td></tr>
<tr><td>MB</td><td>6</td><td>I</td><td>MULTIBUS MODE SELECT determines timing of the command and control outputs. When high, the bus controller operates in Multibus mode. When low, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/$\overline{\text{AEN}}$ input pin is selected by this signal. Typically, this input is a strapping option and not dynamically changed. This input may be connected to V_{CC} or GND.</td></tr>
</table>

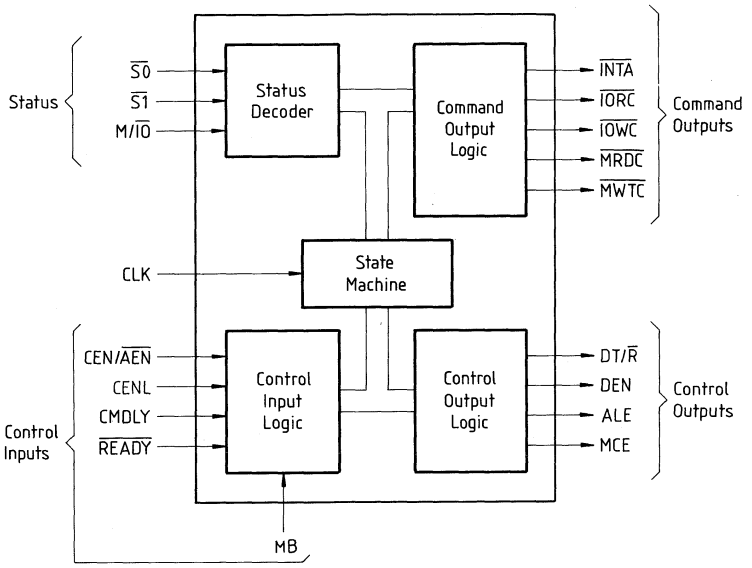
Pin Definitions and Function (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CMDLY	7	I	COMMAND DELAY allows delaying the start of a command. CMDLY is an active high input. If sampled high, the command output is not activated and CMDLY is again sampled at the next CLK cycle. When sampled low the selected command is enabled. If $\overline{\text{READY}}$ is detected low before the command output is activated, the SAB 82288 will terminate the bus cycle, even if no command was issued. Setup and hold times must be satisfied for proper operation. This input may be connected to GND if no delays are required before starting a command.
$\overline{\text{MRDC}}$	8	O	$\overline{\text{MEMORY READ COMMAND}}$ instructs the memory device to place data onto the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{MWTC}}$	9	O	$\overline{\text{MEMORY WRITE COMMAND}}$ instructs a memory device to read the data on the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{IOWC}}$	11	O	$\overline{\text{I/O WRITE COMMAND}}$ instructs an I/O device to read the data on the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{IORC}}$	12	O	$\overline{\text{I/O READ COMMAND}}$ instructs an I/O device to place data onto the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{INTA}}$	13	O	$\overline{\text{INTERRUPT ACKNOWLEDGE}}$ tells an interrupting device that its interrupt request is being acknowledged. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
CENL	14	I	COMMAND ENABLE LATCHED is a bus controller select signal which enables the bus controller to respond to the current bus cycle being initiated. CENL is an active high input latched internally at the start of each bus cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. This input may be connected to V_{CC} to select this SAB 82288 for all transfers. No control inputs affect CENL. Setup and hold times must be met for proper operation.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CEN/$\overline{\text{AEN}}$	15	I	COMMAND ENABLE/$\overline{\text{ADDRESS ENABLE}}$ controls the command and DEN outputs of the bus controller. CEN/$\overline{\text{AEN}}$ inputs may be asynchronous to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs. This input may be connected to V_{CC} or GND. When MB is high this pin has the $\overline{\text{AEN}}$ function. $\overline{\text{AEN}}$ is an active low input which indicates that the CPU has been granted use of a shared bus and the bus controller command outputs may exit tristate off and become inactive (high). $\overline{\text{AEN}}$ high indicates that the CPU does not have control of the shared bus and forces the command outputs into tristate off and DEN inactive (low). $\overline{\text{AEN}}$ would normally be controlled by an SAB 82289 bus arbiter which activates $\overline{\text{AEN}}$ when that arbiter owns the bus to which the bus controller is attached. When MB is low this pin has the CEN function. CEN is an unlatched active high input which allows the bus controller activate its command and DEN outputs. With MB low, CEN low forces the command and DEN outputs inactive but does not tristate them.
DEN	16	O	DATA ENABLE controls when data transceivers connected to the local data bus should be enabled. DEN is an active high control output. DEN is delayed for write cycles in the Multibus mode.
DT/$\overline{\text{R}}$	17	O	DATA TRANSMIT/$\overline{\text{RECEIVE}}$ establishes the direction of data flow to or from the local data bus. When high, this control output indicates that a write bus cycle is being performed. A low indicates a read bus cycle. DEN is always inactive when DT/$\overline{\text{R}}$ changes states. This output is high when no bus cycle is active. DT/$\overline{\text{R}}$ is not affected by any of the control inputs.
M/$\overline{\text{IO}}$	18	I	MEMORY or $\overline{\text{I/O}}$ SELECT determines whether the current bus cycle is in the memory space or I/O space. When low, the current bus cycle is in the I/O space. This input has a pullup resistor sufficient to hold it high when nothing drives it. Setup and hold times must be met for proper operation.
V_{CC}	20	–	POWER SUPPLY (+5 V)
GND	10	–	GROUND (0 V)

Block Diagram



Functional Description

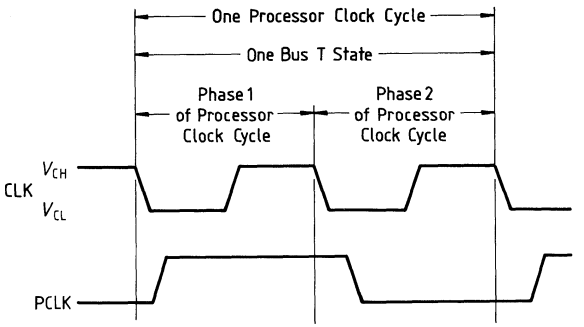
Introduction

The SAB 82288 bus controller is used in SAB 80286 systems to provide address latch control, data transceiver control, and standard level-type command outputs. The command outputs are timed and have sufficient drive capabilities for large TTL buses and meet all IEEE-796 requirements for Multibus. A special Multibus mode is provided to statisfy all address/data setup and hold time requirements. Command timing may be tailored to special needs via a CMDLY input to determine the start of a command and $\overline{\text{READY}}$ to determine the end of a command.
Connection to multiple buses is supported with a latched enable input (CENL). An address decoder can determine which, if any, bus controller should be enabled for the bus cycle. This input is latched to allow an address decoder to take full advantage of the pipelined timing on the SAB 80286 local bus.
Buses shared by several bus controllers are supported. An $\overline{\text{AEN}}$ input prevents the bus controller from driving the shared bus command and data signals except when enabled by an external bus arbiter such as the SAB 82289.
Separate DEN and DT/$\overline{\text{R}}$ outputs control the data transceivers for all buses. Bus contention is eliminated by disabling DEN before changing DT/$\overline{\text{R}}$. The DEN timing allows sufficient time for tristate bus drivers to enter tristate off before enabling other drivers onto the same bus.
The term CPU refers to any SAB 80286 processor or SAB 80286 support component which may become an SAB 80286 local bus master and thereby drive the SAB 82288 status inputs.

Processor Cycle Definition

Any CPU which drives the local bus uses an internal clock which is one half the frequency of the system clock (CLK) (see figure below). Knowledge of the phase of the local bus master's internal clock is required for proper operation of the SAB 80286 local bus. The local bus master informs the bus controller of its internal clock phase when it asserts the status signals. Status signals are always asserted in phase 1 of the local bus master's internal clock.

CLK Relationship to the Processor Clock and Bus T-States

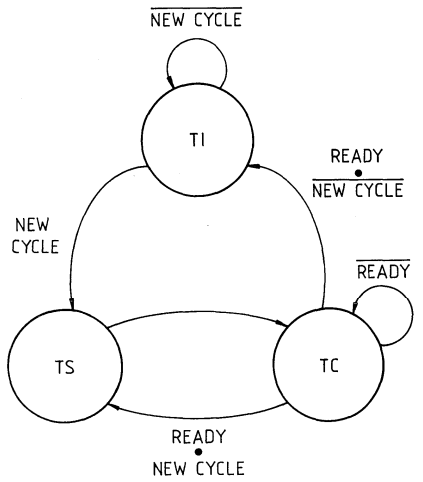


Bus State Definition

The SAB 82288 bus controller has three bus states (see figure below): Idle (TI), Status (TS), and Command (TC). Each bus state is two CLK cycles long. Bus state phases correspond to the internal CPU processor clock phases.

The TI bus state occurs when no bus cycle is currently active on the SAB 80286 local bus. This state may be repeated indefinitely. When control of the local bus is being passed between masters, the bus remains in the TI state.

Bus States



Bus Cycle Definition

The $\overline{S1}$ and $\overline{S0}$ inputs signal the start of a bus cycle. When either input becomes low, a bus cycle is started. The TS bus state is defined to be the two CLK cycles during which either $\overline{S1}$ or $\overline{S0}$ is active (see figure on bus cycle definition). These inputs are sampled by the SAB 82288 at every falling edge of CLK. When either $\overline{S1}$ or $\overline{S0}$ is sampled low, the next CLK cycle is considered the second phase of the internal CPU clock cycle.
The local bus enters the TC bus state after the TS state. The shortest bus cycle may have one TS state and one TC state. Longer bus cycles are formed by repeating TC states. A repeated TC bus state is called a wait state.

The $\overline{READY}$ input determines whether the current TC bus state is to be repeated. The $\overline{READY}$ input has the same timing and effect for all bus cycles. $\overline{READY}$ is sampled at the end of each TC bus state to see if it is active. If sampled high, the TC bus state is repeated. This is called inserting a wait state. The control and command outputs do not change during wait states.
When $\overline{READY}$ is sampled low, the current bus cycle is terminated. Note that the bus controller may enter the TS bus state directly from TC if the status lines are sampled active at the next falling edge of CLK.

Bus Cycle Definition

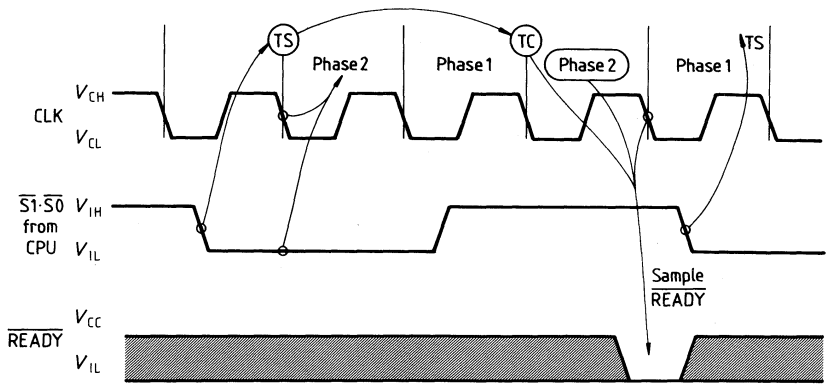


Table 2 Command and Control Output for Each Type of Bus Cycle

Type of bus cycle	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Command activated	DT/$\overline{R}$ state	ALE, DEN issued?	MCE issued?
Interrupt acknowledge	0	0	0	$\overline{INTA}$	low	yes	yes
I/O read	0	0	1	$\overline{IORC}$	low	yes	no
I/O write	0	1	0	$\overline{IOWC}$	high	yes	no
None; idle	0	1	1	none	high	no	no
Halt/shutdown	1	0	0	none	high	no	no
Memory read	1	0	1	$\overline{MRDC}$	low	yes	no
Memory write	1	1	0	$\overline{MWTC}$	high	yes	no
None; idle	1	1	1	none	high	no	no

Operating Modes

Two types of buses are supported by the SAB 82288: Multibus and non-Multibus. When the MB input is high, Multibus timing is used. In Multibus mode, the SAB 82288 delays command and data activation to meet IEEE-796 requirements on address to command active and write data to command active setup timing. Multibus mode requires at least one wait state in the bus cycle since the command outputs are delayed. The non-Multibus mode does not delay any outputs and does not require wait states. The MB input affects the timing of the command and DEN outputs.

Command and Control Outputs

The type of bus cycle performed by the local bus master is encoded in the M/$\overline{IO}$, $\overline{S1}$, and $\overline{S0}$ inputs. Different command and control outputs are activated depending on the type of bus cycle. Table 2 indicates the cycle decoding done by the SAB 82288 and the effect on command, DT/$\overline{R}$, ALE, DEN, and MCE outputs.

Bus cycles come in three forms: read, write, and halt. Read bus cycles include memory read, I/O read, and interrupt acknowledge. The timing of the associated read command outputs ($\overline{MRDC}$, $\overline{IORC}$, and $\overline{INTA}$), control outputs (ALE, DEN, DT/$\overline{R}$) and control inputs (CEN/$\overline{AEN}$, CENL, CMDLY, MB, and $\overline{READY}$) are identical for all read bus cycles. Read cycles differ only in which command output is activated. The MCE control output is only asserted during interrupt acknowledge cycles.

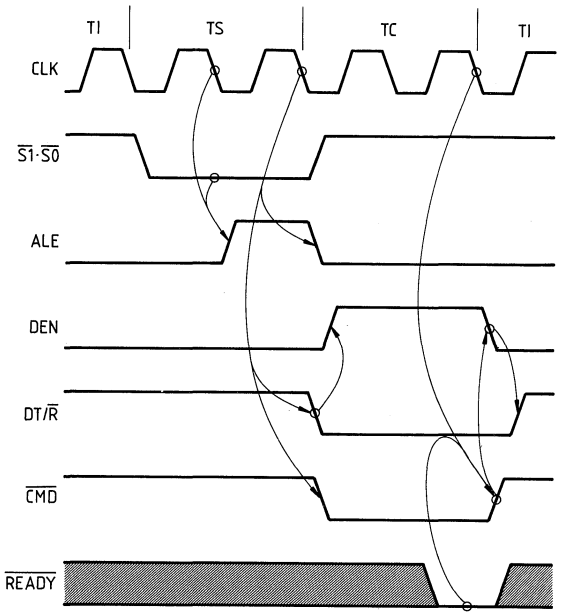
Write bus cycles activate different control and command outputs with different timing than read bus cycles. Memory write and I/O write are write bus cycles whose timing for command outputs ($\overline{MWTC}$ and $\overline{IOWC}$), control outputs (ALE, DEN, DT/$\overline{R}$) and control inputs (CEN/$\overline{AEN}$, CENL, CMDLY, MB, and $\overline{READY}$) are identical. They differ only in which command output is activated.

Halt bus cycles are different because no command or control output is activated. All control inputs are ignored until the next bus cycle is started via $\overline{S1}$ and $\overline{S0}$.

The basic command and control output timing for read and write bus cycles is shown in the next five figures. Halt bus cycles are not shown since they activate no outputs. The basic idle-read-idle and idle-write-idle bus cycles are shown. The signal label $\overline{CMD}$ represents the appropriate command output for the bus cycle. For those five figures, the CMDLY input is connected to GND and CENL to V_{CC}. The effects of CENL and CMDLY are described later in the section on control inputs.

The next two figures show non-Multibus cycles. MB is connected to GND while CEN is connected to V_{CC}. The figure on page 10 shows a read cycle with no wait states while the figure on page 11 shows a write cycle with one wait state. The $\overline{READY}$ input is shown to illustrate how wait states are added.

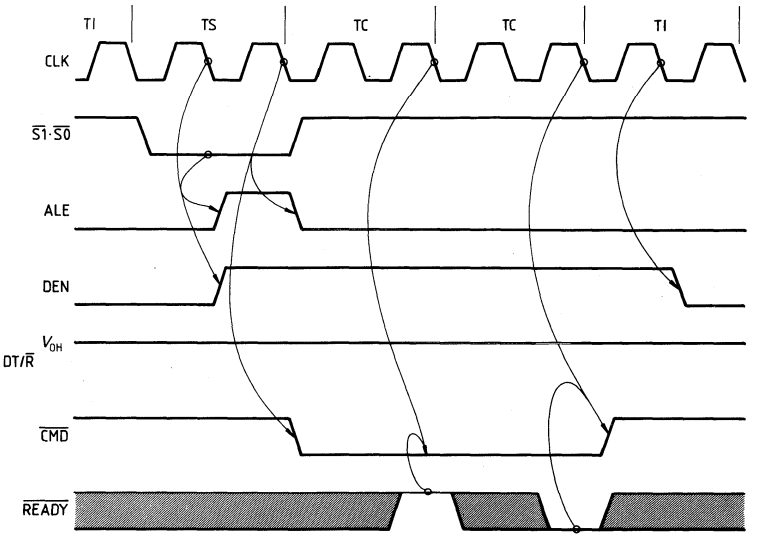
Idle-Read-Idle Bus Cycles with MB = 0



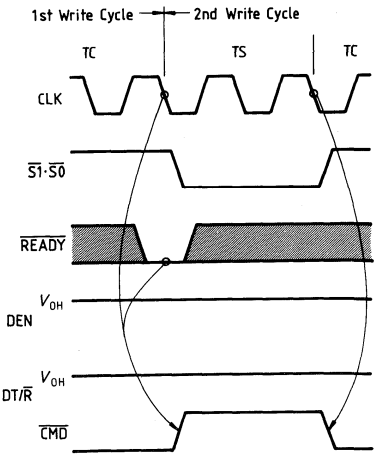
Bus cycles can occur back-to-back with no TI bus states between TC and TS. Back-to-back cycles do not affect the timing of the command and control outputs. Command and control outputs always reach the states shown for the same clock edge (within TS, TC, or following bus state) of a bus cycle. A special case in control timing occurs for back-to-back write cycles with MB = 0. In this case, DT/$\overline{R}$ and DEN remain high between the bus cycles (see respective write-write cycle diagram). The command and ALE output timing does not change.

The figures on pages 12 and 13 show a Multibus cycle with MB = 1. $\overline{AEN}$ and CMDLY are connected to GND. The effects of CMDLY and $\overline{AEN}$ are described later in the section on control inputs. The top figure shows a read cycle with one wait state and the figure below shows a write cycle with two wait states. The second wait state of the write cycle is shown only for example purposes and is not required. The $\overline{READY}$ input is shown to illustrate how wait states are added.

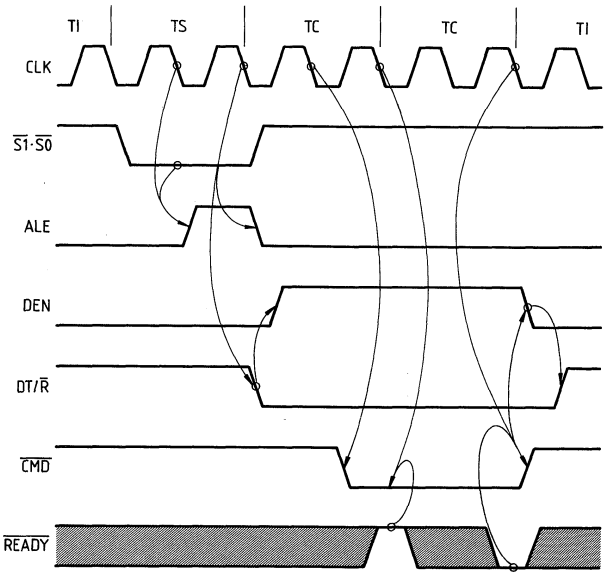
Idle-Write-Idle Bus Cycles with MB = 0



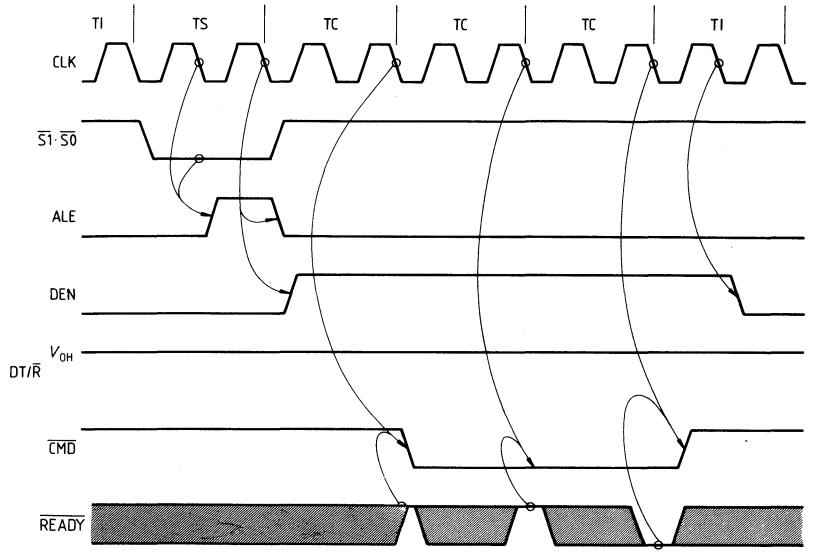
Write-Write Bus Cycles with MB = 0



Idle-Read-Idle Bus Cycles with MB = 1



Idle-Write-Idle Bus Cycles with MB = 1



The MB control input affects the timing of the command and DEN outputs. These outputs are automatically delayed in Multibus mode to satisfy three requirements:

1) 50 ns minimum setup time for valid address before any command output becomes active.
2) 50 ns minimum setup time for valid write data before any write command output becomes active.
3) 65 ns maximum time from when any read command becomes inactive until the slave's read data drivers reach tristate off.

Three signal transitions are delayed by MB = 1 as compared to MB = 0:

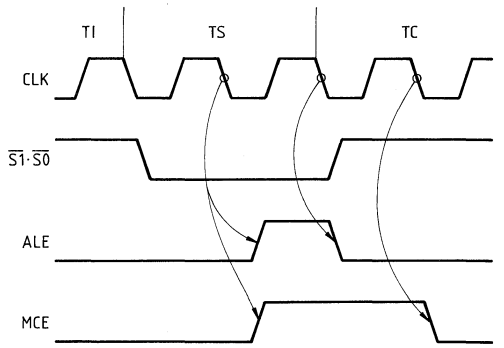
1) The high to low transition of the read command outputs ($\overline{IORC}$, $\overline{MRDC}$, and $\overline{INTA}$) is delayed one CLK cycle.
2) The high to low transition of the write command outputs ($\overline{IOWC}$ and $\overline{MWTC}$) is delayed two CLK cycles.
3) The low to high transition of DEN for write cycles is delayed one CLK cycle.

Back-to-back bus cycles with MB = 1 do not change the timing of any of the command or control outputs. DEN always becomes inactive between bus cycles with MB = 1.

Except for a halt or shutdown bus cycle, ALE will be issued during the second half of TS for any bus cycle. ALE becomes inactive at the end of the TS to allow latching the address to keep it stable during the entire bus cycle. The address outputs may change during phase 2 of any TC bus state. ALE is not affected by any control input.

The following figure shows how MCE is timed during interrupt acknowledge (INTA) bus cycles. MCE is one CLK cycle longer than ALE to hold the cascade address from a master SAB 8259A valid after the falling edge of ALE. With the exception of the MCE control output, an INTA bus cycle is identical in timing with a read bus cycle. MCE is not affected by any control input.

MCE Operation for an INTA Bus Cycle



Control Inputs

The control inputs can alter the basic timing of command outputs, allow interfacing to multiple buses, and share a bus between different masters. For many SAB 80286 systems, each CPU will have more than one bus which may be used to perform a bus cycle. Normally, a CPU will only have one bus controller active for each bus cycle. Some buses may be shared by more than one CPU (i.e. Multibus) requiring only one of them use the bus at a time.

Systems with multiple and shared buses use two control input signals of the SAB 82288 bus controller, CENL and $\overline{AEN}$ (see figure on system use of those signals). CENL enables the bus controller to control the current bus cycle. The $\overline{AEN}$ input prevents a bus controller from driving its command outputs. $\overline{AEN}$ high means that another bus controller may be driving the shared bus.

In the figure on the $\overline{AEN}$ and CENL signal, two buses are shown: a local bus and a Multibus. Only one bus is used for each CPU bus cycle. The CENL inputs of the bus controllers select which bus controller is to perform the bus cycle. An address decoder determines which bus to use for each bus cycle. The SAB 82288 connected to the shared Multibus must be selected by CENL and be given access to the Multibus by $\overline{AEN}$ before it will begin a Multibus operation.

CENL must be sampled high at the end of the TS bus state (see waveforms) to enable the bus controller to activate its command and control outputs. If sampled low the commands and DEN will not go active and DT/$\overline{R}$ will remain high. The bus controller will ignore the CMDLY, CEN, and $\overline{READY}$ inputs until another bus cycle is started via $\overline{S1}$ and $\overline{S0}$. Since an address decoder is commonly used to identify which bus is required for each bus cycle, CENL is latched to avoid the need for latching its input.

The CENL input can effect the DEN control output. When MB = 0, DEN normally becomes active during phase 2 of TS in write bus cycles. This transition occurs before CENL is sampled. If CENL is sampled low, the DEN output will be forced low during TC as shown in the timing waveforms.

When MB = 1, CEN/$\overline{AEN}$ becomes $\overline{AEN}$, $\overline{AEN}$ controls when the bus controller command outputs enter and exit tristate off. $\overline{AEN}$ is intended to be driven by a bus arbiter, like the SAB 82289, which assures only one bus controller is driving the shared bus at any time. When $\overline{AEN}$ makes a low to high transition, the command outputs immediately enter tristate off and DEN is forced inactive. An inactive DEN should force the local data transceivers connected to the shared data bus into tristate off (see next figure). The low to high transition of $\overline{AEN}$ should only occur during TI or TS bus states.

The high-to-low transition of $\overline{AEN}$ signals that the bus controller may now drive the shared bus command signals. Since a bus cycle may be active or be in the process of starting, $\overline{AEN}$ can become active during any T-state. $\overline{AEN}$ low immediately allows DEN to go to the appropriate state. Three CLK

edges later, the command outputs will go active (see timing waveforms). The Multibus requires this delay for the address and data to be valid on the bus before the commands become active.

When MB = 0, CEN/$\overline{\text{AEN}}$ becomes CEN. CEN is an asynchronous input which immediately affects the command and DEN outputs. When CEN makes a high-to-low transition, the commands and DEN are immediately forced inactive. When CEN makes a low-to-high transition, the commands and DEN outputs immediately go to the appropriate state (see timing waveforms). $\overline{\text{READY}}$ must still become active to terminate a bus cycle if CEN remains low for a selected bus controller (CENL was latched high).

Some memory or I/O systems may require more address or write data setup time to command active than provided by the basic command output timing. To provide flexible command timing, the CMDLY input can delay the activation of command outputs. The CMDLY input must be sampled low to activate the command outputs. CMDLY does not affect the control outputs ALE, MCE, DEN, and DT/$\overline{\text{R}}$.

CMDLY is first sampled on the falling edge of the CLK ending TS. If sampled high, the command output is not activated, and CMDLY is again sampled on the next falling edge of CLK. Once sampled low, the proper command output becomes active immediately if MB = 0. If MB = 1, the proper command goes active no earlier than shown in the figures on pages 12 and 13.

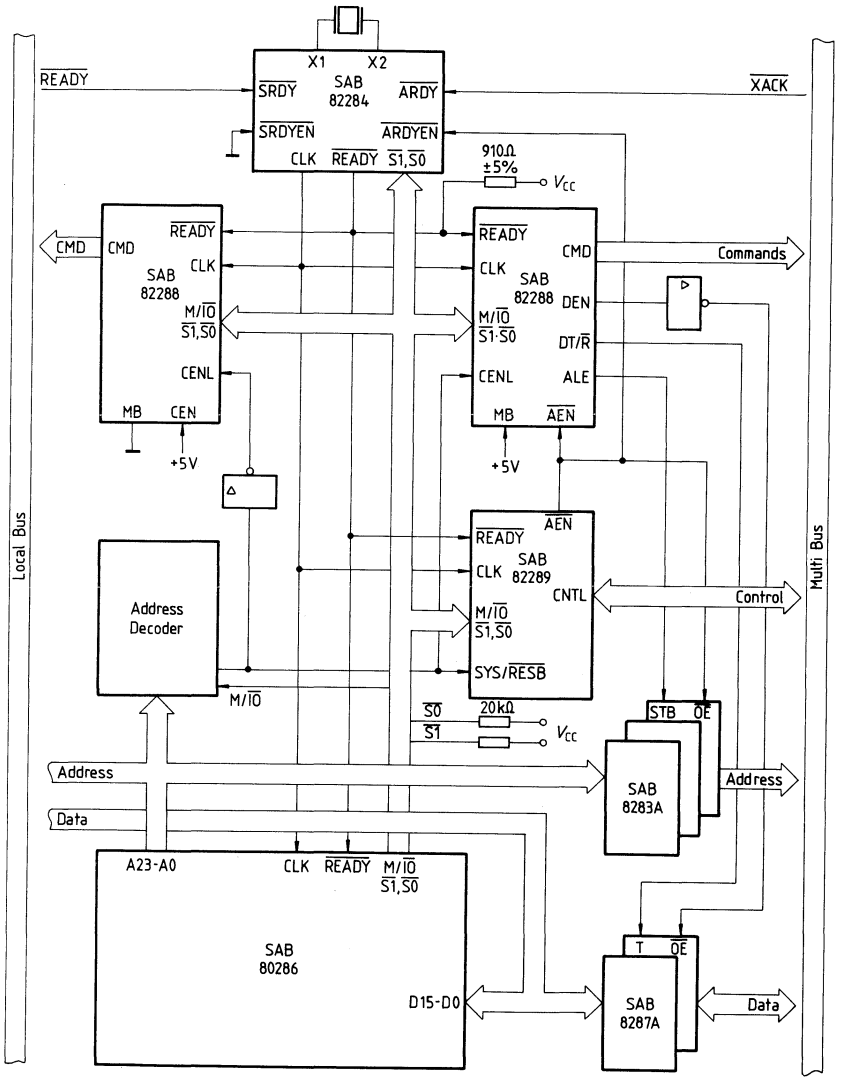
$\overline{\text{READY}}$ can terminate a bus cycle before CMDLY allows a command to be issued. In this case no commands are issued and the bus controller will deactivate DEN and DT/$\overline{\text{R}}$ in the same manner as if a command had been issued.

Waveforms

The waveforms show the timing relationships of inputs and outputs and do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown via the general cases. Special cases are shown when needed. The waveforms provide some functional descriptions of the SAB 82288; however, most functional descriptions are provided in the figures of section Functional Description.

To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

System Use of $\overline{AEN}$ and CENL



Absolute Maximum Ratings [1]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to + 150°C
Voltage on any pin with respect to GND	−0.5 to +7V
Power dissipation	1 W

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ± 10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
I_{CC}	Power supply current	–	100	mA	–
I_F	Forward input current ($\overline{S0}$, $\overline{S1}$, M/$\overline{IO}$)	–	−0.5	mA	V_F = 0.45 V
I_{LI}	Input leakage current (all other)	–	± 10	µA	0 V ≦ V_{IN} ≦ V_{CC}
I_{LO}	Output leakage current	–	± 10	µA	0.45 V ≦ V_{OUT} ≦ V_{CC}
V_{OL}	Low output voltage Command outputs Control outputs	–	0.45	V	 I_{OL} = 32 mA I_{OL} = 16 mA
V_{OH}	High output voltage Command outputs Control outputs	2.4	–	V	 I_{OH} = −5 mA I_{OH} = −1 mA
V_{IL}	Low input voltage	−0.5	0.8	V	–
V_{CL}	CLK low input voltage	−0.5	0.6	V	–
V_{IH}	High input voltage	2.0	V_{CC} +0.5	V	–
V_{CH}	CLK high input voltage	3.8		V	–

Capacitance

T_A = 25°C, V_{CC} = GND = 0 V, f_C = 1 MHz

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_{CLK}	CLK input capacitance	–	12	pf	Unmeasured pins returned to GND
C_I	Input capacitance	–	10	pf	
C_{IO}	Input/output capacitance	–	20	pF	

Note: These parameters are periodically sampled, not 100% tested.

[1] Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics SAB 82288

T_A = 0 to 70°C, V_{CC} = 5 V ± 10%

Unless otherwise specified, the AC timings are referred to signal points of 0.8 V and 2.0 V as illustrated in the waveforms.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_1	CLK period	62	250	ns	–
t_2	CLK high time	20	235	ns	at 3.6 V
t_3	CLK low time	15	230	ns	at 1.0 V
t_4	CLK rise time	–	10	ns	1.0 to 3.6 V
t_5	CLK fall time	–	10	ns	3.6 to 1.0 V
t_6	M/$\overline{IO}$ and status setup time	22	–	ns	–
t_7	M/$\overline{IO}$ and status hold time	0	–	ns	–
t_8	CENL setup time	20	–	ns	–
t_9	CENL hold time	0	–	ns	–
t_{10}	$\overline{READY}$ setup time	38	–	ns	–
t_{11}	$\overline{READY}$ hold time	25	–	ns	–
t_{12}	CMDLY setup time	20	–	ns	–
t_{13}	CMDLY hold time	0	–	ns	–
t_{14}	$\overline{AEN}$ setup time	20	–	ns	1)
t_{15}	$\overline{AEN}$ hold time	0	–	ns	1)
t_{16}	ALE, MCE active delay	3	20	ns	2)
t_{17}	ALE, MCE inactive delay	–	20	ns	2)
t_{18}	DEN (write) inactive from CENL	–	35	ns	2)
t_{19}	DT/$\overline{R}$ low from CLK	–	25	ns	2)
t_{20}	DEN (read) active from DT/$\overline{R}$	5	35	ns	2)
t_{21}	DEN (read) inactive delay	3	35	ns	2)
t_{22}	DT/$\overline{R}$ high from DEN inactive	5	35	ns	2)
t_{23}	DEN (write) active delay	–	30	ns	2)
t_{24}	DEN (write) inactive delay	3	30	ns	2)
t_{25}	DEN inactive from CEN	–	25	ns	2)
t_{26}	DEN active from CEN	–	30	ns	2)
t_{27}	DT/$\overline{R}$ high from CLK and CEN	–	35	ns	2) 3)
t_{28}	DEN active from $\overline{AEN}$	–	30	ns	2)

Notes see next page

AC Characteristics SAB 82288 (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{29}	Command active delay	3	25	ns	[4]
t_{30}	Command inactive delay	3	25	ns	[4]
t_{31}	Command inactive from CEN	–	25	ns	[4]
t_{32}	Command active from CEN	–	25	ns	[4]
t_{33}	Command valid delay from $\overline{AEN}$	–	40	ns	[4]
t_{34}	Command float time	–	40	ns	[4]
t_{35}	MB setup time	20	–	ns	–
t_{36}	MB hold time	0	–	ns	–
t_{37}	Command inactive enable from MB↓	–	40	ns	[4]
t_{38}	Command float time from MB↑	–	40	ns	–
t_{39}	DEN inactive from MB↑	–	30	ns	[2]
t_{40}	DEN active from MB↓	–	35	ns	[2]

[1] $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold times are specified to guarantee the response shown in the waveforms.

[2] Control output load: C_L = 150 pF, I_{OL} = 16 mA, I_{OH} = −1 mA.

[3] t_{27} only applies to bus cycles where MB = 0, the SAB 82288 was selected, and DEN = 0 when the cycle is terminated (because CEN = 0).

[4] Command output load: C_L = 300 pF, I_{OL} = 32 mA, I_{OH} = −5 mA.

AC Characteristics SAB 82288-6

T_A = 0 to 70°C, V_{CC} = 5V ± 10%

Unless otherwise specified, the AC timings are referred to signal points of 0.8 V and 2.0 V as illustrated in the waveforms.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_1	CLK period	83	250	ns	–
t_2	CLK high time	25	235	ns	at 3.6 V
t_3	CLK low time	20	225	ns	at 1.0 V
t_4	CLK rise time	–	10	ns	1.0 to 3.6 V
t_5	CLK fall time	–	10	ns	3.6 to 1.0 V
t_6	M/$\overline{IO}$ and status setup time	28	–	ns	–
t_7	M/$\overline{IO}$ and status hold time	0	–	ns	–
t_8	CENL setup time	30	–	ns	–
t_9	CENL hold time	0	–	ns	–
t_{10}	$\overline{READY}$ setup time	50	–	ns	–
t_{11}	$\overline{READY}$ hold time	35	–	ns	–
t_{12}	CMDLY setup time	25	–	ns	–
t_{13}	CMDLY hold time	0	–	ns	–
t_{14}	$\overline{AEN}$ setup time	25	–	ns	1)
t_{15}	$\overline{AEN}$ hold time	0	–	ns	1)
t_{16}	ALE, MCE active delay	3	25	ns	2)
t_{17}	ALE, MCE inactive delay	–	35	ns	2)
t_{18}	DEN (write) inactive from CENL	–	35	ns	2)
t_{19}	DT/$\overline{R}$ low from CLK	–	40	ns	2)
t_{20}	DEN (read) active from DT/$\overline{R}$	5	50	ns	2)
t_{21}	DEN (read) inactive delay	3	40	ns	2)
t_{22}	DT/$\overline{R}$ high from DEN inactive	5	45	ns	2)
t_{23}	DEN (write) active delay	–	35	ns	2)
t_{24}	DEN (write) inactive delay	3	35	ns	2)
t_{25}	DEN inactive from CEN	–	40	ns	2)
t_{26}	DEN active from CEN	–	35	ns	2)
t_{27}	DT/$\overline{R}$ high from CLK and CEN	–	50	ns	2) 3)
t_{28}	DEN active from $\overline{AEN}$	–	35	ns	2)

Notes see next page

AC Characteristics SAB 82288-6 (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{29}	Command active delay	3	40	ns	[4]
t_{30}	Command inactive delay	3	30	ns	[4]
t_{31}	Command inactive from CEN	–	35	ns	[4]
t_{32}	Command active from CEN	–	45	ns	[4]
t_{33}	Command valid delay from $\overline{AEN}$	–	40	ns	[4]
t_{34}	Command float time	–	40	ns	[4]
t_{35}	MB setup time	25	–	ns	–
t_{36}	MB hold time	0	–	ns	–
t_{37}	Command inactive enable from MB↓	–	40	ns	[4]
t_{38}	Command float time from MB↑	–	40	ns	–
t_{39}	DEN inactive from MB↑	–	40	ns	[2]
t_{40}	DEN active from MB↓	–	35	ns	[2]

[1] $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold times are specified to guarantee the response shown in the waveforms.

[2] Control output load: C_L = 150 pF, I_{OL} = 16 mA, I_{OH} = −1 mA.

[3] t_{27} only applies to bus cycles where MB = 0, the SAB 82288 was selected, and DEN = 0 when the cycle is terminated (because CEN = 0).

[4] Command output load: C_L = 300 pF, I_{OL} = 32 mA, I_{OH} = −5 mA.

AC Characteristics SAB 82288-1

T_A = 0 to 70°C, V_{CC} = 5 V ± 10%

Unless otherwise specified, the AC timings are referred to signal points of 0.8 V and 2.0 V as illustrated in the waveforms.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_1	CLK period	50	250	ns	–
t_2	CLK high time	16	235	ns	at 3.6 V
t_3	CLK low time	12	230	ns	at 1.0 V
t_4	CLK rise time	–	8	ns	1.0 to 3.6 V
t_5	CLK fall time	–	8	ns	3.6 to 1.0 V
t_6	M/$\overline{IO}$ and status setup time	18	–	ns	–
t_7	M/$\overline{IO}$ and status hold time	0	–	ns	–
t_8	CENL setup time	15	–	ns	–
t_9	CENL hold time	0	–	ns	–
t_{10}	$\overline{READY}$ setup time	26	–	ns	–
t_{11}	$\overline{READY}$ hold time	25	–	ns	–
t_{12}	CMDLY setup time	15	–	ns	–
t_{13}	CMDLY hold time	0	–	ns	–
t_{14}	$\overline{AEN}$ setup time	15	–	ns	1)
t_{15}	$\overline{AEN}$ hold time	0	–	ns	1)
t_{16}	ALE, MCE active delay	3	16	ns	2)
t_{17}	ALE, MCE inactive delay	–	19	ns	2)
t_{18}	DEN (write) inactive from CENL	–	23	ns	2)
t_{19}	DT/$\overline{R}$ low from CLK	–	23	ns	2)
t_{20}	DEN (read) active from DT/$\overline{R}$	5	21	ns	2)
t_{21}	DEN (read) inactive delay	3	21	ns	2)
t_{22}	DT/$\overline{R}$ high from DEN inactive	5	20	ns	2)
t_{23}	DEN (write) active delay	–	23	ns	2)
t_{24}	DEN (write) inactive delay	3	19	ns	2)
t_{25}	DEN inactive from CEN	–	25	ns	2)
t_{26}	DEN active from CEN	–	24	ns	2)
t_{27}	DT/$\overline{R}$ high from CLK and CEN	–	25	ns	2) 3)
t_{28}	DEN active from $\overline{AEN}$	–	26	ns	2)

Notes see next page

AC Characteristics SAB 82288-1 (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{29}	Command active delay	3	21	ns	[4]
t_{30}	Command inactive delay	3	20	ns	[4]
t_{31}	Command inactive from CEN	–	25	ns	[4]
t_{32}	Command active from CEN	–	25	ns	[4]
t_{33}	Command inactive enable from $\overline{AEN}$	–	40	ns	[4]
t_{34}	Command float time	–	40	ns	[4]
t_{35}	MB setup time	20	–	ns	–
t_{36}	MB hold time	0	–	ns	–
t_{37}	Command inactive enable from MB↓	–	40	ns	[4]
t_{38}	Command float time from MB↑	–	40	ns	–
t_{39}	DEN inactive from MB↑	–	26	ns	[2]
t_{40}	DEN active from MB↓	–	35	ns	[2]

[1] $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold times are specified to guarantee the response shown in the waveforms.

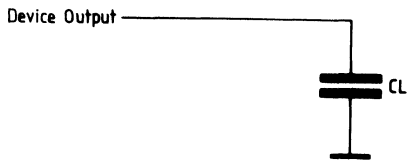
[2] Control output load: C_L = 150 pF, I_{OL} = 16 mA, I_{OH} = −1 mA.

[3] t_{27} only applies to bus cycles where MB = 0, the SAB 82288 was selected, and DEN = 0 when the cycle is terminated (because CEN = 0).

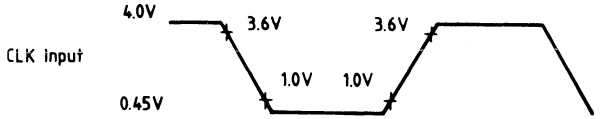
[4] Command output load: C_L = 300 pF, I_{OL} = 32 mA, I_{OH} = −5 mA.

AC Testing Waveforms

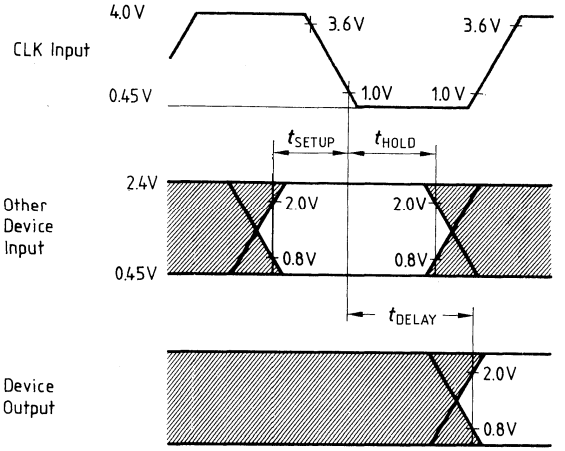
Test Loading on Outputs



Drive and Measurement Points – CLK Input

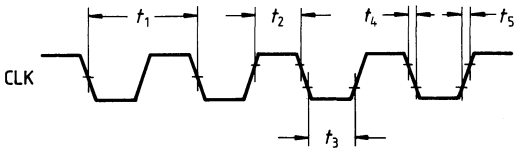


Setup, Hold and Delay Time Measurement – General

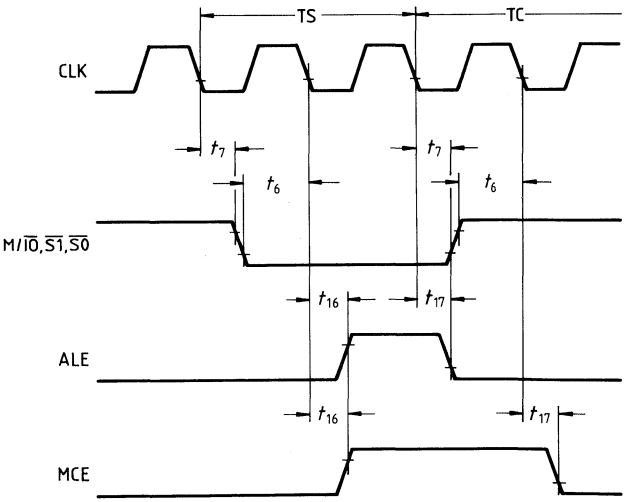


Waveforms

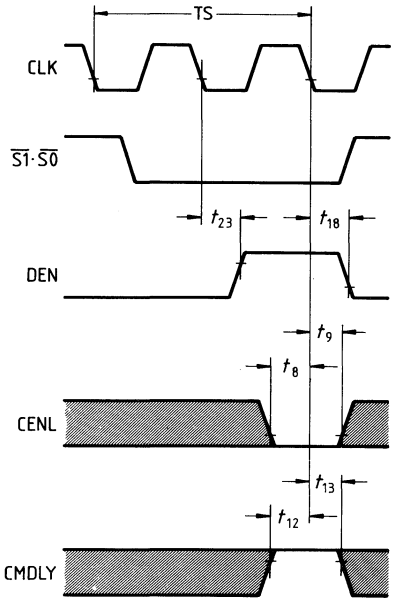
CLK Characteristics



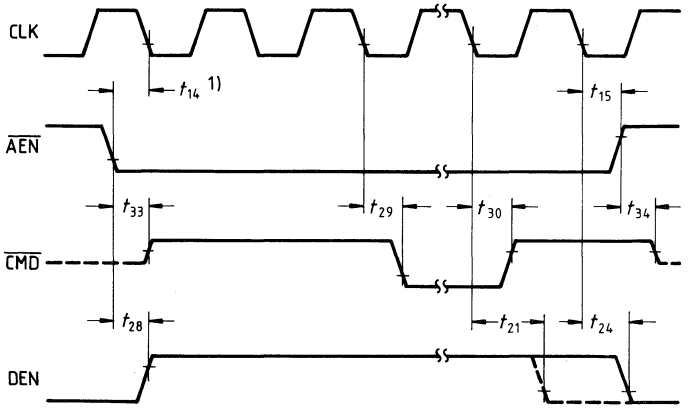
Status, ALE, MCE Characteristics



CENL, CMDLY, DEN Characteristics with MB = 0 and CEN = 1 during Write Cycle

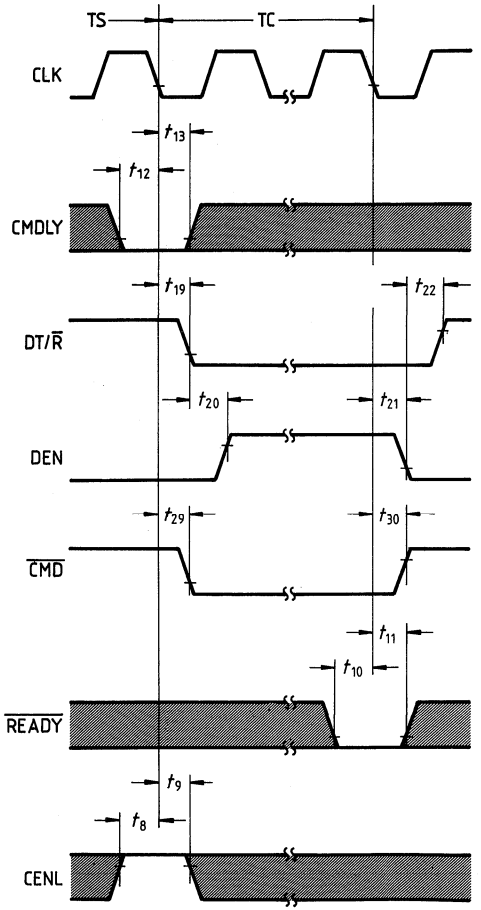


AEN Characteristics with MB = 1

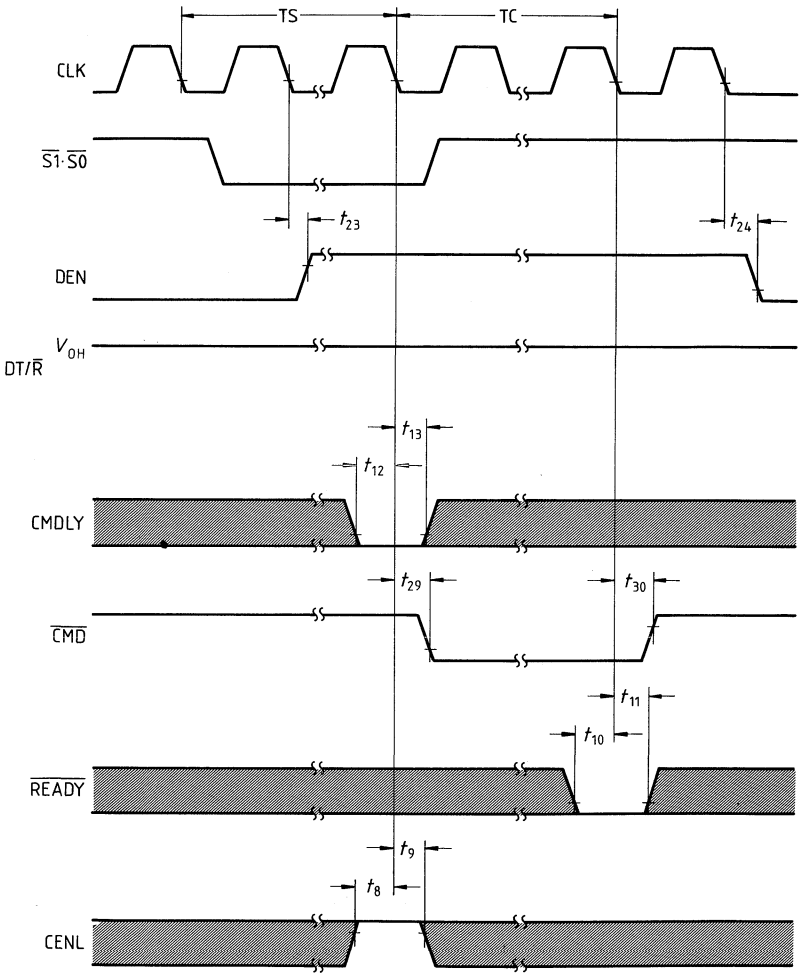


1) AEN is an asynchronous input. AEN setup and hold time is specified to guarantee the response shown in the waveforms.

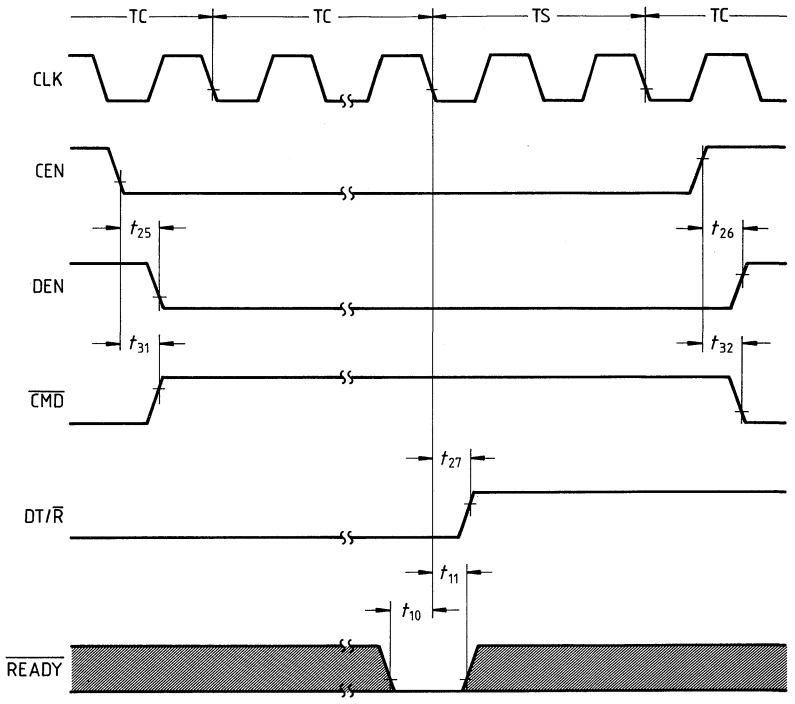
Read Cycle Characteristics with MB = 0 and CEN = 1



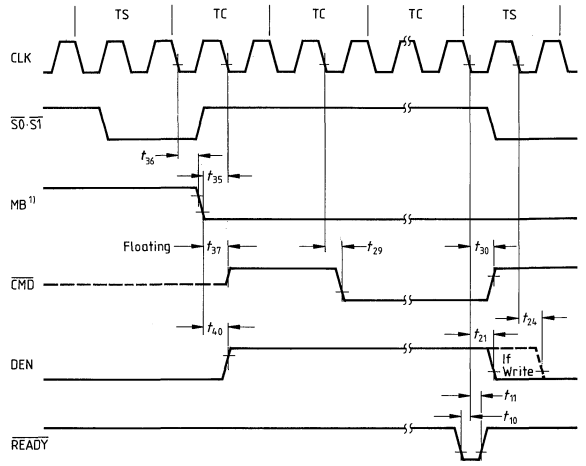
Write Cycle Characteristics with MB = 0 and CEN = 1

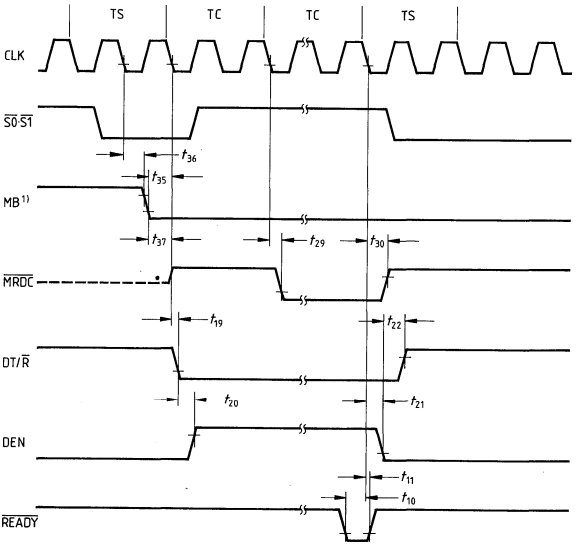


CEN Characteristics with MB = 0



MB Characteristics with $\overline{AEN}$/CEN = High

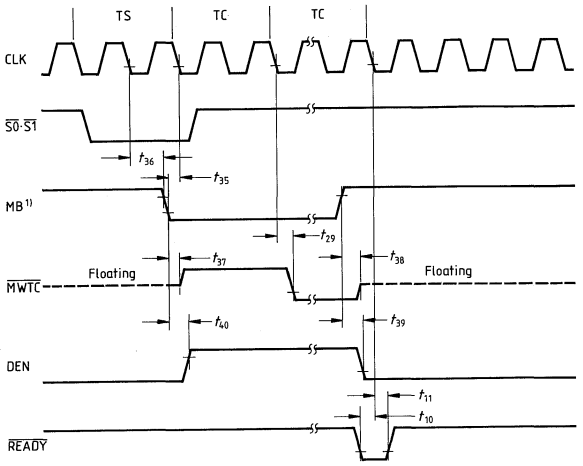




1) MB is an asynchronous input. MB setup and hold times specified to guarantee the response shown in the waveforms.

If the setup time t_{35} is met, two clock cycles will occur before $\overline{CMD}$ becomes active after the falling edge of MB.

MB Characteristics with $\overline{AEN}$/CEN = High (cont'd)

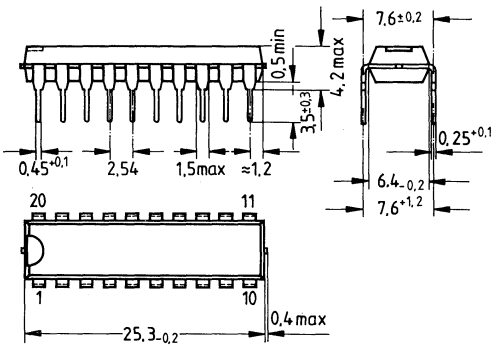


1) MB is an asynchronous input. MB setup and hold times specified to guarantee the response shown in the waveforms.

If the setup time t_{35} is met, two clock cycles will occur before $\overline{CMD}$ becomes active after the falling edge of MB.

Package Outlines

Plastic Package, P-DIP, 20 Pins



Dimensions in mm

Ordering Information

Type	Ordering code	Function
SAB 82288-P	Q67 120-Y75	Bus controller (plastic package) up to 16 MHz
SAB 82288-6-P	Q67 120-Y 110	Bus controller (plastic package) up to 12 MHz
SAB 82288-1-P	Q67 120-Y69	Bus controller (plastic package) up to 20 MHz

Advance Information

SAB 82C288 Bus Controller for SAB 80286 Processors

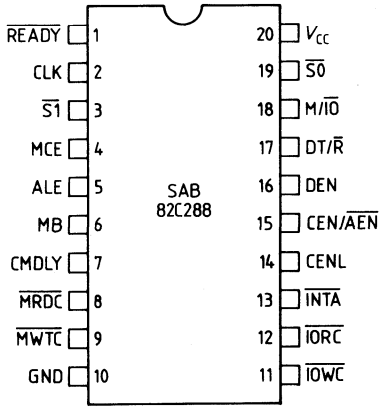
SAB 82C288 up to 16 MHz
SAB 82C288-12 up to 25 MHz

- Provides commands and control for local and system bus
- Offers wide flexibility in system configurations
- Flexible command timing

SAB 82C288-1 up to 20 MHz

- Optimal Multibus®-compatible timing
- Control drivers with 16 mA I_{OL} and tristate command drivers with 32 mA I_{OL}
- Single +5 V supply

Pin Configuration



Pin Names

CLK	System Clock
$\overline{S0}$, $\overline{S1}$	Bus Cycle Status
M/$\overline{IO}$	Memory or I/O Select
MB	Multibus Mode Select
CENL	Command Enable Latched
CMDLY	Command Delay
$\overline{READY}$	Bus Cycle Termination
CEN/$\overline{AEN}$	Command Enable/Address Enable
ALE	Address Latch Enable
MCE	Master Cascade Enable
DEN	Data Enable
DT/$\overline{R}$	Data Transmit/Receive
$\overline{IOWC}$	I/O Write Command
$\overline{IORC}$	I/O Read Command
$\overline{MWTC}$	Memory Write Command
$\overline{MRDC}$	Memory Read Command
$\overline{INTA}$	Interrupt Acknowledge
V_{CC}	Power Supply (+5 V)
GND	Ground (0 V)

The SAB 82C288 bus controller is a 20-pin CMOS component for use in SAB 80286 microsystems. The bus controller provides command and control outputs with flexible timing options. Separate command outputs are used for memory and I/O devices. The data bus is controlled with separate data enable and direction control signals. Two modes of operation are possible: Multibus-compatible bus cycles, and high-speed bus cycles.

Multibus® is a registered trademark of Intel Corporation.

Pin Definitions and Functions

<table>
<tr><th>Symbol</th><th>Pin</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{\text{READY}}$</td><td>1</td><td>I</td><td>$\overline{\text{READY}}$ indicates the end of the current bus cycle. $\overline{\text{READY}}$ is an active low input. Multibus mode requires at least one wait state to allow the command outputs to become active. $\overline{\text{READY}}$ must be low during reset, to force the SAB 82C288 into the idle state. Setup and hold times must be met for proper operation.</td></tr>
<tr><td>CLK</td><td>2</td><td>I</td><td>SYSTEM CLOCK provides the basic timing control for the SAB 82C288 in an SAB 80286 microsystem. Its frequency is twice the internal processor clock frequency. The falling edge of this input signal establishes when inputs are sampled and control outputs change.</td></tr>
<tr><td>$\overline{\text{S0}}$, $\overline{\text{S1}}$</td><td>3, 19</td><td>I</td><td>BUS CYCLE STATUS starts a bus cycle and, along with M/$\overline{\text{IO}}$, defines the type of bus cycle. These inputs are active low. A bus cycle is started when either $\overline{\text{S1}}$ or $\overline{\text{S0}}$ is sampled low at the falling edge of CLK. These inputs have pullup resistors sufficient to hold them high when nothing drives them. Setup and hold times must be met for proper operation.
<table>
<tr><th colspan="4">SAB 80286 bus cycle status definition</th></tr>
<tr><th>M/$\overline{\text{IO}}$</th><th>$\overline{\text{S1}}$</th><th>$\overline{\text{S0}}$</th><th>Type of bus cycle</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>I/O read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I/O write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>None; idle</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Halt or shutdown</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Memory read</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Memory write</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>None; idle</td></tr>
</table></td></tr>
<tr><td>MCE</td><td>4</td><td>O</td><td>MASTER CASCADE ENABLE signals that a cascade address from a master SAB 8259A interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. This control output is active high. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.</td></tr>
<tr><td>ALE</td><td>5</td><td>O</td><td>ADDRESS LATCH ENABLE controls the address latches used to hold an address stable during a bus cycle. This control output is active high. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.</td></tr>
<tr><td>MB</td><td>6</td><td>I</td><td>MULTIBUS MODE SELECT determines timing of the command and control outputs. When high, the bus controller operates in Multibus mode. When low, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/$\overline{\text{AEN}}$ input pin is selected by this signal. Typically, this input is a strapping option and not dynamically changed. This input may be connected to V_{CC} or GND.</td></tr>
</table>

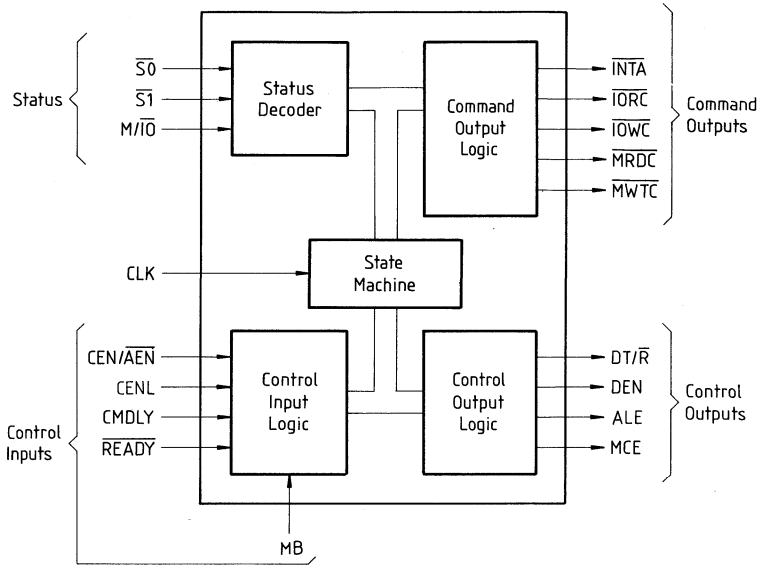
Pin Definitions and Function (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CMDLY	7	I	COMMAND DELAY allows delaying the start of a command. CMDLY is an active high input. If sampled high, the command output is not activated and CMDLY is again sampled at the next CLK cycle. When sampled low the selected command is enabled. If $\overline{\text{READY}}$ is detected low before the command output is activated, the SAB 82C288 will terminate the bus cycle, even if no command was issued. Setup and hold times must be satisfied for proper operation. This input may be connected to GND if no delays are required before starting a command.
$\overline{\text{MRDC}}$	8	O	$\overline{\text{MEMORY READ COMMAND}}$ instructs the memory device to place data onto the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{MWTC}}$	9	O	$\overline{\text{MEMORY WRITE COMMAND}}$ instructs a memory device to read the data on the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{IOWC}}$	11	O	$\overline{\text{I/O WRITE COMMAND}}$ instructs an I/O device to read the data on the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{IORC}}$	12	O	$\overline{\text{I/O READ COMMAND}}$ instructs an I/O device to place data onto the data bus. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{INTA}}$	13	O	$\overline{\text{INTERRUPT ACKNOWLEDGE}}$ tells an interrupting device that its interrupt request is being acknowledged. This command output is active low. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
CENL	14	I	COMMAND ENABLE LATCHED is a bus controller select signal which enables the bus controller to respond to the current bus cycle being initiated. CENL is an active high input latched internally at the start of each bus cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. This input may be connected to V_{CC} to select this SAB 82C288 for all transfers. No control inputs affect CENL. Setup and hold times must be met for proper operation.

Pin Definitions and Functions (cont'd)

Symbol	Pin	Input (I) Output (O)	Function
CEN/$\overline{\text{AEN}}$	15	I	COMMAND ENABLE/$\overline{\text{ADDRESS ENABLE}}$ controls the command and DEN outputs of the bus controller. CEN/$\overline{\text{AEN}}$ inputs may be asynchronous to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs. This input may be connected to V_{CC} or GND. When MB is high this pin has the $\overline{\text{AEN}}$ function. $\overline{\text{AEN}}$ is an active low input which indicates that the CPU has been granted use of a shared bus and the bus controller command outputs may exit tristate off and become inactive (high). $\overline{\text{AEN}}$ high indicates that the CPU does not have control of the shared bus and forces the command outputs into tristate off and DEN inactive (low). $\overline{\text{AEN}}$ would normally be controlled by an SAB 82289 bus arbiter which activates $\overline{\text{AEN}}$ when that arbiter owns the bus to which the bus controller is attached. When MB is low this pin has the CEN function. CEN is an unlatched active high input which allows the bus controller activate its command and DEN outputs. With MB low, CEN low forces the command and DEN outputs inactive but does not tristate them.
DEN	16	O	DATA ENABLE controls when data transceivers connected to the local data bus should be enabled. DEN is an active high control output. DEN is delayed for write cycles in the Multibus mode.
DT/$\overline{\text{R}}$	17	O	DATA TRANSMIT/$\overline{\text{RECEIVE}}$ establishes the direction of data flow to or from the local data bus. When high, this control output indicates that a write bus cycle is being performed. A low indicates a read bus cycle. DEN is always inactive when DT/$\overline{\text{R}}$ changes states. This output is high when no bus cycle is active. DT/$\overline{\text{R}}$ is not affected by any of the control inputs.
M/$\overline{\text{IO}}$	18	I	MEMORY or $\overline{\text{I/O}}$ SELECT determines whether the current bus cycle is in the memory space or I/O space. When low, the current bus cycle is in the I/O space. This input has a pullup resistor sufficient to hold it high when nothing drives it. Setup and hold times must be met for proper operation.
V_{CC}	20	–	POWER SUPPLY (+5 V)
GND	10	–	GROUND (0 V)

Block Diagram



Functional Description

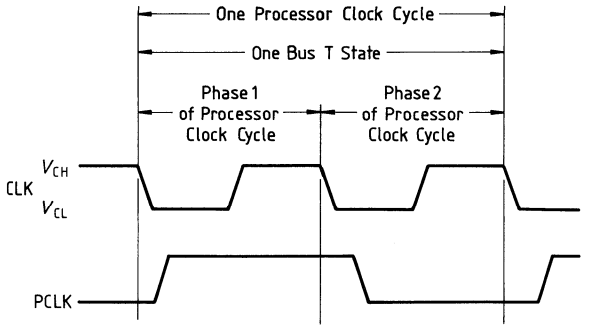
Introduction

The SAB 82C288 bus controller is used in SAB 80286 systems to provide address latch control, data transceiver control, and standard level-type command outputs. The command outputs are timed and have sufficient drive capabilities for large TTL buses and meet all IEEE-796 requirements for Multibus. A special Multibus mode is provided to satisfy all address/data setup and hold time requirements. Command timing may be tailored to special needs via a CMDLY input to determine the start of a command and $\overline{\text{READY}}$ to determine the end of a command.
Connection to multiple buses is supported with a latched enable input (CENL). An address decoder can determine which, if any, bus controller should be enabled for the bus cycle. This input is latched to allow an address decoder to take full advantage of the pipelined timing on the SAB 80286 local bus.
Buses shared by several bus controllers are supported. An $\overline{\text{AEN}}$ input prevents the bus controller from driving the shared bus command and data signals except when enabled by an external bus arbiter such as the SAB 82289.
Separate DEN and DT/$\overline{\text{R}}$ outputs control the data transceivers for all buses. Bus contention is eliminated by disabling DEN before changing DT/$\overline{\text{R}}$. The DEN timing allows sufficient time for tristate bus drivers to enter tristate off before enabling other drivers onto the same bus.
The term CPU refers to any SAB 80286 processor or SAB 80286 support component which may become an SAB 80286 local bus master and thereby drive the SAB 82C288 status inputs.

Processor Cycle Definition

Any CPU which drives the local bus uses an internal clock which is one half the frequency of the system clock (CLK) (see figure below). Knowledge of the phase of the local bus master's internal clock is required for proper operation of the SAB 80286 local bus. The local bus master informs the bus controller of its internal clock phase when it asserts the status signals. Status signals are always asserted in phase 1 of the local bus master's internal clock.

CLK Relationship to the Processor Clock and Bus T-States

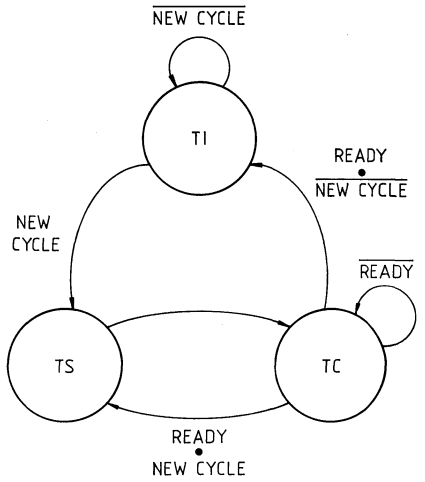


Bus State Definition

The SAB 82C288 bus controller has three bus states (see figure below): Idle (TI), Status (TS), and Command (TC). Each bus state is two CLK cycles long. Bus state phases correspond to the internal CPU processor clock phases.

The TI bus state occurs when no bus cycle is currently active on the SAB 80286 local bus. This state may be repeated indefinitely. When control of the local bus is being passed between masters, the bus remains in the TI state.

Bus States



Bus Cycle Definition

The $\overline{S1}$ and $\overline{S0}$ inputs signal the start of a bus cycle. When either input becomes low, a bus cycle is started. The TS bus state is defined to be the two CLK cycles during which either $\overline{S1}$ or $\overline{S0}$ is active (see figure on bus cycle definition). These inputs are sampled by the SAB 82C288 at every falling edge of CLK. When either $\overline{S1}$ or $\overline{S0}$ is sampled low, the next CLK cycle is considered the second phase of the internal CPU clock cycle.
The local bus enters the TC bus state after the TS state. The shortest bus cycle may have one TS state and one TC state. Longer bus cycles are formed by repeating TC states. A repeated TC bus state is called a wait state.

The $\overline{READY}$ input determines whether the current TC bus state is to be repeated. The $\overline{READY}$ input has the same timing and effect for all bus cycles. $\overline{READY}$ is sampled at the end of each TC bus state to see if it is active. If sampled high, the TC bus state is repeated. This is called inserting a wait state. The control and command outputs do not change during wait states.
When $\overline{READY}$ is sampled low, the current bus cycle is terminated. Note that the bus controller may enter the TS bus state directly from TC if the status lines are sampled active at the next falling edge of CLK.

Bus Cycle Definition

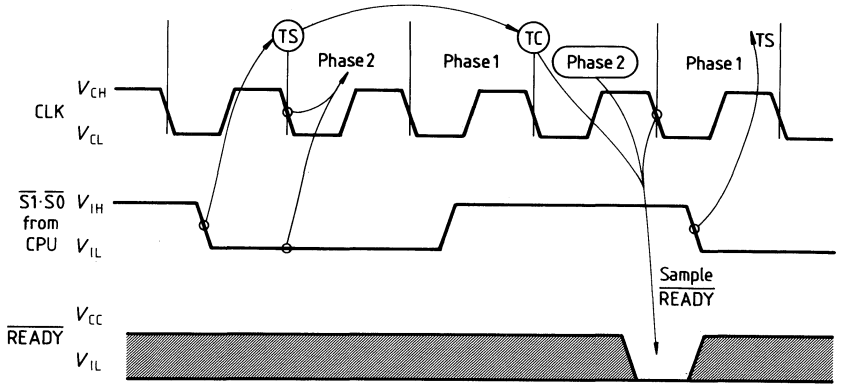


Table 2 Command and Control Output for Each Type of Bus Cycle

Type of bus cycle	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Command activated	DT/$\overline{R}$ state	ALE, DEN issued?	MCE issued?
Interrupt acknowledge	0	0	0	$\overline{INTA}$	low	yes	yes
I/O read	0	0	1	$\overline{IORC}$	low	yes	no
I/O write	0	1	0	$\overline{IOWC}$	high	yes	no
None; idle	0	1	1	none	high	no	no
Halt/shutdown	1	0	0	none	high	no	no
Memory read	1	0	1	$\overline{MRDC}$	low	yes	no
Memory write	1	1	0	$\overline{MWTC}$	high	yes	no
None; idle	1	1	1	none	high	no	no

Operating Modes

Two types of buses are supported by the SAB 82C288: Multibus and non-Multibus. When the MB input is high, Multibus timing is used. In Multibus mode, the SAB 82C288 delays command and data activation to meet IEEE-796 requirements on address to command active and write data to command active setup timing. Multibus mode requires at least one wait state in the bus cycle since the command outputs are delayed. The non-Multibus mode does not delay any outputs and does not require wait states. The MB input affects the timing of the command and DEN outputs.

Command and Control Outputs

The type of bus cycle performed by the local bus master is encoded in the M/$\overline{IO}$, $\overline{S1}$, and $\overline{S0}$ inputs. Different command and control outputs are activated depending on the type of bus cycle. Table 2 indicates the cycle decoding done by the SAB 82C288 and the effect on command, DT/$\overline{R}$, ALE, DEN, and MCE outputs.

Bus cycles come in three forms: read, write, and halt. Read bus cycles include memory read, I/O read, and interrupt acknowledge. The timing of the associated read command outputs ($\overline{MRDC}$, $\overline{IORC}$, and $\overline{INTA}$), control outputs (ALE, DEN, DT/$\overline{R}$) and control inputs (CEN/$\overline{AEN}$, CENL, CMDLY, MB, and $\overline{READY}$) are identical for all read bus cycles. Read cycles differ only in which command output is activated. The MCE control output is only asserted during interrupt acknowledge cycles.

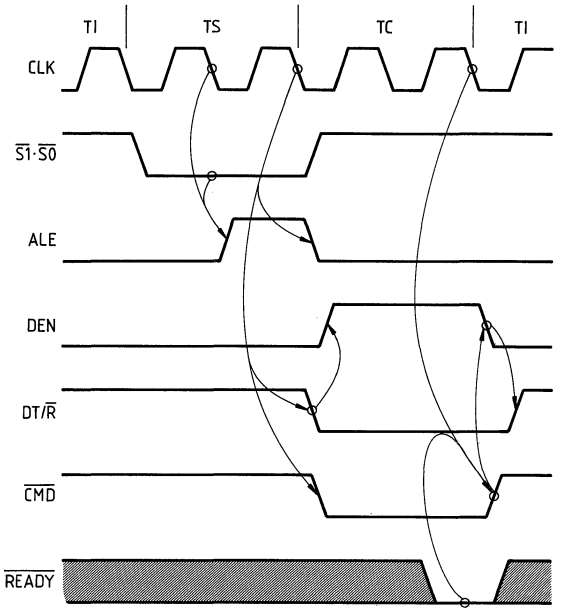
Write bus cycles activate different control and command outputs with different timing than read bus cycles. Memory write and I/O write are write bus cycles whose timing for command outputs ($\overline{MWTC}$ and $\overline{IOWC}$), control outputs (ALE, DEN, DT/$\overline{R}$) and control inputs (CEN/$\overline{AEN}$, CENL, CMDLY, MB, and $\overline{READY}$) are identical. They differ only in which command output is activated.

Halt bus cycles are different because no command or control output is activated. All control inputs are ignored until the next bus cycle is started via $\overline{S1}$ and $\overline{S0}$.

The basic command and control output timing for read and write bus cycles is shown in the next five figures. Halt bus cycles are not shown since they activate no outputs. The basic idle-read-idle and idle-write-idle bus cycles are shown. The signal label $\overline{CMD}$ represents the appropriate command output for the bus cycle. For those five figures, the CMDLY input is connected to GND and CENL to V_{CC}. The effects of CENL and CMDLY are described later in the section on control inputs.

The next two figures show non-Multibus cycles. MB is connected to GND while CEN is connected to V_{CC}. The figure on page 10 shows a read cycle with no wait states while the figure on page 11 shows a write cycle with one wait state. The $\overline{READY}$ input is shown to illustrate how wait states are added.

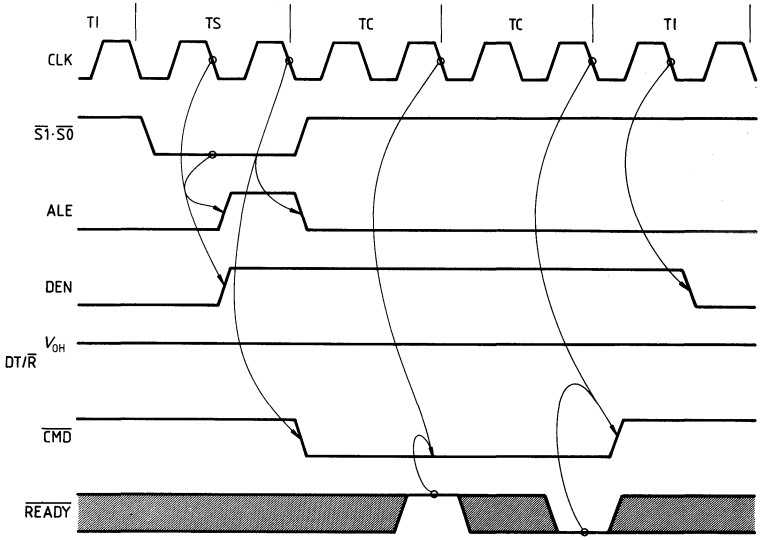
Idle-Read-Idle Bus Cycles with MB = 0



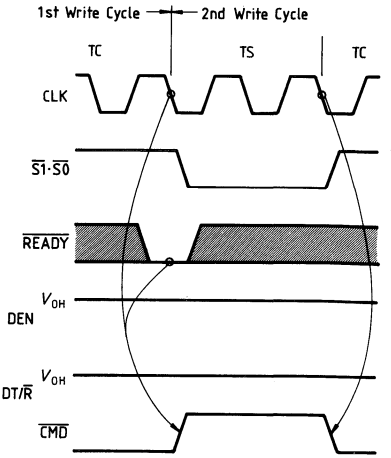
Bus cycles can occur back-to-back with no TI bus states between TC and TS. Back-to-back cycles do not affect the timing of the command and control outputs. Command and control outputs always reach the states shown for the same clock edge (within TS, TC, or following bus state) of a bus cycle. A special case in control timing occurs for back-to-back write cycles with MB = 0. In this case, DT/$\overline{R}$ and DEN remain high between the bus cycles (see respective write-write cycle diagram). The command and ALE output timing does not change.

The figures on pages 12 and 13 show a Multibus cycle with MB = 1. $\overline{AEN}$ and CMDLY are connected to GND. The effects of CMDLY and $\overline{AEN}$ are described later in the section on control inputs. The top figure shows a read cycle with one wait state and the figure below shows a write cycle with two wait states. The second wait state of the write cycle is shown only for example purposes and is not required. The $\overline{READY}$ input is shown to illustrate how wait states are added.

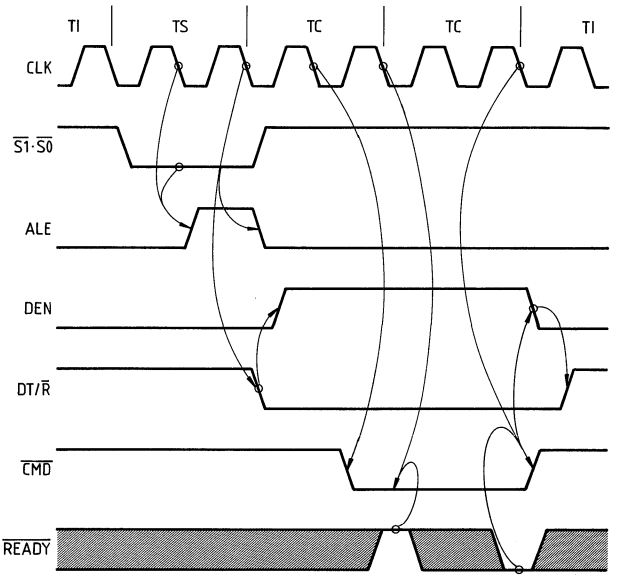
Idle-Write-Idle Bus Cycles with MB = 0



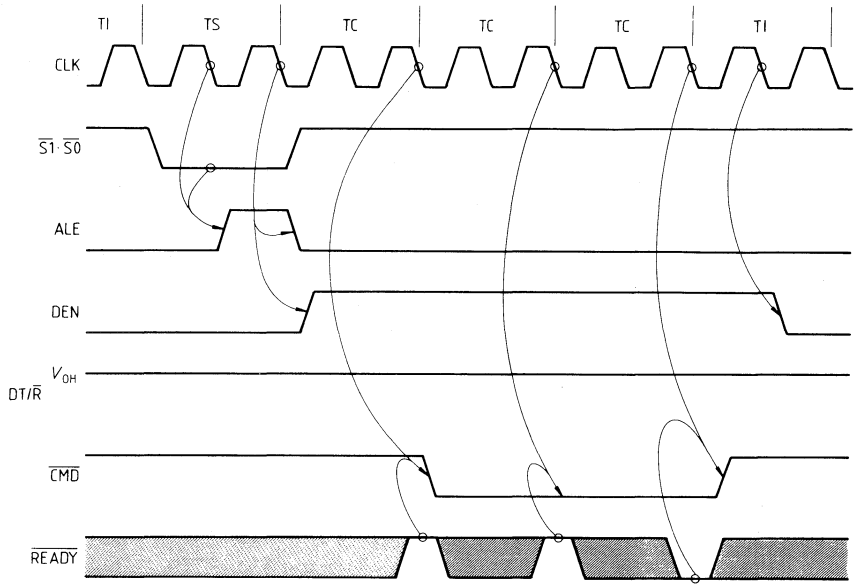
Write-Write Bus Cycles with MB = 0



Idle-Read-Idle Bus Cycles with MB = 1



Idle-Write-Idle Bus Cycles with MB = 1



The MB control input affects the timing of the command and DEN outputs. These outputs are automatically delayed in Multibus mode to satisfy three requirements:

1) 50 ns minimum setup time for valid address before any command output becomes active.
2) 50 ns minimum setup time for valid write data before any write command output becomes active.
3) 65 ns maximum time from when any read command becomes inactive until the slave's read data drivers reach tristate off.

Three signal transitions are delayed by MB = 1 as compared to MB = 0:

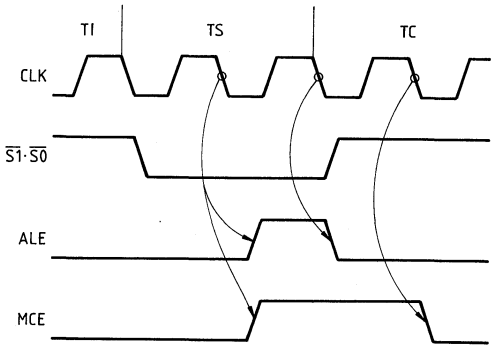
1) The high to low transition of the read command outputs ($\overline{IORC}$, $\overline{MRDC}$, and $\overline{INTA}$) is delayed one CLK cycle.
2) The high to low transition of the write command outputs ($\overline{IOWC}$ and $\overline{MWTC}$) is delayed two CLK cycles.
3) The low to high transition of DEN for write cycles is delayed one CLK cycle.

Back-to-back bus cycles with MB = 1 do not change the timing of any of the command or control outputs. DEN always becomes inactive between bus cycles with MB = 1.

Except for a halt or shutdown bus cycle, ALE will be issued during the second half of TS for any bus cycle. ALE becomes inactive at the end of the TS to allow latching the address to keep it stable during the entire bus cycle. The address outputs may change during phase 2 of any TC bus state. ALE is not affected by any control input.

The following figure shows how MCE is timed during interrupt acknowledge (INTA) bus cycles. MCE is one CLK cycle longer than ALE to hold the cascade address from a master SAB 8259A valid after the falling edge of ALE. With the exception of the MCE control output, an INTA bus cycle is identical in timing with a read bus cycle. MCE is not affected by any control input.

MCE Operation for an INTA Bus Cycle



Control Inputs

The control inputs can alter the basic timing of command outputs, allow interfacing to multiple buses, and share a bus between different masters. For many SAB 80286 systems, each CPU will have more than one bus which may be used to perform a bus cycle. Normally, a CPU will only have one bus controller active for each bus cycle. Some buses may be shared by more than one CPU (i.e. Multibus) requiring only one of them use the bus at a time.

Systems with multiple and shared buses use two control input signals of the SAB 82C288 bus controller, CENL and $\overline{AEN}$ (see figure on system use of those signals). CENL enables the bus controller to control the current bus cycle. The $\overline{AEN}$ input prevents a bus controller from driving its command outputs. $\overline{AEN}$ high means that another bus controller may be driving the shared bus.

In the figure on the $\overline{AEN}$ and CENL signal, two buses are shown: a local bus and a Multibus. Only one bus is used for each CPU bus cycle. The CENL inputs of the bus controllers select which bus controller is to perform the bus cycle. An address decoder determines which bus to use for each bus cycle. The SAB 82C288 connected to the shared Multibus must be selected by CENL and be given access to the Multibus by $\overline{AEN}$ before it will begin a Multibus operation.

CENL must be sampled high at the end of the TS bus state (see waveforms) to enable the bus controller to activate its command and control outputs. If sampled low the commands and DEN will not go active and DT/$\overline{R}$ will remain high. The bus controller will ignore the CMDLY, CEN, and $\overline{READY}$ inputs until another bus cycle is started via $\overline{S1}$ and $\overline{S0}$. Since an address decoder is commonly used to identify which bus is required for each bus cycle, CENL is latched to avoid the need for latching its input.

The CENL input can effect the DEN control output. When MB = 0, DEN normally becomes active during phase 2 of TS in write bus cycles. This transition occurs before CENL is sampled. If CENL is sampled low, the DEN output will be forced low during TC as shown in the timing waveforms.

When MB = 1, CEN/$\overline{AEN}$ becomes $\overline{AEN}$, $\overline{AEN}$ controls when the bus controller command outputs enter and exit tristate off. $\overline{AEN}$ is intended to be driven by a bus arbiter, like the SAB 82289, which assures only one bus controller is driving the shared bus at any time. When $\overline{AEN}$ makes a low to high transition, the command outputs immediately enter tristate off and DEN is forced inactive. An inactive DEN should force the local data transceivers connected to the shared data bus into tristate off (see next figure). The low to high transition of $\overline{AEN}$ should only occur during TI or TS bus states.

The high-to-low transition of $\overline{AEN}$ signals that the bus controller may now drive the shared bus command signals. Since a bus cycle may be active or be in the process of starting, $\overline{AEN}$ can become active during any T-state. $\overline{AEN}$ low immediately allows DEN to go to the appropriate state. Three CLK

edges later, the command outputs will go active (see timing waveforms). The Multibus requires this delay for the address and data to be valid on the bus before the commands become active.

When MB = 0, CEN/$\overline{\text{AEN}}$ becomes CEN. CEN is an asynchronous input which immediately affects the command and DEN outputs. When CEN makes a high-to-low transition, the commands and DEN are immediately forced inactive. When CEN makes a low-to-high transition, the commands and DEN outputs immediately go to the appropriate state (see timing waveforms). $\overline{\text{READY}}$ must still become active to terminate a bus cycle if CEN remains low for a selected bus controller (CENL was latched high).

Some memory or I/O systems may require more address or write data setup time to command active than provided by the basic command output timing. To provide flexible command timing, the CMDLY input can delay the activation of command outputs. The CMDLY input must be sampled low to activate the command outputs. CMDLY does not affect the control outputs ALE, MCE, DEN, and DT/$\overline{\text{R}}$.

CMDLY is first sampled on the falling edge of the CLK ending TS. If sampled high, the command output is not activated, and CMDLY is again sampled on the next falling edge of CLK. Once sampled low, the proper command output becomes active immediately if MB = 0. If MB = 1, the proper command goes active no earlier than shown in the figures on pages 12 and 13.

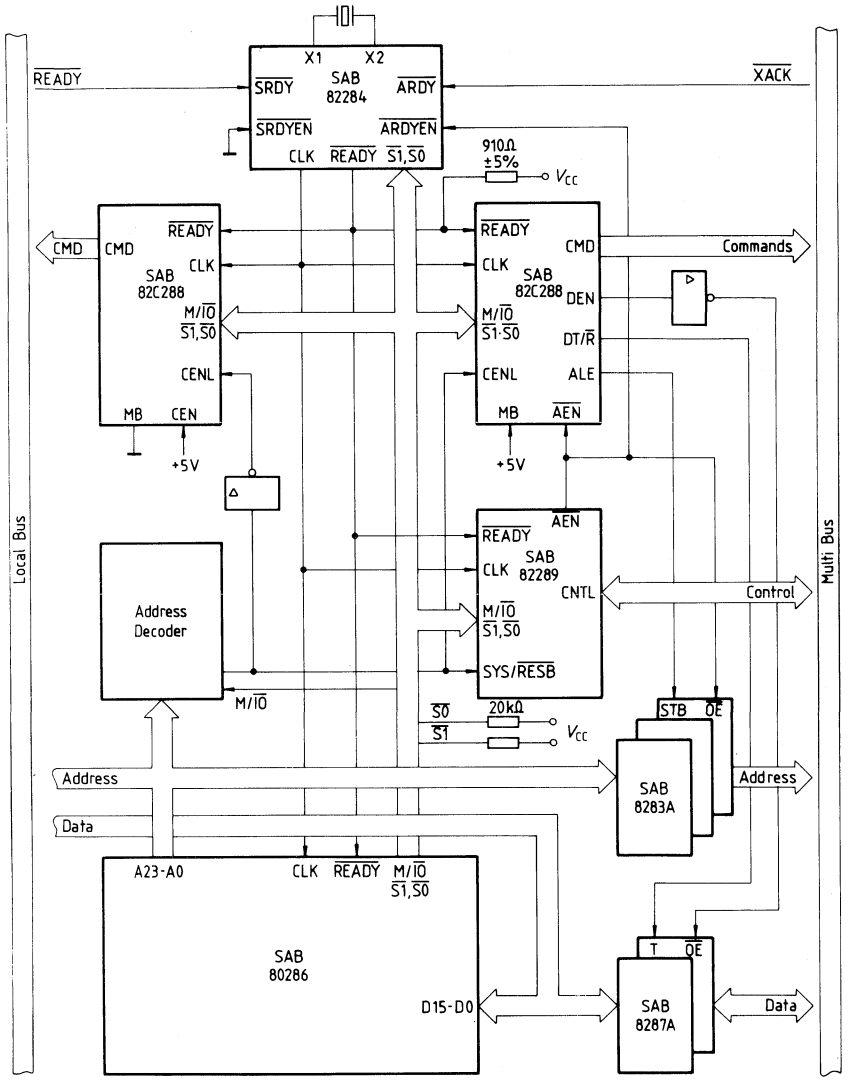
$\overline{\text{READY}}$ can terminate a bus cycle before CMDLY allows a command to be issued. In this case no commands are issued and the bus controller will deactivate DEN and DT/$\overline{\text{R}}$ in the same manner as if a command had been issued.

Waveforms

The waveforms show the timing relationships of inputs and outputs and do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown via the general cases. Special cases are shown when needed. The waveforms provide some functional descriptions of the SAB 82C288; however, most functional descriptions are provided in the figures of section Functional Description.

To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

System Use of $\overline{\text{AEN}}$ and CENL



Absolute Maximum Ratings [1)]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to GND	−0.5 to +7V
Power dissipation	1 W

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
I_{CC}	Power supply current	–	20	mA	at 8 MHz; outputs open
I_F	Forward input current ($\overline{S0}$, $\overline{S1}$, M/$\overline{IO}$)	–	−0.5	mA	V_F = 0.45 V
I_{LI}	Input leakage current (all other)	–	±10	µA	0 V ≦ V_{IN} ≦ V_{CC}
I_{LO}	Output leakage current	–	±10	µA	0.45 V ≦ V_{OUT} ≦ V_{CC}
V_{OL}	Low output voltage Command outputs Control outputs	–	0.45	V	 I_{OL} = 32 mA I_{OL} = 16 mA
V_{OH}	High output voltage Command outputs Control outputs	2.4	–	V	 I_{OH} = −5 mA I_{OH} = −1 mA
V_{IL}	Low input voltage	−0.5	0.8	V	–
V_{CL}	CLK low input voltage	−0.5	0.6	V	–
V_{IH}	High input voltage	2.0	V_{CC} +0.5	V	–
V_{CH}	CLK high input voltage	3.8		V	–

Capacitance

T_A = 25°C, V_{CC} = GND = 0 V, f_C = 1 MHz

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
C_I	Input capacitance	–	10	pF	Unmeasured pins returned to GND
C_{IO}	Input/output capacitance	–	20	pF	

Note: These parameters are periodically sampled, not 100% tested.

[1)] Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics SAB 82C288

T_A = 0 to 70°C, V_{CC} = 5 V ±10%

Unless otherwise specified, the AC timings are referred to signal points of 0.8 V and 2.0 V as illustrated in the waveforms.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_1	CLK period	62	250	ns	–
t_2	CLK high time	20	235	ns	at 3.6 V
t_3	CLK low time	15	230	ns	at 1.0 V
t_4	CLK rise time	–	10	ns	1.0 to 3.6 V
t_5	CLK fall time	–	10	ns	3.6 to 1.0 V
t_6	M/$\overline{IO}$ and status setup time	22	–	ns	–
t_7	M/$\overline{IO}$ and status hold time	0	–	ns	–
t_8	CENL setup time	20	–	ns	–
t_9	CENL hold time	0	–	ns	–
t_{10}	$\overline{READY}$ setup time	38	–	ns	–
t_{11}	$\overline{READY}$ hold time	25	–	ns	–
t_{12}	CMDLY setup time	20	–	ns	–
t_{13}	CMDLY hold time	0	–	ns	–
t_{14}	$\overline{AEN}$ setup time	20	–	ns	1)
t_{15}	$\overline{AEN}$ hold time	0	–	ns	1)
t_{16}	ALE, MCE active delay	3	20	ns	2)
t_{17}	ALE, MCE inactive delay	–	20	ns	2)
t_{18}	DEN (write) inactive from CENL	–	35	ns	2)
t_{19}	DT/$\overline{R}$ low from CLK	–	25	ns	2)
t_{20}	DEN (read) active from DT/$\overline{R}$	5	35	ns	2)
t_{21}	DEN (read) inactive delay	3	35	ns	2)
t_{22}	DT/$\overline{R}$ high from DEN inactive	5	35	ns	2)
t_{23}	DEN (write) active delay	–	30	ns	2)
t_{24}	DEN (write) inactive delay	3	30	ns	2)
t_{25}	DEN inactive from CEN	–	25	ns	2)
t_{26}	DEN active from CEN	–	30	ns	2)
t_{27}	DT/$\overline{R}$ high from CLK and CEN	–	35	ns	2) 3)
t_{28}	DEN active from $\overline{AEN}$	–	30	ns	2)

Notes see next page

AC Characteristics SAB 82C288 (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{29}	Command active delay	3	25	ns	[4]
t_{30}	Command inactive delay	3	25	ns	[4]
t_{31}	Command inactive from CEN	–	25	ns	[4]
t_{32}	Command active from CEN	–	25	ns	[4]
t_{33}	Command valid delay from $\overline{AEN}$	–	40	ns	[4]
t_{34}	Command float time	–	40	ns	[4]
t_{35}	MB setup time	20	–	ns	–
t_{36}	MB hold time	0	–	ns	–
t_{37}	Command inactive enable from MB↓	–	40	ns	[4]
t_{38}	Command float time from MB↑	–	40	ns	–
t_{39}	DEN inactive from MB↑	–	30	ns	[2]
t_{40}	DEN active from MB↓	–	35	ns	[2]

[1] $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold times are specified to guarantee the response shown in the waveforms.

[2] Control output load: $C_L = 150$ pF, $I_{OL} = 16$ mA, $I_{OH} = -1$ mA.

[3] t_{27} only applies to bus cycles where MB = 0, the SAB 82C288 was selected, and DEN = 0 when the cycle is terminated (because CEN = 0).

[4] Command output load: $C_L = 300$ pF, $I_{OL} = 32$ mA, $I_{OH} = -5$ mA.

AC Characteristics SAB 82C288-1

T_A = 0 to 70°C, V_{CC} = 5 V ±10%

Unless otherwise specified, the AC timings are referred to signal points of 0.8 V and 2.0 V as illustrated in the waveforms.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_1	CLK period	50	250	ns	–
t_2	CLK high time	16	235	ns	at 3.6 V
t_3	CLK low time	12	230	ns	at 1.0 V
t_4	CLK rise time	–	8	ns	1.0 to 3.6 V
t_5	CLK fall time	–	8	ns	3.6 to 1.0 V
t_6	M/$\overline{IO}$ and status setup time	18	–	ns	–
t_7	M/$\overline{IO}$ and status hold time	0	–	ns	–
t_8	CENL setup time	15	–	ns	–
t_9	CENL hold time	0	–	ns	–
t_{10}	$\overline{READY}$ setup time	26	–	ns	–
t_{11}	$\overline{READY}$ hold time	25	–	ns	–
t_{12}	CMDLY setup time	15	–	ns	–
t_{13}	CMDLY hold time	0	–	ns	–
t_{14}	$\overline{AEN}$ setup time	15	–	ns	1)
t_{15}	$\overline{AEN}$ hold time	0	–	ns	1)
t_{16}	ALE, MCE active delay	3	16	ns	2)
t_{17}	ALE, MCE inactive delay	–	19	ns	2)
t_{18}	DEN (write) inactive from CENL	–	23	ns	2)
t_{19}	DT/$\overline{R}$ low from CLK	–	23	ns	2)
t_{20}	DEN (read) active from DT/$\overline{R}$	5	21	ns	2)
t_{21}	DEN (read) inactive delay	3	21	ns	2)
t_{22}	DT/$\overline{R}$ high from DEN inactive	5	20	ns	2)
t_{23}	DEN (write) active delay	–	23	ns	2)
t_{24}	DEN (write) inactive delay	3	19	ns	2)
t_{25}	DEN inactive from CEN	–	25	ns	2)
t_{26}	DEN active from CEN	–	24	ns	2)
t_{27}	DT/$\overline{R}$ high from CLK and CEN	–	25	ns	2) 3)
t_{28}	DEN active from $\overline{AEN}$	–	26	ns	2)

Notes see next page

AC Characteristics SAB 82C288-1 (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{29}	Command active delay	3	21	ns	[4]
t_{30}	Command inactive delay	3	20	ns	[4]
t_{31}	Command inactive from CEN	–	25	ns	[4]
t_{32}	Command active from CEN	–	25	ns	[4]
t_{33}	Command valid delay from $\overline{AEN}$	–	40	ns	[4]
t_{34}	Command float time	–	40	ns	[4]
t_{35}	MB setup time	20	–	ns	–
t_{36}	MB hold time	0	–	ns	–
t_{37}	Command inactive enable from MB↓	–	40	ns	[4]
t_{38}	Command float time from MB↑	–	40	ns	–
t_{39}	DEN inactive from MB↑	–	26	ns	[2]
t_{40}	DEN active from MB↓	–	35	ns	[2]

[1] $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold times are specified to guarantee the response shown in the waveforms.

[2] Control output load: $C_L = 150$ pF, $I_{OL} = 16$ mA, $I_{OH} = -1$ mA.

[3] t_{27} only applies to bus cycles where MB = 0, the SAB 82C288 was selected, and DEN = 0 when the cycle is terminated (because CEN = 0).

[4] Command output load: $C_L = 300$ pF, $I_{OL} = 32$ mA, $I_{OH} = -5$ mA.

AC Characteristics SAB 82C288-12

T_A = 0 to 70°C, V_{CC} = 5 V ±10%

Unless otherwise specified, the AC timings are referred to signal points of 0.8 V and 2.0 V as illustrated in the waveforms.

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_1	CLK period	40	250	ns	–
t_2	CLK high time	13	239	ns	at 3.6 V
t_3	CLK low time	11	237	ns	at 1.0 V
t_4	CLK rise time	–	8	ns	1.0 to 3.6 V
t_5	CLK fall time	–	8	ns	3.6 to 1.0 V
t_6	M/$\overline{IO}$ and status setup time	15	–	ns	–
t_7	M/$\overline{IO}$ and status hold time	0	–	ns	–
t_8	CENL setup time	15	–	ns	–
t_9	CENL hold time	0	–	ns	–
t_{10}	$\overline{READY}$ setup time	18	–	ns	–
t_{11}	$\overline{READY}$ hold time	20	–	ns	–
t_{12}	CMDLY setup time	15	–	ns	–
t_{13}	CMDLY hold time	0	–	ns	–
t_{14}	$\overline{AEN}$ setup time	15	–	ns	1)
t_{15}	$\overline{AEN}$ hold time	0	–	ns	1)
t_{16}	ALE, MCE active delay	3	16	ns	2)
t_{17}	ALE, MCE inactive delay	–	19	ns	2)
t_{18}	DEN (write) inactive from CENL	–	23	ns	2)
t_{19}	DT/$\overline{R}$ low from CLK	–	23	ns	2)
t_{20}	DEN (read) active from DT/$\overline{R}$	5	21	ns	2)
t_{21}	DEN (read) inactive delay	3	19	ns	2)
t_{22}	DT/$\overline{R}$ high from DEN inactive	5	18	ns	2)
t_{23}	DEN (write) active delay	–	23	ns	2)
t_{24}	DEN (write) inactive delay	3	19	ns	2)
t_{25}	DEN inactive from CEN	–	25	ns	2)
t_{26}	DEN active from CEN	–	24	ns	2)
t_{27}	DT/$\overline{R}$ high from CLK and CEN	–	25	ns	2) 3)
t_{28}	DEN active from $\overline{AEN}$	–	26	ns	2)

Notes see next page

AC Characteristics SAB 82C288-12 (cont'd)

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
t_{29}	Command active delay	3	21	ns	[4]
t_{30}	Command inactive delay	3	20	ns	[4]
t_{31}	Command inactive from CEN	–	25	ns	[4]
t_{32}	Command active from CEN	–	25	ns	[4]
t_{33}	Command valid delay from $\overline{AEN}$	–	40	ns	[4]
t_{34}	Command float time	–	40	ns	[4]
t_{35}	MB setup time	20	–	ns	–
t_{36}	MB hold time	0	–	ns	–
t_{37}	Command inactive enable from MB↓	–	40	ns	[4]
t_{38}	Command float time from MB↑	–	40	ns	–
t_{39}	DEN inactive from MB↑	–	26	ns	[2]
t_{40}	DEN active from MB↓	–	30	ns	[2]

[1] $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold times are specified to guarantee the response shown in the waveforms.

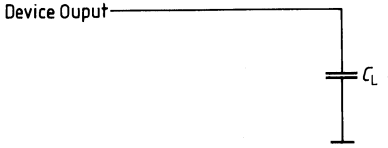
[2] Control output load: $C_L = 150$ pF, $I_{OL} = 16$ mA, $I_{OH} = -1$ mA.

[3] t_{27} only applies to bus cycles where MB = 0, the SAB 82C288 was selected, and DEN = 0 when the cycle is terminated (because CEN = 0).

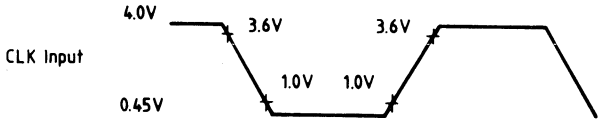
[4] Command output load: $C_L = 300$ pF, $I_{OL} = 32$ mA, $I_{OH} = -5$ mA.

AC Testing Waveforms

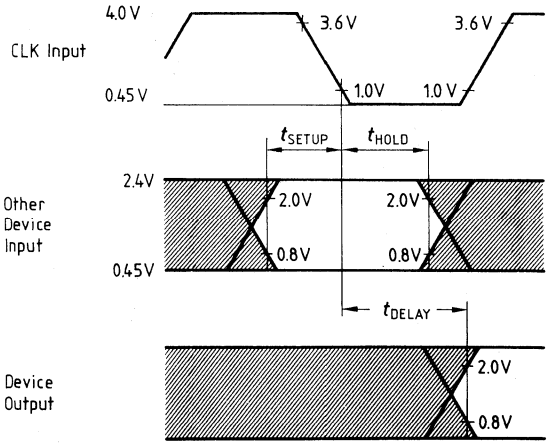
Test Loading on Outputs



Drive and Measurement Points – CLK Input

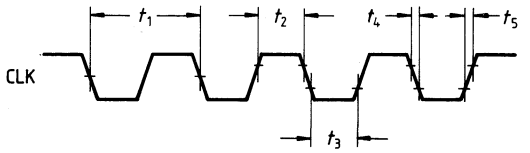


Setup, Hold and Delay Time Measurement – General

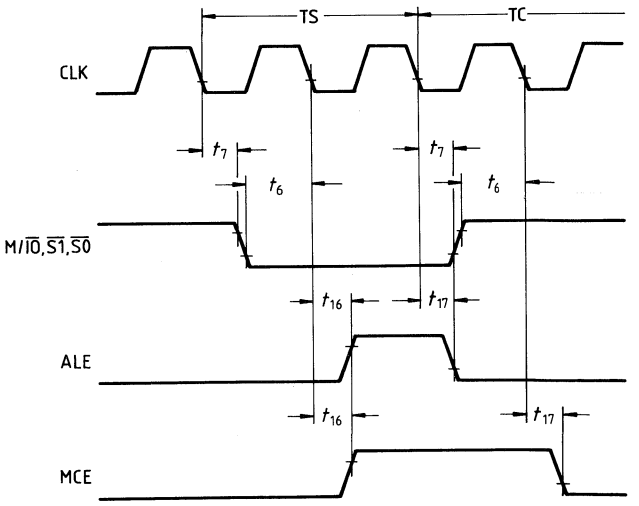


Waveforms

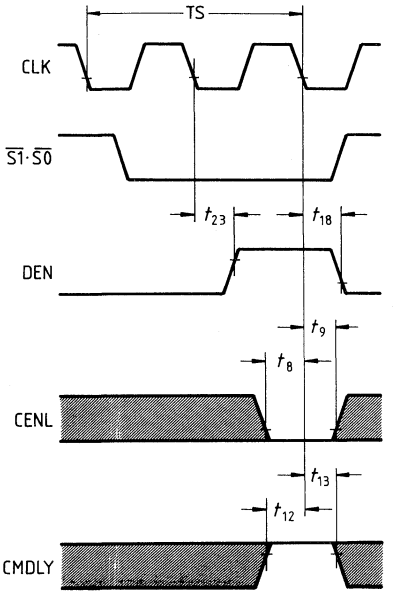
CLK Characteristics



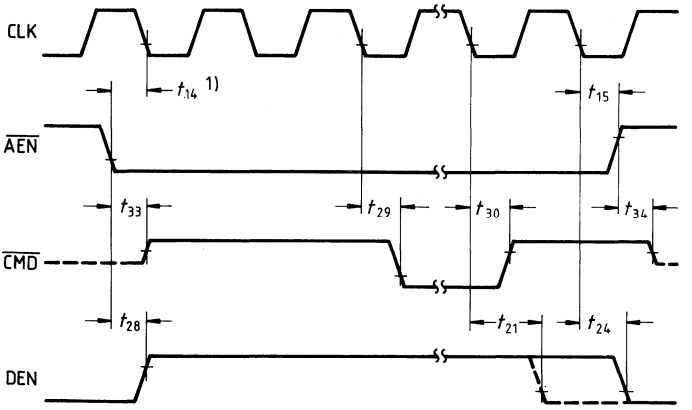
Status, ALE, MCE Characteristics



CENL, CMDLY, DEN Characteristics with MB = 0 and CEN = 1 during Write Cycle

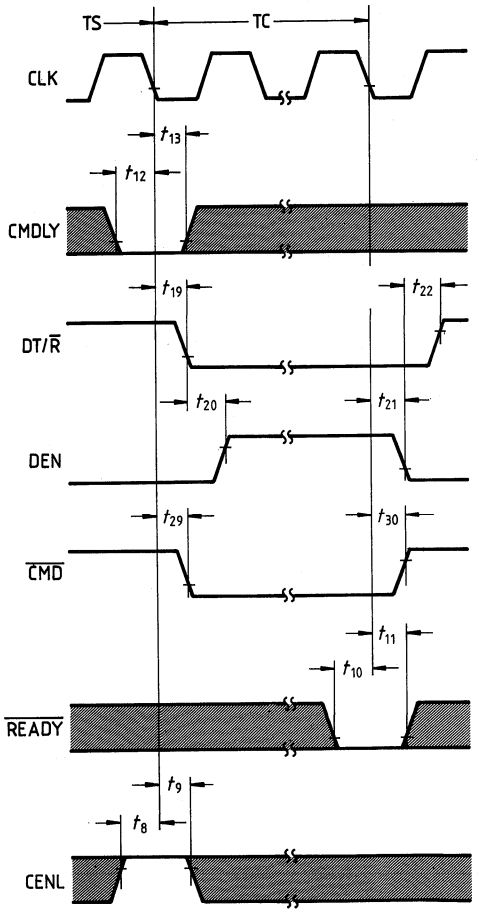


AEN Characteristics with MB = 1

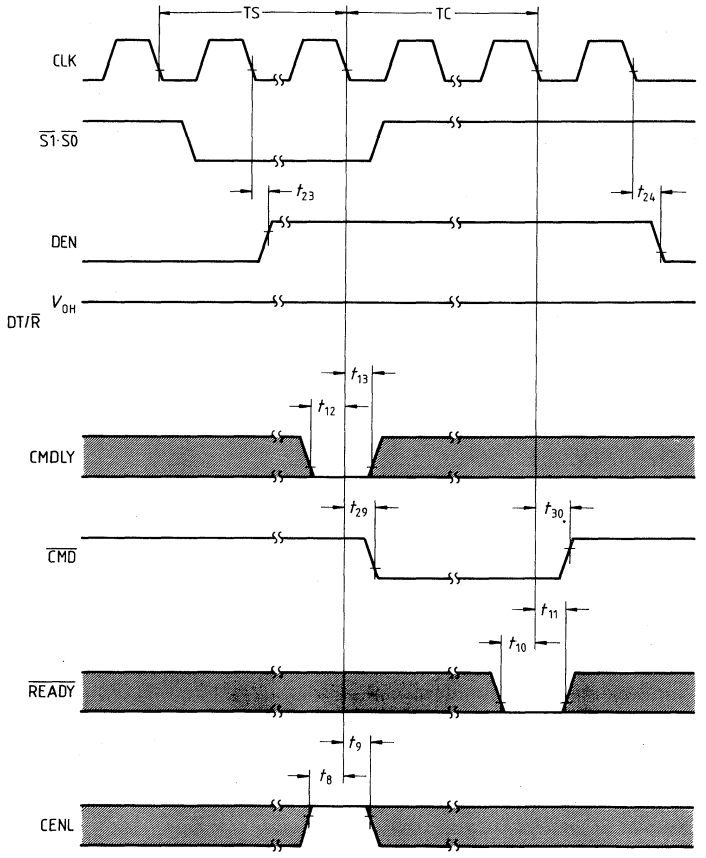


1) AEN is an asynchronous input. AEN setup and hold time is specified to guarantee the response shown in the waveforms.

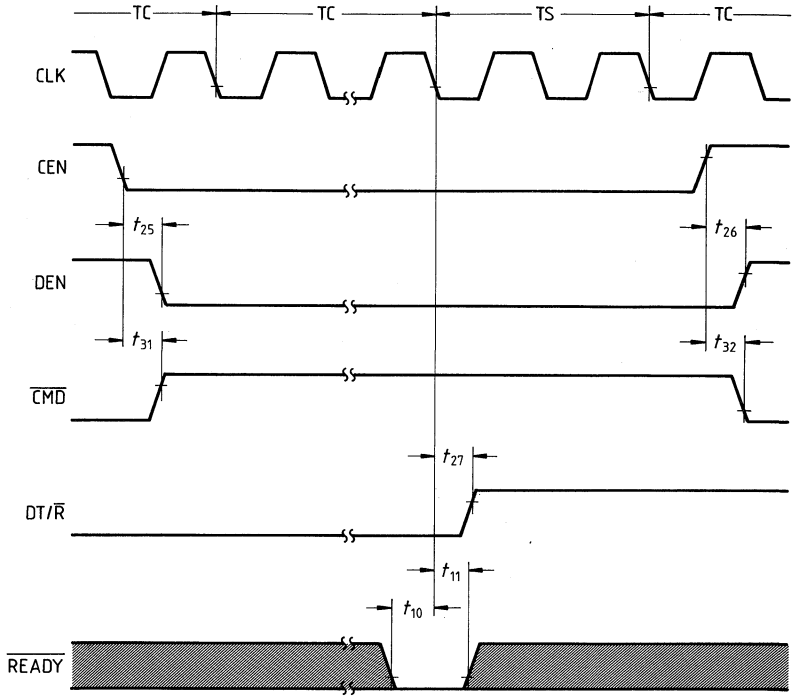
Read Cycle Characteristics with MB = 0 and CEN = 1



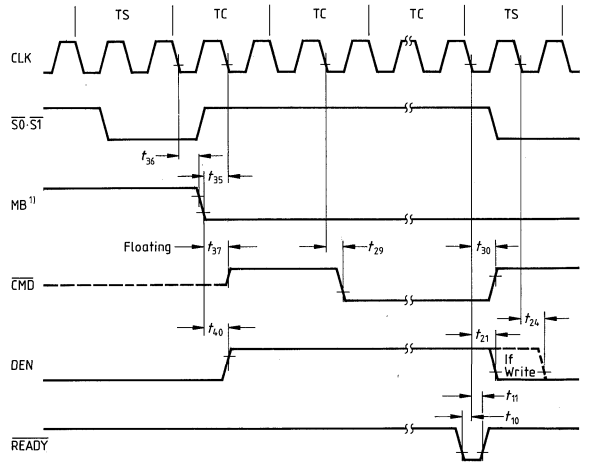
Write Cycle Characteristics with MB = 0 and CEN = 1

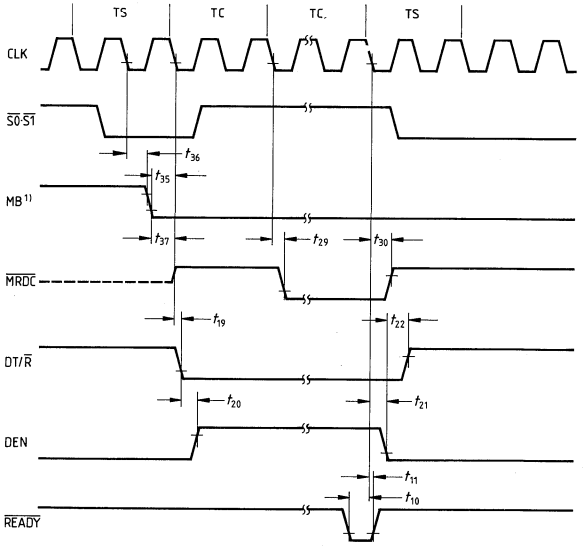


CEN Characteristics with MB = 0



MB Characteristics with $\overline{AEN}$/CEN = High

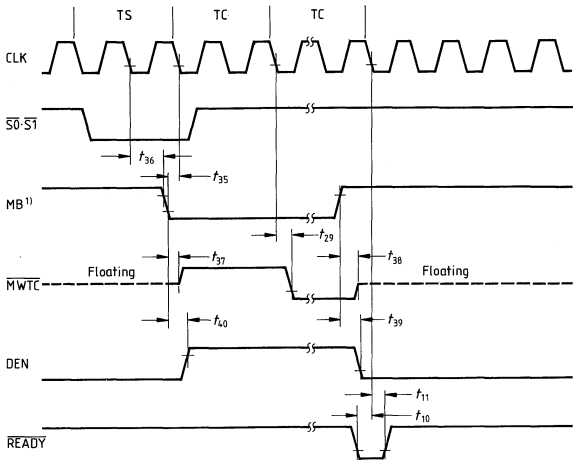




1) MB is an asynchronous input. MB setup and hold times specified to guarantee the response shown in the waveforms.

If the setup time t_{35} is met, two clock cycles will occur before $\overline{CMD}$ becomes active after the falling edge of MB.

MB Characteristics with $\overline{AEN}$/CEN = High (cont'd)

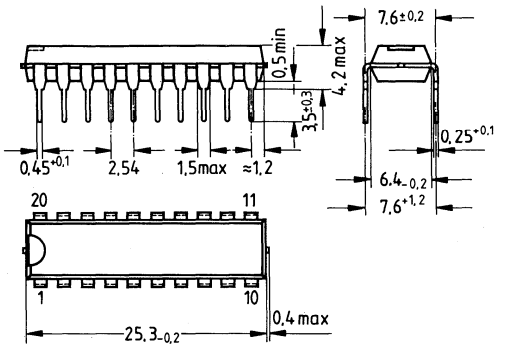


1) MB is an asynchronous input. MB setup and hold times specified to guarantee the response shown in the waveforms.

If the setup time t_{35} is met, two clock cycles will occur before $\overline{CMD}$ becomes active after the falling edge of MB.

Package Outlines

Plastic Package, P-DIP, 20 Pins



Dimensions in mm

Ordering Information

Type	Ordering code	Description
SAB 82C288-P	Q67120-Y138	Bus controller (plastic package) up to 16 MHz
SAB 82C288-1-P	Q67120-P258	Bus controller (plastic package) up to 20 MHz
SAB 82C288-12-P	Q67120-P259	Bus controller (plastic package) up to 25 MHz

Preliminary

SAB 82289 Bus Arbiter for SAB 80286 Processors

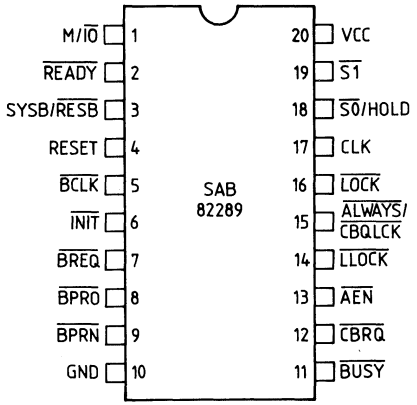
SAB 82289-6 up to 12 MHz

- Supports multimaster system bus arbitration protocol
- Synchronizes SAB 80286 processor with multimaster bus
- Compatible with IEEE 796 standard bus (Multibus®)

SAB 82289 up to 16 MHz

- Three modes of bus release operation for flexible system configuration
- Supports parallel, serial and rotating priority resolving schemes

Pin Configuration



Pin Names

S0/HOLD	Status S0/Hold Input
S1, M/IO	Status Inputs
BUSY	Busy Input/Output
READY	Ready Input
SYSB/RESB	System/Resident Bus
RESET	Processor Reset
BCLK	Bus Clock
INIT	Initialize
BREQ	Bus Request
BPRO	Bus Priority Out
BPRN	Bus Priority In
CLK	System Clock
AEN	Address Enable
ALWAYS/ CBQLCK	Always Release/ Common Bus Request Lock
LLOCK	Level Lock
CBRQ	Common Bus Request
LOCK	Bus Lock
VCC	+5V
GND	Ground (0V)

The SAB 82289 Bus Arbiter is a 5 V, 20-pin MYMOS component for use in multiple bus master SAB 80286 systems. The SAB 82289 provides a compact solution to system bus arbitration for the SAB 80286 CPU.

The complete IEEE 796 Standard bus arbitration protocol is supported. Three modes of bus release operation support a number of bus usage models.

Multibus® is a registered trademark of Intel Corporation.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
M/$\overline{IO}$, $\overline{S1}$	1, 19	I	STATUS INPUTS are the status input signal pins from the SAB 80286 processor. The arbiter decodes these inputs together with the $\overline{S0}$ /HOLD input to initiate bus request and surrender actions. A bus cycle is started when either $\overline{S1}$ or $\overline{S0}$ is sampled low at the falling edge of CLK. The SAB 80286's $\overline{S1}$ and M/$\overline{IO}$ pins meet the setup and hold time requirements of these pins.
			SAB 80286 Bus Cycle Status Encoding
			M/$\overline{IO}$ | $\overline{S1}$ | $\overline{S0}$/HOLD | Type of Bus Cycle 0 | 0 | 0 | Interrupt acknowledge 0 | 0 | 1 | I/O read 0 | 1 | 0 | I/O write 0 | 1 | 1 | None, bus idle 1 | 0 | 0 | Halt or shutdown 1 | 0 | 1 | Memory read 1 | 1 | 0 | Memory write 1 | 1 | 1 | None, bus idle
			When supporting the HOLD output of another bus master, the $\overline{S1}$ and M/$\overline{IO}$ pins must be held high during TS, the Status Cycle, for proper operation.
$\overline{READY}$	2	I	$\overline{READY}$ is an active-low signal which indicates the end of the bus cycle. The SAB 80286 halt or shutdown cycle does not require $\overline{READY}$ to terminate the bus cycle. Setup and hold times for this pin must be met for proper operation.
SYSB/$\overline{RESB}$	3	I	SYSTEM BUS/$\overline{RESIDENT\ BUS}$ is an input signal which determines whether the multimaster system bus is required for the current bus cycle. The signal can originate from address mapping circuitry such as a decoder or PROM attached to the processor address and status pins. The arbiter will request or retain control of the multimaster system bus when the SYSB/$\overline{RESB}$ pin is sampled high at the end of the TS bus state. During an interrupt acknowledge cycle, this input is sampled on every falling edge of CLK starting at the end of the TS state until either SYSB/$\overline{RESB}$ is sampled high or the bus cycle is terminated by the $\overline{READY}$ signal. Setup and hold times for this pin must be met for proper operation.
RESET	4	I	PROCESSOR RESET is an active-high input synchronous to the system clock (CLK). RESET is the processsor initialization and an indication to the arbiter to release the multimaster bus and clear any pending request.
$\overline{BCLK}$	5	I	$\overline{BUS\ CLOCK}$ is the multimaster system bus clock to which the multimaster bus interface signals are synchronized. $\overline{BCLK}$ can be asynchronous to CLK.
$\overline{INIT}$	6	I	$\overline{INITIALIZE}$ is an active-low Multibus signal used to reset all arbiters on the Multibus system. It will cause the release of the multimaster bus, but will not clear the pending bus master request so that the arbiter can again request the multimaster bus. No arbiters have the use of the multimaster bus immediately after initialization. $\overline{INIT}$ is an asynchronous signal to CLK.

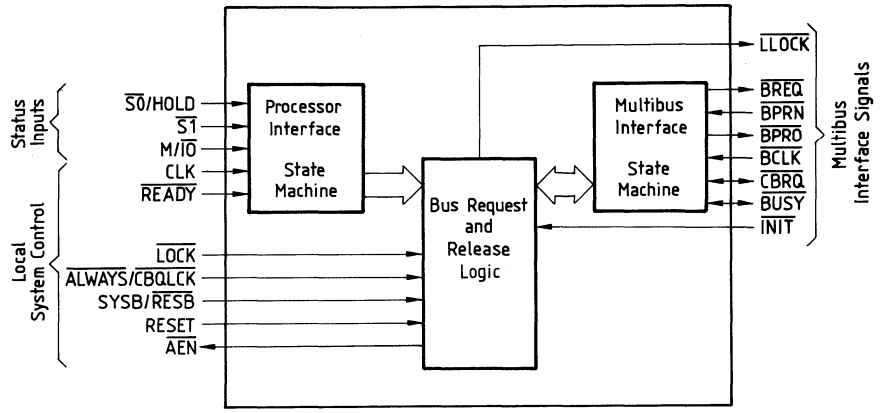
Pin Definitions and Functions (continued)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{BREQ}}$	7	O	$\overline{\text{BUS REQUEST}}$ is an active-low output signal used in the parallel and rotating priority resolving schemes. The arbiter activates $\overline{\text{BREQ}}$ to request the use of the multimaster system bus. The arbiter holds $\overline{\text{BREQ}}$ active as long as it is requesting or has possession of the multimaster system bus.
$\overline{\text{BPRO}}$	8	O	$\overline{\text{BUS PRIORITY OUT}}$ is an active-low output signal used in serial priority resolving scheme. $\overline{\text{BPRO}}$ is connected to $\overline{\text{BPRN}}$ of the next lower priority arbiter to grant or revoke priority from that arbiter.
$\overline{\text{BPRN}}$	9	I	$\overline{\text{BUS PRIORITY IN}}$ is an active-low input indicating that this arbiter has the highest priority of any arbiter requesting the system bus. $\overline{\text{BPRN}}$ high signals the arbiter that a higher priority arbiter is requesting or has possession of the system bus. Setup and hold times for this pin must be met for proper operation.
$\overline{\text{BUSY}}$	11	I/O (open-drain)	$\overline{\text{BUSY}}$ is a Multibus signal which is asserted when the system bus is in use. $\overline{\text{BUSY}}$ is an open drain input/output requiring an external pullup resistor. As an input $\overline{\text{BUSY}}$ asserted indicates when the Multibus is in use. Setup and hold times must be met for proper operation. As an output $\overline{\text{BUSY}}$ is asserted to signal when this arbiter has taken control of the Multibus.
$\overline{\text{CBRQ}}$	12	I/O (open-drain)	$\overline{\text{COMMON BUS REQUEST}}$ is a Multibus signal that indicates when an arbiter is requesting the Multibus. This pin is an open-drain input/output requiring an external pullup resistor. As an input $\overline{\text{CBRQ}}$ indicates that another arbiter is requesting the multimaster system bus. The input function of this pin is enabled by the $\overline{\text{CBQLCK}}$ signal. Setup and hold times for this pin must be met for proper operation. As an output $\overline{\text{CBRQ}}$ is asserted to indicate that this arbiter is requesting the Multibus. The arbiter pulls $\overline{\text{CBRQ}}$ low when it issues $\overline{\text{BREQ}}$. The arbiter releases $\overline{\text{CBRQ}}$ when it obtains the Multibus.
$\overline{\text{AEN}}$	13	O	$\overline{\text{ADDRESS ENABLE}}$ is the output of the arbiter which goes directly to the processor's address latches, the SAB 82288 bus controller and the SAB 82284 clock generator. $\overline{\text{AEN}}$ asserted causes the bus controller and address latches to enable their output drivers. $\overline{\text{AEN}}$ also drives the clock generator's $\overline{\text{ARDYEN}}$ input to enable its asynchronous ready input ($\overline{\text{ARDY}}$). $\overline{\text{AEN}}$ can also be used as an active-low hold acknowledge to a bus master other than the SAB 80286. It signals to the bus master that control of the system bus has been relinquished when $\overline{\text{AEN}}$ is inactive (high). Note that $\overline{\text{AEN}}$ goes active relative to $\overline{\text{BCLK}}$ and goes inactive relative to CLK.

Pin Definitions and Functions (continued)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{LLOCK}}$	14	O	$\overline{\text{LEVEL LOCK}}$ is an active-low output signal decoded from the processor $\overline{\text{LOCK}}$ signal. $\overline{\text{LLOCK}}$ can be used as Multibus $\overline{\text{LOCK}}$ when buffered with a tri-state buffer enabled by the $\overline{\text{AEN}}$ signal. $\overline{\text{LLOCK}}$ will be cleared by RESET but not by $\overline{\text{INIT}}$.
$\overline{\text{ALWAYS}}$/ $\overline{\text{CBQLCK}}$	15	I	$\overline{\text{ALWAYS RELEASE}}$ or $\overline{\text{COMMON BUS REQUEST LOCK}}$ can be programmed at processor reset to be either the ALWAYS RELEASE ($\overline{\text{ALWAYS}}$) strapping option or the COMMON BUS REQUEST LOCK ($\overline{\text{CBQLCK}}$) control input. Setup and hold times for this pin must be met for proper programming. When this pin is low during the falling edge of processor reset ($\overline{\text{ALWAYS}}$ option) the arbiter is programmed to surrender the multimaster system bus after each bus transfer cycle. The SAB 82289 will remain in the ALWAYS RELEASE mode until it is reprogrammed during the next processor reset. The bus arbiter is programmed to support the COMMON BUS REQUEST LOCK function by forcing this input pin high during the falling edge of the processor reset. $\overline{\text{CBQLCK}}$ itself is an active-low signal which when active prevents the arbiter from surrendering the multimaster system bus to a common bus request through the $\overline{\text{CBRQ}}$ input pin.
$\overline{\text{LOCK}}$	16	I	$\overline{\text{LOCK}}$ is a processor-generated signal which when asserted (low) prevents the arbiter from surrendering the multimaster system bus to any other bus arbiter, regardless of its priority. $\overline{\text{LOCK}}$ is sampled by the arbiter at the end of the TS (status) bus state. Setup and hold times for this pin must be met for proper operation.
CLK	17	I	SYSTEM CLOCK accepts the CLK signal from the SAB 82284 clock generator chip as the timing reference for the bus arbiter and processor interface signals.
$\overline{\text{S0}}$/HOLD	18	I	STATUS INPUT $\overline{\text{S0}}$ or HOLD is either the $\overline{\text{S0}}$ status signal from the SAB 80286 or the HOLD signal from some other bus master. The function of this input is established during the processor reset of the SAB 82289 bus arbiter. The SAB 80286 $\overline{\text{S0}}$ pin meets the setup and hold time requirements of this pin. The $\overline{\text{S0}}$ pin function is selected by forcing this input high during the falling edge of processor reset if the SAB 82289 is used to support an SAB 80286 processor, the $\overline{\text{S0}}$ output of the processor will be high during reset. In supporting the SAB 80286 processor, the SAB 82289 decodes the $\overline{\text{S0}}$ pin together with the other status input $\overline{\text{S1}}$ and M/$\overline{\text{IO}}$ to determine the beginning of a processor bus cycle and initiate bus request and surrender actions. The HOLD function of the $\overline{\text{S0}}$/HOLD pin is selected by holding this input low during the falling edge of processor reset. When supporting a bus master other than SAB 80286 the SAB 82289 monitors the HOLD signal to initiate bus request and surrender actions.
VCC	20	–	POWER SUPPLY (+5V)
GND	10	–	GROUND (0V)

Figure 1
Block Diagram



Functional Description

The SAB 82289 bus arbiter in conjunction with the SAB 82288 bus controller and the SAB 82284 clock generator interfaces the SAB 80286 processor or some other bus master to a multimaster system bus. The arbiter multiplexes a processor to a multimaster system bus. It avoids contention with other bus masters.

The SAB 82289 has two separate state machines which communicate through bus request and release logic. The processor interface state machine is synchronous with the local system clock (CLK) and the multimaster system bus interface state machine is synchronous with the bus clock ($\overline{BCLK}$).

The SAB 82289 performs all signaling to request, obtain, and release the system bus. External logic is used to determine which bus cycles require the system bus and to resolve priorities of simultaneous requests for control of the system bus.

SAB 82289 with SAB 80286

In a SAB 80286 system using a SAB 82289 bus arbiter, the SAB 80286 processor is unaware of the arbiter's existence and issues commands as though it had exclusive use of a multimaster system bus, such as Multibus. If the processor cycle requires Multibus access, the arbiter requests control of the Multibus. Until the request is granted the SAB 82289 keeps $\overline{AEN}$ disabled to prevent the SAB 82288 bus controller and the address latches from accessing the Multibus. $\overline{AEN}$ inactive also disasserts the asynchronous ready enable ($\overline{ARDYEN}$) input of the SAB 82284 clock chip so that the system bus will appear as "NOT READY" to the SAB 80286 processor.

Once the SAB 82289 bus arbiter has acquired the bus, it will assert $\overline{AEN}$ allowing the SAB 82288 bus controller and the address latches to access the system bus and asserting the $\overline{ARDYEN}$ input of the SAB 82284 clock chip.

Typically, once the data transfer command has been issued by the SAB 82288 and the data transfer has taken place, a transfer acknowledge ($\overline{XACK}$) signal is returned to the processor on the multimaster system bus to indicate "READY" from the accessed slave device. The processor remains in a series of "wait states" (repeated TC states) until the addressed device responds with $\overline{XACK}$ asserted signal to the SAB 82284's $\overline{ARDY}$ input and the SAB 82284 asserts $\overline{READY}$ to the processor. The processor then completes its bus cycle.

SAB 82289 with Other Bus Masters

When supporting other bus masters, the $\overline{S0}$/HOLD and $\overline{READY}$ pins of the bus arbiter can be connected to the "hold" pin of that master. The inverted $\overline{AEN}$ signal from the SAB 82289 can be used as the hold acknowledge (HLDA) input for the other bus master.

The bus master sends a HOLD signal to the bus arbiter when it needs the system bus for a memory access. If the arbiter currently controls the system bus, $\overline{AEN}$ will be active. Otherwise $\overline{AEN}$ will be inactive and the arbiter will request control of the system bus. The bus master will have to wait until the SAB 82289 has asserted $\overline{AEN}$ (low) before it starts its bus cycle.

When the bus master no longer requires the Multibus it will have to inactivate the HOLD signal. The arbiter interprets the Multibus access as a single bus cycle which is terminated by HOLD going inactive (low). Thus the arbiter will not release the Multibus to any other bus master during a bus access cycle.

Processor Cycle Definition

Any SAB 80286 system which gains access to the Multibus through the SAB 82289 bus arbiter uses an internal clock which is one half the frequency of the system clock (CLK) (see figure 2). Knowledge of the phase of the local bus master internal clock is required for proper SAB 82289 control of the SAB 80286 interface to Multibus. The local bus master informs the bus arbiter of its internal clock phase when it asserts the status signals. The SAB 80286's $\overline{S0}$ and $\overline{S1}$ status signals are always first asserted in phase 1 of the local bus master's internal clock.

Bus State Definition

The SAB 82289 bus arbiter has three processor bus states (see figure 3): idle (TI), status (TS), command (TC). Each bus state is two CLK cycles long. Bus state phases correspond to the internal CPU clock phases.

Figure 2
CLK Relationship to Internal Processor Phase, and Bus T-States

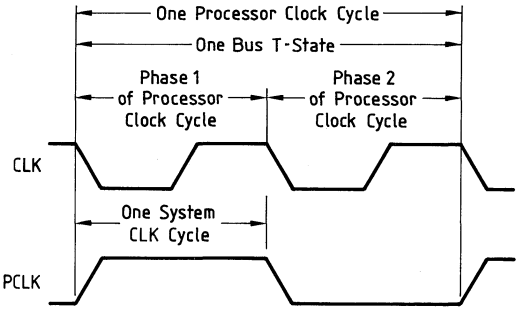
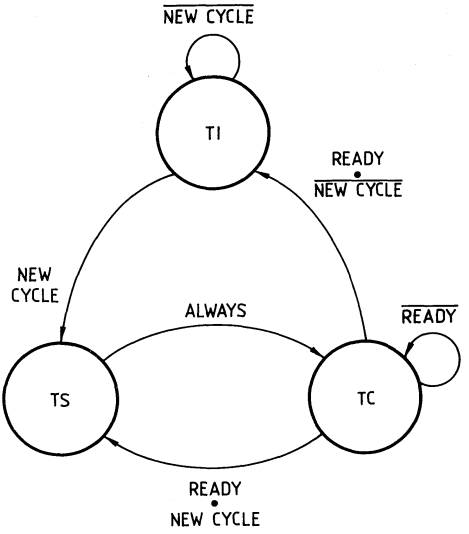


Figure 3
SAB 82289 Processor Bus States



Bus Cycle Definition

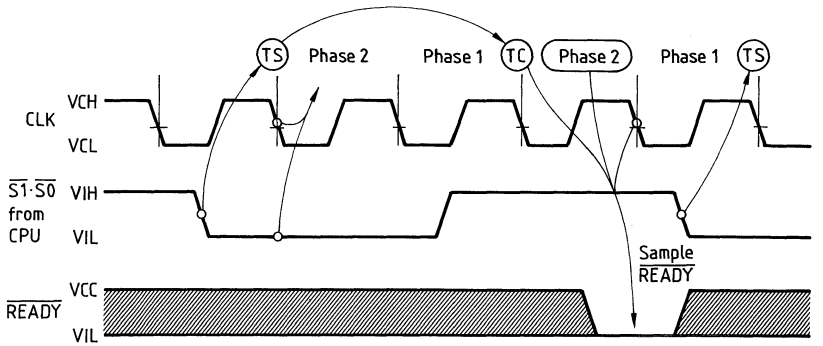
The $\overline{S1}$ and $\overline{S0}$ status inputs are sampled by the SAB 82289 on the falling edge of CLK and signal the start of a bus cycle by going active (low). The TS bus state is defined to be the two CLK cycles during which either $\overline{S1}$ or $\overline{S0}$ is active (see figure 4). When either $\overline{S1}$ or $\overline{S0}$ is sampled low, the next CLK cycle is considered the second phase of the associated processor clock cycle.

The arbiter enters the TC bus state after the TS state. The shortest bus cycle may have one TS state and one TC state. Longer bus cycles are formed by repeating TC states. A repeated TC bus state is called a wait state.

The $\overline{READY}$ input determines whether the current TC bus state is to be repeated. The $\overline{READY}$ input has the same timing and effect for all bus cycles. $\overline{READY}$ is sampled at the end of each TC bus state to see if it is active. If sampled high, the TC bus state is repeated. This is called inserting a wait state.

When $\overline{READY}$ is sampled low, the current bus cycle is terminated. Note that the bus arbiter may enter the TS bus state directly from TC if the status lines are sampled active (low) at the next falling edge of CLK (see figure 4). If neither of the status lines is sampled active at that time the SAB 82289 will enter the TI bus state. The TI bus state will be repeated until the status inputs are sampled active.

Figure 4
SAB 80286 Bus Cycle Definition (without Wait States)



Arbitration between Bus Masters

The Multibus protocol allows multiple processing elements to compete with each other to access common system resources. Since the local SAB 80286 processor does not have exclusive use of the system bus, if the Multibus is "BUSY" the SAB 80286 processor will have to wait before it can access the system bus.

The SAB 82289 bus arbiter provides an integrated solution for controlling access to a multimaster system bus. The bus arbiter allows both higher and lower priority bus masters to acquire the system bus depending on which release mode is used. In general higher priority masters obtain the bus immediately after any lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus or the proper surrender conditions exist. The SAB 82289 handles this arbitration in a manner completely transparent to the bus master (e.g. SAB 80286 processor).

At the end of each transfer, the arbiter may retain or release the system bus. This decision is controlled by the processor state, bus arbitration inputs and arbiter strapping options (see releasing the Multibus, ahead).

Priority Resolving Techniques

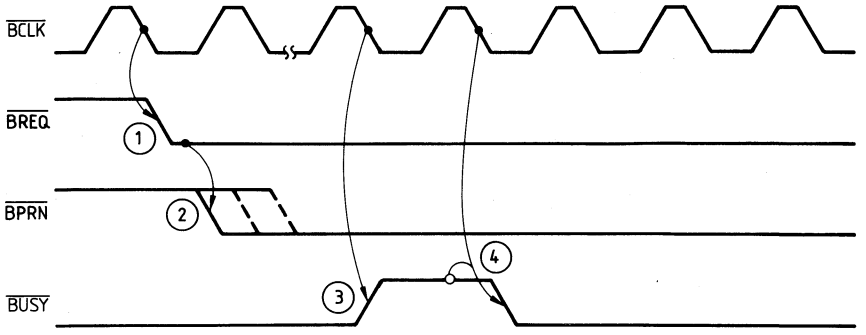
Some means of resolving priority between bus masters requesting the multimaster bus simultaneously must be provided. The SAB 82289 bus arbiter supports parallel, serial and rotating system bus priority resolving techniques. All of these techniques are based on the concept that, at a given time, one bus master will have priority above all the others.

An individual arbiter is the highest priority arbiter requesting the Multibus when its $\overline{\text{BPRN}}$ input is asserted (low). The highest priority requesting arbiter cannot immediately seize the system bus. It must wait until the present bus transaction is completed. Upon completing its current transaction the present bus owner surrenders the bus by releasing $\overline{\text{BUSY}}$.

$\overline{\text{BUSY}}$ is an active-low "wired OR" Multibus signal connecting all bus arbiters on the system bus. When $\overline{\text{BUSY}}$ goes inactive, the arbiter which has requested the system bus and presently has bus priority ($\overline{\text{BPRN}}$ low), seizes the bus by pulling $\overline{\text{BUSY}}$ low (see waveform in figure 5).

The generation of a multimaster bus request ($\overline{\text{BREQ}}$) is controlled by the type of bus cycle and the SYSB/$\overline{\text{RESB}}$ input. Whenever the processor signals the status for memory read, memory write, I/O read,

Figure 5
Bus Exchange Timing for the Multibus



(1) Higher Priority Bus Arbiter Requests the Multimaster System Bus
(2) Attains Priority. (Does not Yet Own Bus).
(3) Lower Priority Bus Arbiter Releases $\overline{\text{BUSY}}$.
(4) Higher Priority Bus Arbiter then Acquires the Bus and Pulls $\overline{\text{BUSY}}$ Low.

I/O write or interrupt acknowledge cycle, and SYSB/$\overline{\text{RESB}}$ is high at the end of TS, a bus request is generated.

When the status inputs indicate an interrupt acknowledge bus cycle, the arbiter allows external logic to decide (through the SYSB/$\overline{\text{RESB}}$ input) whether the interrupt acknowledge cycle should use the Multibus.

Figure 6 shows how SYSB/$\overline{\text{RESB}}$ is repeatedly sampled until it is sampled high or the bus cycle is terminated. If the bus cycle is completed ($\overline{\text{READY}}$ is sampled low) before SYSB/$\overline{\text{RESB}}$ is sampled high, the arbiter will not request the Multibus.

The SAB 82289 bus arbiter does not generate a separate $\overline{\text{BREQ}}$ for each bus cycle. Instead the SAB 82289 generates $\overline{\text{BREQ}}$ when it requests the bus and holds $\overline{\text{BREQ}}$ active during the time that it has possession of the bus. Note that all multimaster system bus requests (via $\overline{\text{BREQ}}$) are synchronized to the system bus clock ($\overline{\text{BCLK}}$).

Figure 6
Bus Request Timing During an Interrupt Acknowledge Cycle

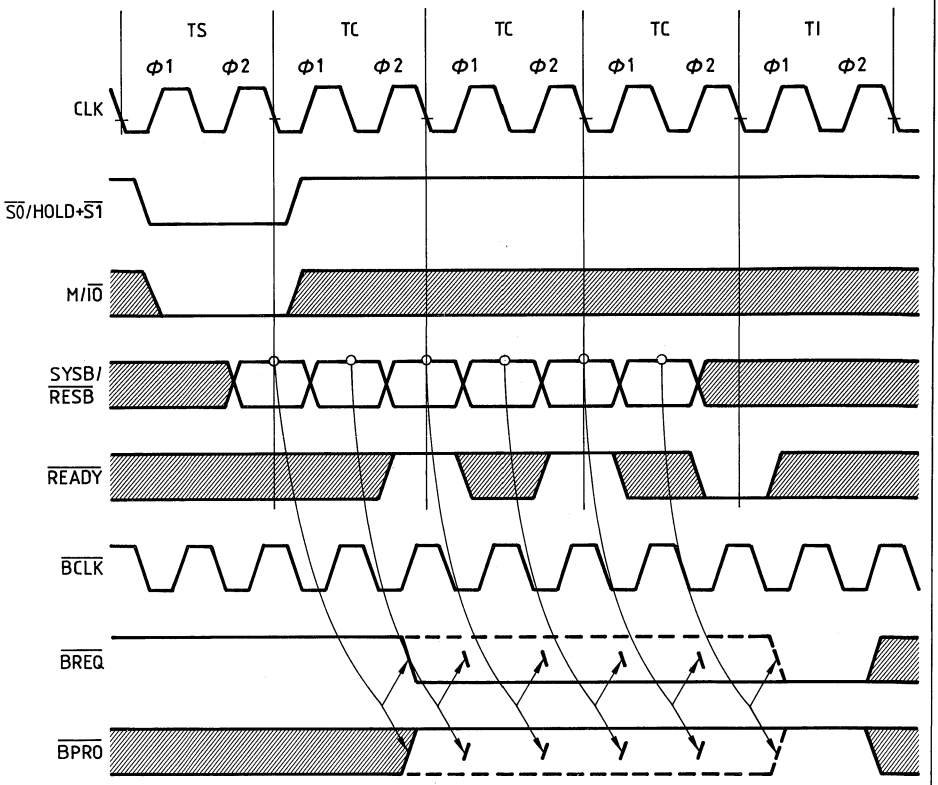


Figure 7
Parallel Priority Resolving Technique

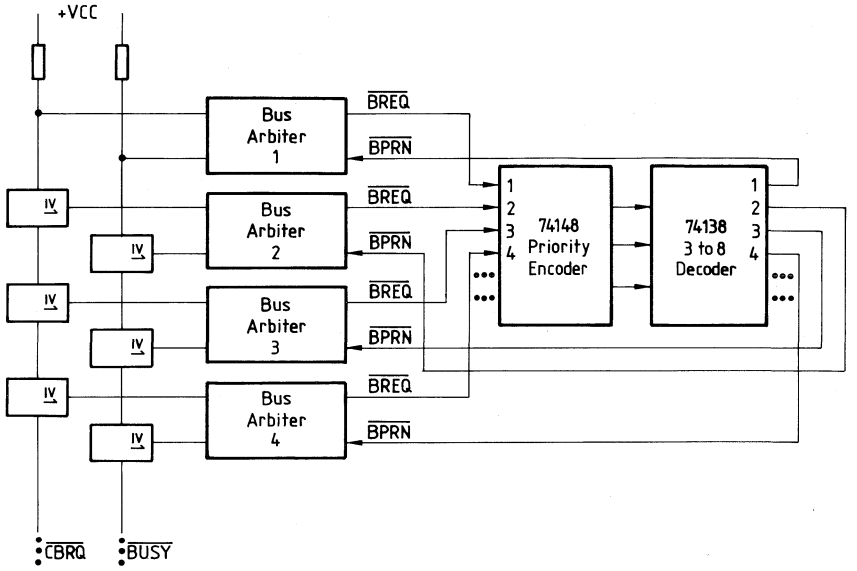
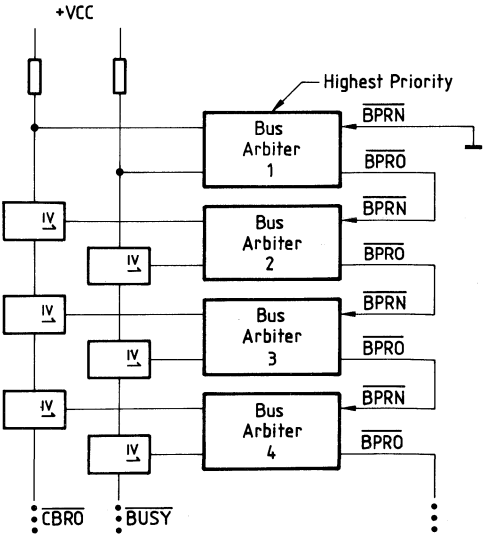


Figure 8
Connections for Serial Priority Resolving Technique



Parallel Priority Resolving Technique

The parallel priority resolving technique requires a separate bus request line ($\overline{BREQ}$) for each arbiter on the multimaster system bus (see figure 7). Each $\overline{BREQ}$ line enters a priority encoder which generates the binary address of the highest priority $\overline{BREQ}$ line currently active. The binary address is decoded to select the $\overline{BPRN}$ line corresponding to the highest priority arbiter requesting the bus. In a parallel scheme, the $\overline{BPRO}$ output is not used.

The arbiter receiving priority ($\overline{BPRN}$ low) then allows its associated bus master onto the multimaster system bus as soon as the bus becomes available (i.e. the bus is no longer busy). Any number of bus masters may be accommodated in this way, limited only by the complexity of the external priority resolving circuitry. Such circuitry must resolve the priority within one $\overline{BCLK}$ period.

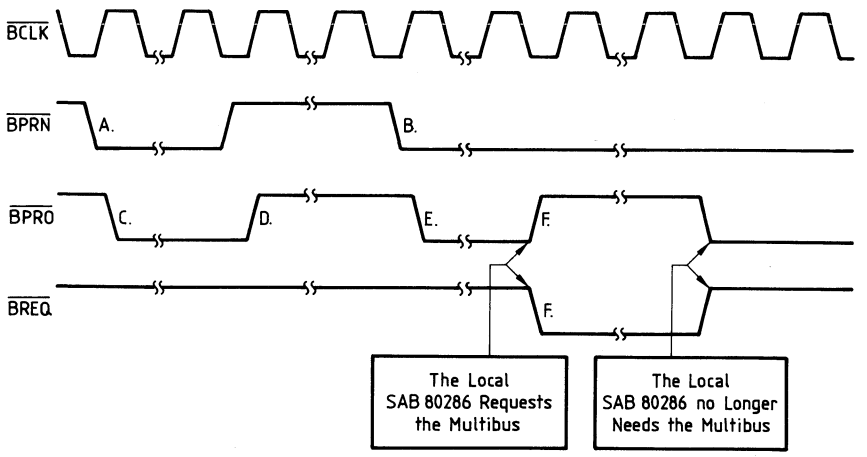
Serial Priority Resolving Technique

The serial priority resolving technique eliminates the need for the priority circuitry of the parallel technique by daisy-chaining the bus arbiters together, that is, connecting the higher priority arbiter's $\overline{BPRO}$ output to the $\overline{BPRN}$ of the next lower priority arbiter (see figure 8). The highest priority bus arbiter would have its $\overline{BPRN}$ tied low in this configuration, signifying to the arbiter that it always has the highest priority when requesting the system bus. In a serial scheme, the $\overline{BREQ}$ output is not used.

Since arbitration must be resolved within one $\overline{BCLK}$ period the number of arbiters connected together in the serial priority is limited by the arbiter's $\overline{BPRN}$ to $\overline{BPRO}$ propagation delay (18ns). For a 10 MHz Multibus $\overline{BCLK}$, five SAB 82289 bus arbiters may be connected in serial configuration.

$$\text{Maximum number of chained-priority devices} = \frac{\overline{BCLK}\text{ period}}{\overline{BPRN}\text{ to }\overline{BPRO}\text{ delay}}$$

Figure 9
Serial Priority Bus Behavior



Note: Events A through F described in the following

When using the serial priority resolving scheme, a higher priority arbiter (for example, arbiter 2, figure 8) passes priority to the next lower priority arbiter (arbiter 3) by asserting its $\overline{\text{BPRO}}$ signal (low). This asserts $\overline{\text{BPRN}}$ of next arbiter (arbiter 3) as shown in figure 9 event A and event B. An arbiter's $\overline{\text{BPRO}}$ is asserted if the arbiter has priority ($\overline{\text{BPRN}}$ is asserted) but is not accessing or requesting the system bus (as indicated by $\overline{\text{BREQ}}$ inactive as shown in figure 9 event C and event E for arbiter 3). Whenever a higher priority arbiter (arbiter 3) issues a bus request its $\overline{\text{BPRO}}$ goes inactive causing the next lower priority arbiter (arbiter 4) to lose its bus priority (figure 9 event F). Any arbiter (arbiter 3) will also bring its $\overline{\text{BPRO}}$ inactive if its $\overline{\text{BPRN}}$ goes inactive (from arbiter 2), thereby passing the loss of bus priority on to the lower priority arbiters (e.g. arbiter 4) as shown in figure 9 event D.

Rotating Priority Resolving Technique

The rotating priority resolving technique is similar to the parallel priority resolving technique except that priority is dynamically re-assigned. The priority encoder is replaced by a more complex circuitry which rotates priority between requesting arbiters, thus allowing each arbiter an equal chance to use the multimaster system bus over a given period of time.

Selecting the Appropriate Priority Resolving Technique

The choice of a priority resolving technique involves a trade-off between external logic complexity and ease of Multibus access for the different bus masters in the system. The rotating priority resolving technique requires a substantial amount of external logic, but guarantees all the bus masters an equal opportunity to access the system bus. The serial priority resolving technique uses no external logic but has fixed bus master priority levels and can accomodate only a limited number of bus arbiters.

The parallel priority resolving technique is in general a compromise between the other two techniques (for example parallel priority configuration in figure 7 allows up to eight arbiters to be present on the Multibus, with fixed priority levels, while not requiring a large amount of complex external logic to implement).

Releasing the Multibus

Following a data transfer cycle on the Multibus, the SAB 82289 bus arbiter can either retain control of the system bus or release the bus for use by some other bus master. The SAB 82289 can operate in one of three modes, defining different conditions under which the arbiter relinquishes control of the multimaster system bus. These release modes are described in the table below.

If the arbiter was programmed to operate in Always Release Mode (mode 1) during the previous reset, it will surrender the Multibus after each complete transfer cycle. If the arbiter is not in Always Release Mode, it will not surrender the bus until the local SAB 80286 processor enters a halt state, the arbiter is forced off the bus by the loss of $\overline{\text{BPRN}}$ (mode 2 or 3), or by a common bus request when the $\overline{\text{CBRQ}}$ input is enabled by the $\overline{\text{CBQLCK}}$ input (mode 2).

$\overline{\text{CBRQ}}$ can save the bus exchange overhead in many cases. If $\overline{\text{CBRQ}}$ is high, it indicates to the bus master that no other master is requesting the bus and therefore the present bus master can retain the bus. Without $\overline{\text{CBRQ}}$, only $\overline{\text{BPRN}}$ indicates whether or not another master is requesting the bus and that only if the other master is of higher priority. Between its bus transfer cycles the master must give up the bus in order to allow lower priority masters to take the bus if they need it. At the start of the master's next transfer cycle, the bus must be regained. If no other master has the bus, this can take approximately two $\overline{\text{BCLK}}$ periods. To avoid this overhead of unnecessarily giving up and regaining the bus when no other masters needs it, $\overline{\text{CBRQ}}$ is

SAB 82289 Release Modes

Release Mode	Conditions under which the bus arbiter releases the system bus (unless cycles are LOCKed)
Mode 1	The bus arbiter always releases the bus at the end of each transfer cycle
Mode 2	The bus arbiter ratains the bus until: • a higher-priority bus master requests the bus, driving $\overline{\text{BPRN}}$ high • a lower-priority bus master requests the bus by pulling $\overline{\text{CBRQ}}$ low
Mode 3	The bus arbiter retains the bus until: • a higher-priority bus master requests the bus, driving $\overline{\text{BPRN}}$ high ($\overline{\text{CBRQ}}$ low ignored)

extremely useful. Any master that wants but does not have the bus, must assert $\overline{CBRQ}$ (low). If $\overline{CBRQ}$ line is not asserted the bus does not have to be released, thereby eliminating the delay of regaining the bus at the start of the next cycle.

The $\overline{LOCK}$ input to the arbiter can be used to override any of the conditions shown in the table before. While $\overline{LOCK}$ is asserted, the arbiter will not surrender control of the Multibus to any other requesting arbiter. Note that the arbiter will surrender the Multibus (synchronous to $\overline{BCLK}$) either in response to RESET or $\overline{INIT}$ signals independent of the current release mode or the state of the arbiter inputs.

The three bus release modes have the same operation when supporting either the SAB 80286 processor or some other bus master.

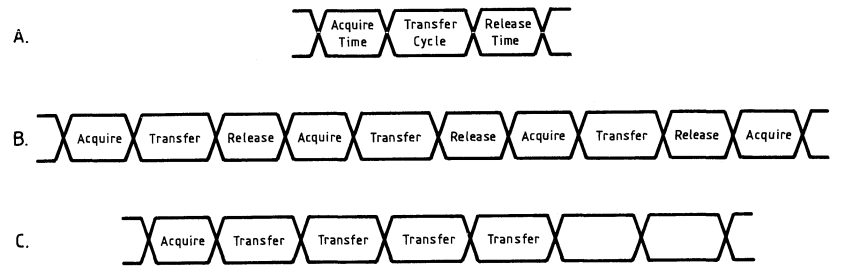
Selecting the Appropriate Release Mode

The choice of which release mode to use may affect the bus utilization of the individual subsystems, and the system as a whole. Mode-dependent performance variations are due to the bus acquisition/release overhead. The effect of these acquire and release times on system bus efficiency is illustrated in figure 10.

An isolated transfer on the multimaster system bus is depicted in figure 10-A. Figure 10-B shows utilization for the bus arbiter operation in mode 1. The arbiter must request and release the system bus for each transfer cycle. Lower priority arbiters have easy access to the system bus, but overall bus efficiency is low. Bus utilization for a bus arbiter operating in mode 2 or 3 is shown in the figure 10-C. In this situation the arbiter acquires the bus once for a sequence of transfers. The arbiter retains the bus until forced off by another bus master's request as defined in table before.

The three release modes of the SAB 82289 allow the designer to optimize the system use of the Multibus.

Figure 10
Effects of Bus Contention on Bus Efficiency



Configuring the SAB 82289 Release Mode

The SAB 82289 bus arbiter can be configured in any of its three bus release modes without additional hardware. It can also be configured to switch between mode 2 and mode 3 under software control of the SAB 80286 processor, requiring that a parallel port or addressable latch be used to drive the $\overline{\text{ALWAYS}}/\overline{\text{CBQLCK}}$ input pin of the SAB 82289 (see figure below).

Figure 11
SAB 82289 Release Mode Configurations

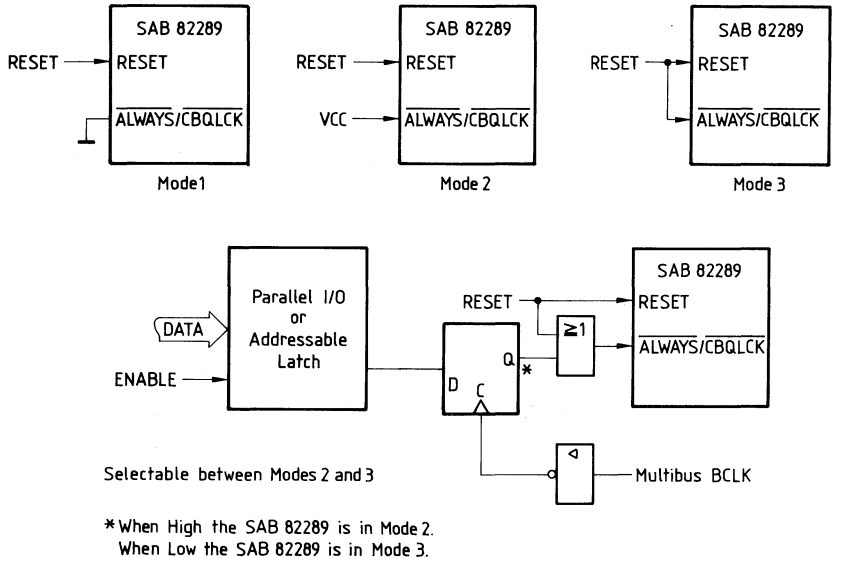
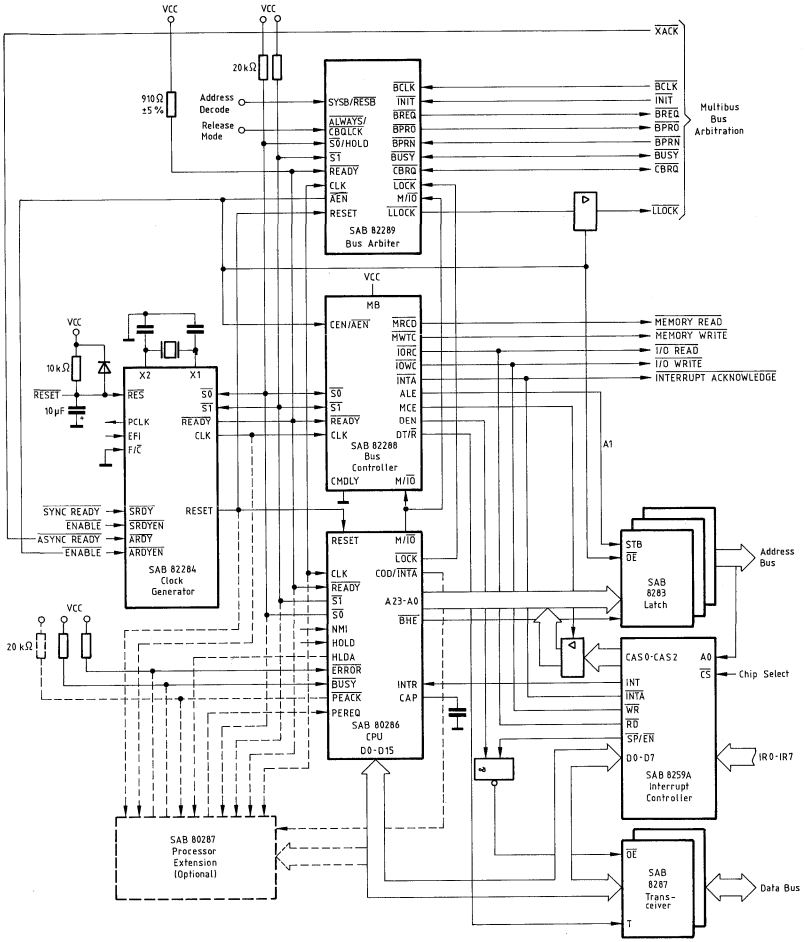


Figure 12
Typical SAB 80286 Subsystem Multibus Interface



Asserting the $\overline{\text{LOCK}}$ Signal

Independent of the particular release mode of the SAB 82289 bus arbiter, the SAB 80286 processor can assert a $\overline{\text{LOCK}}$ signal synchronously to CLK to prevent the arbiter from releasing the Multibus. This software-controlled $\overline{\text{LOCK}}$ signal prevents the SAB 82289 from surrendering the system bus to any other bus master, whether that bus master is of higher or lower priority. The $\overline{\text{LOCK}}$ signal is typically used for implementing software semaphores for shared resources or for critical processes that must run in real-time.

The SAB 82289 $\overline{\text{LLOCK}}$ output is the Multibus timing-compatible signal asserted during all bus cycles which are locked together. The $\overline{\text{LLOCK}}$ is set or reset depending on processor $\overline{\text{LOCK}}$ at the end of the TS cycle. $\overline{\text{LLOCK}}$ will delay going inactive until the termination of the current transfer cycle.

The SAB 82289 will continue to assert the $\overline{\text{LLOCK}}$ signal retaining control of the Multibus until the end of the first "unLOCKed" SAB 80286 bus cycle (SAB 80286 disables its $\overline{\text{LOCK}}$ output on the last bus cycle indicating that no future locked cycles are needed). While the $\overline{\text{LOCK}}$ signal will force the arbiter presently in control to hold the system bus, it cannot force another arbiter to surrender the bus any earlier than it normally would.

The $\overline{\text{LLOCK}}$ signal from the SAB 82289 must be connected to a tri-state buffer in order to drive the Multibus $\overline{\text{LOCK}}$ signal. This tri-state buffer should be enabled by the $\overline{\text{AEN}}$ signal from the arbiter going active.

SAB 82289 Reset and Initialization

The SAB 82289 bus arbiter provides the RESET and $\overline{\text{INIT}}$ pins for initialization. RESET is a CLK synchronous signal from the SAB 82284 clock generator and $\overline{\text{INIT}}$ is an asynchronous signal on the multimaster system bus. By having RESET pin high or $\overline{\text{INIT}}$ pin low the $\overline{\text{BREQ}}$, $\overline{\text{BUSY}}$ and $\overline{\text{AEN}}$ output pins will all become inactive. RESET will also deactivate the $\overline{\text{LLOCK}}$ signal. Unlike RESET, $\overline{\text{INIT}}$ will not clear any pending bus request, the bus request would be asserted after the $\overline{\text{INIT}}$ signal goes inactive.

Note that when the SAB 82289 is initialized by the RESET input it does not wait until the end of the current bus cycle to reset. Any bus cycle in process when RESET goes active will be aborted by the arbiter. Although the $\overline{\text{INIT}}$ signal will also interrupt an active bus cycle, the arbiter can request the Multibus and complete the bus cycle when $\overline{\text{INIT}}$ goes inactive.

As mentioned in the pin description and figure 11 the functions of the $\overline{\text{S0}}$/HOLD pin and the release mode ($\overline{\text{ALWAYS}}$/$\overline{\text{CBQLCK}}$ pin) are programmed at the falling edge of RESET.

Absolute Maximum Ratings [1)]

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin With Respect to GND	−0.5 to +7V
Power Dissipation	1 W

DC Characteristics

TA = 0 to 70°C, VCC = 5V ±5%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
VIL	Input low Voltage	−0.5	0.8	V	–
VIH	Input High Voltage	2.0	VCC+0.5	V	–
VILC	CLK Input Low Voltage	−0.5	0.6	V	–
VIHC	CLK Input High Voltage	3.8	VCC+1.0	V	–
VOL	Output Low Voltage: $\overline{BUSY}$, $\overline{CBRQ}$ $\overline{BPRO}$, $\overline{BREQ}$, $\overline{AEN}$ $\overline{LLOCK}$	–	0.45	V	 IOL = 32mA IOL = 16 mA IOL = 5mA
VOH	Output High Voltage	2.4	–	V	IOH = 400 µA
ILI	Input Leakage Current	–	±10 ±1	µA mA	0.45 V ≤VIN ≤VCC 0 V ≤VIN <0.45 V
iLO	Output Leakage Current	–	±10	µA	0.45 V ≤VOUT ≤VCC
ICC	Power Supply Current	–	120	mA	–
CCLK	CLK, $\overline{BCLK}$ Input Capacitance	–	12	pF	fC = 1 MHz
CIN	Input Capacitance	–	10	pF	fC = 1 MHz
CIO	Input/Output Capacitance	–	20	pF	fC = 1 MHz

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics SAB 82289

TA = 0 to 70°C, VCC = 5V ±5%
AC timings are referenced to 0.8 and 2.0 V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	Limit values * 8 MHz		Unit	Test condition	Shown in Figure
		min.	max.			
1	CLK Cycle Period	62	t5+50	ns	–	13
2	CLK Low Time	15	230	ns	at 1.0 V	13
3	CLK High Time	20	235	ns	at 3.6V	13
4	CLK Rise/Fall Time	–	10	ns	1.0 to 3.6V	13
5	$\overline{\text{BCLK}}$ Cycle Time	100	∞	ns	–	13
6	$\overline{\text{BCLK}}$ High/Low Time	30	–	ns	–	13
7	$\overline{\text{S0}}$/HOLD, $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ Setup	22	–	ns	–	13, 22
8	$\overline{\text{S0}}$/HOLD, $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ Hold	1	–	ns	–	13, 22
9	$\overline{\text{READY}}$ Setup	38	–	ns	–	13
10	$\overline{\text{READY}}$ Hold Time	25	–	ns	–	13
11	$\overline{\text{LOCK}}$, SYSB/$\overline{\text{RESB}}$ Setup Time	20	–	ns	–	13, 18
12	$\overline{\text{LOCK}}$, SYSB/$\overline{\text{RESB}}$ Hold Time	1	–	ns	–	13, 18
13	RESET Setup Time	20	–	ns	–	19
14	RESET Hold Time	1	–	ns	–	19
15	RESET Active Pulse Width	16	–	CLKs	–	19
16	$\overline{\text{INIT}}$ Setup Time	45	–	ns	9)	20
17	$\overline{\text{INIT}}$ Hold Time	1	–	ns	9)	20
18	$\overline{\text{INIT}}$ Active Pulse Width	3 (t1) +3(t14)	–	ns	–	20
19	$\overline{\text{BUSY}}$, $\overline{\text{BPRN}}$, $\overline{\text{CBRQ}}$, $\overline{\text{CBQLCK}}$/$\overline{\text{ALWAYS}}$ Setup to $\overline{\text{BCLK}}$ (or to RESET)	20	–	ns	–	13, 15, 21, 22
20	$\overline{\text{BUSY}}$, $\overline{\text{BPRN}}$, $\overline{\text{CBRQ}}$, $\overline{\text{CBQLCK}}$/$\overline{\text{ALWAYS}}$ Hold to $\overline{\text{BCLK}}$ (or to RESET)	1	–	ns	–	13, 15, 21, 22
21	$\overline{\text{BCLK}}$ to $\overline{\text{BREQ}}$ Delay	–	30	ns	1)	13,14,22
22	$\overline{\text{BCLK}}$ to $\overline{\text{BPRO}}$ Delay	–	35	ns	2)	17
23	$\overline{\text{BPRN}}$ to $\overline{\text{BPRO}}$ Delay	–	25	ns	2)	17
24	$\overline{\text{BCLK}}$ to $\overline{\text{BUSY}}$ Active Delay	1	60	ns	3)	13, 22

For notes see next page.

AC Characteristics SAB 82289 (continued)

Symbol	Parameter	Limit values * 8 MHz		Unit	Test condition	Shown in Figure
		min.	max.			
25	$\overline{BCLK}$ to $\overline{BUSY}$ Float Delay	–	35	ns	4)	13, 14
26	$\overline{BCLK}$ to $\overline{CBRQ}$ Active Delay	–	55	ns	5)	13, 22
27	$\overline{BCLK}$ to $\overline{CBRQ}$ Float Delay	–	35	ns	4)	13,20,22
28	$\overline{BCLK}$ to $\overline{AEN}$ Active Delay	1	25	ns	6)	13
29	CLK to $\overline{AEN}$ Inactive Delay	3	25	ns	6)	13, 14
30	CLK to $\overline{LLOCK}$ Delay	–	20	ns	7)	18
31	RESET to $\overline{LLOCK}$ Delay	–	35	ns	7)	19
32	CLK to $\overline{BCLK}$ Setup Time	38	–	ns	8)	13,16,20
33	$\overline{BCLK}$ to $\overline{AEN}$ Output Delay	1	30	ns	6)	22

*) Preliminary

1) $\overline{BREQ}$ load CL = 60 pF

2) $\overline{BPRO}$ load CL = 60 pF

3) $\overline{BUSY}$ load CL = 300 pF

4) Float condition occurs when output current is less than ILO in magnitude

5) $\overline{CBRQ}$ load CL = 300 pF

6) $\overline{AEN}$ load CL = 150 pF

7) $\overline{LLOCK}$ load CL = 60 pF

8) In actual use, CLK and $\overline{BCLK}$ are usually asynchronous to each other. However, for component testing purposes this specification is required to assure signal recognition at specific CLK and $\overline{BCLK}$ edges.

9) $\overline{INIT}$ is asynchronous to CLK and to $\overline{BCLK}$. However, for component testing purposes, this specification is required to assure signal recognition at specific CLK and $\overline{BCLK}$ edges.

AC Characteristics SAB 82289-6

TA = 0 to 70°C, VCC = 5V ±5%
AC timings are referenced to 0.8 and 2.0 V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	Limit values * 6 MHz		Unit	Test condition	Shown in Figure
		min.	max.			
1	CLK Cycle Period	83	t5+50	ns	–	13
2	CLK Low Time	20	225	ns	at 1.0 V	13
3	CLK High Time	25	230	ns	at 3.6 V	13
4	CLK Rise/Fall Time	–	10	ns	1.0 to 3.6 V	13
5	$\overline{\text{BCLK}}$ Cycle Time	100	∞	ns	–	13
6	$\overline{\text{BCLK}}$ High/Low Time	30	–	ns	–	13
7	$\overline{\text{S0}}$/HOLD, $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ Setup	28	–	ns	–	13, 22
8	$\overline{\text{S0}}$/HOLD, $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ Hold	1	–	ns	–	13, 22
9	$\overline{\text{READY}}$ Setup	50	–	ns	–	13
10	$\overline{\text{READY}}$ Hold Time	35	–	ns	–	13
11	$\overline{\text{LOCK}}$, SYSB/$\overline{\text{RESB}}$ Setup Time	28	–	ns	–	13, 18
12	$\overline{\text{LOCK}}$, SYSB/$\overline{\text{RESB}}$ Hold Time	1	–	ns	–	13, 18
13	RESET Setup Time	28	–	ns	–	19
14	RESET Hold Time	1	–	ns	–	19
15	RESET Active Pulse Width	16	–	CLKs	–	19
16	$\overline{\text{INIT}}$ Setup Time	45	–	ns	9)	20
17	$\overline{\text{INIT}}$ Hold Time	1	–	ns	9)	20
18	$\overline{\text{INIT}}$ Active Pulse Width	3 (t1) +3(t14)	–	ns	–	20
19	$\overline{\text{BUSY}}$, $\overline{\text{BPRN}}$, $\overline{\text{CBRQ}}$, $\overline{\text{CBQLCK}}$/$\overline{\text{ALWAYS}}$ Setup to $\overline{\text{BCLK}}$ (or to RESET)	20	–	ns	–	13, 15, 21, 22
20	$\overline{\text{BUSY}}$, $\overline{\text{BPRN}}$ $\overline{\text{CBRQ}}$, $\overline{\text{CBQLCK}}$/$\overline{\text{ALWAYS}}$ Hold to $\overline{\text{BCLK}}$ (or to RESET)	1	–	ns	–	13, 15, 21, 22
21	$\overline{\text{BCLK}}$ to $\overline{\text{BREQ}}$ Delay	–	30	ns	1)	13,14,22
22	$\overline{\text{BCLK}}$ to $\overline{\text{BPRO}}$ Delay	–	35	ns	2)	17
23	$\overline{\text{BPRN}}$ to $\overline{\text{BPRO}}$ Delay	–	25	ns	2)	17
24	$\overline{\text{BCLK}}$ to $\overline{\text{BUSY}}$ Active Delay	1	60	ns	3)	13, 22

For notes see next page.

AC Characteristics SAB 82289-6 (continued)

Symbol	Parameter	Limit values * 6 MHz		Unit	Test condition	Shown in Figure
		min.	max.			
25	$\overline{\text{BCLK}}$ to $\overline{\text{BUSY}}$ Float Delay	–	35	ns	4)	13, 14
26	$\overline{\text{BCLK}}$ to $\overline{\text{CBRQ}}$ Active Delay	–	55	ns	5)	13, 22
27	$\overline{\text{BCLK}}$ to $\overline{\text{CBRQ}}$ Float Delay	–	35	ns	4)	13,20,22
28	$\overline{\text{BCLK}}$ to $\overline{\text{AEN}}$ Active Delay	1	25	ns	6)	13
29	CLK to $\overline{\text{AEN}}$ Inactive Delay	3	25	ns	6)	13, 14
30	CLK to $\overline{\text{LLOCK}}$ Delay	–	20	ns	7)	18
31	RESET to $\overline{\text{LLOCK}}$ Delay	–	35	ns	7)	19
32	CLK to $\overline{\text{BCLK}}$ Setup Time	38	–	ns	8)	13,16,20
33	$\overline{\text{BCLK}}$ to $\overline{\text{AEN}}$ Output Delay	1	30	ns	6)	22

*) Preliminary

1) $\overline{\text{BREQ}}$ load CL = 60 pF

2) $\overline{\text{BPRO}}$ load CL = 60 pF

3) $\overline{\text{BUSY}}$ load CL = 300 pF

4) Float condition occurs when output current is less than ILO in magnitude

5) $\overline{\text{CBRQ}}$ load CL = 300 pF

6) $\overline{\text{AEN}}$ load CL = 150 pF

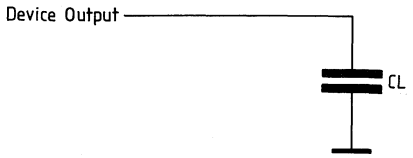
7) $\overline{\text{LLOCK}}$ load CL = 60 pF

8) In actual use, CLK and $\overline{\text{BCLK}}$ are usually asynchronous to each other. However, for component testing purposes this specification is required to assure signal recognition at specific CLK and $\overline{\text{BCLK}}$ edges.

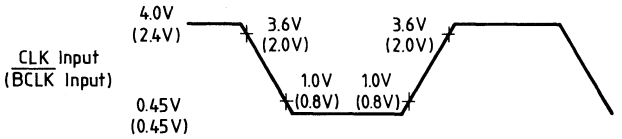
9) $\overline{\text{INIT}}$ is asynchronous to CLK and to $\overline{\text{BCLK}}$. However, for component testing purposes, this specification is required to assure signal recognition at specific CLK and $\overline{\text{BCLK}}$ edges.

AC Testing Waveforms

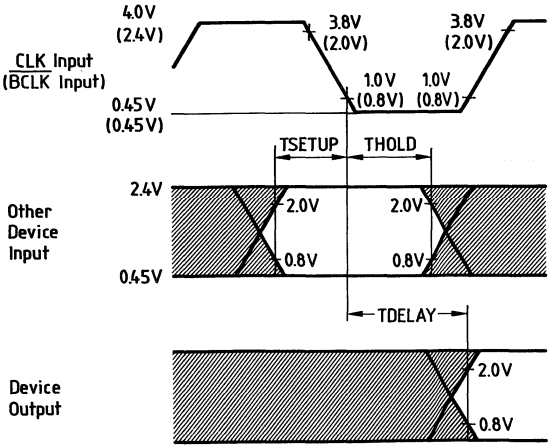
Test Loading on Outputs



Drive and Measurement Points – CLK Input ($\overline{\text{BCLK}}$ Input)



Setup, Hold and Delay Time Measurement – General



Waveforms

The waveforms (figures 13 to 21) show the timing relationships of the inputs and the outputs and do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown via the general cases. Special cases are shown when needed.

To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

The SAB 82289 bus arbiter serves as an interface between the SAB 80286 subsystem which operates synchronously to the CLK signal and Multibus which operates synchronously to $\overline{\text{BCLK}}$ signal. CLK and $\overline{\text{BCLK}}$ generally operate asynchronously to each other and at different frequencies. Thus, the exact clock period in which an input synchronous to one clock will cause a response synchronous to the other clock depends on the relative phase and frequency of CLK and $\overline{\text{BCLK}}$ at the time the input is sensed.

One strict relation between CLK and $\overline{\text{BCLK}}$ must be maintained for proper Multibus arbitration. If the CLK period is too long relative to $\overline{\text{BCLK}}$ period (t1 greater than t5 +50 ns), another arbiter could gain control of the system bus before this arbiter has released $\overline{\text{AEN}}$ synchronously to its CLK. This situation arises since the release of $\overline{\text{AEN}}$ is synchronous to the next falling CLK edge after the processor cycle ends but the release of $\overline{\text{BREQ}}$ and $\overline{\text{BUSY}}$ is synchronous to the next falling $\overline{\text{BCLK}}$ edge after the processor cycle ends. In practice, any CLK frequency greater than 6.66 MHz (i.e. SAB 80286 processor speeds greater than 3.33 MHz) will avoid conflict with a 10 MHz $\overline{\text{BCLK}}$. Therefore all SAB 80286 speed selections are Multibus compatible.

Figure 13
Multibus Acquisition and Always-Release Operation

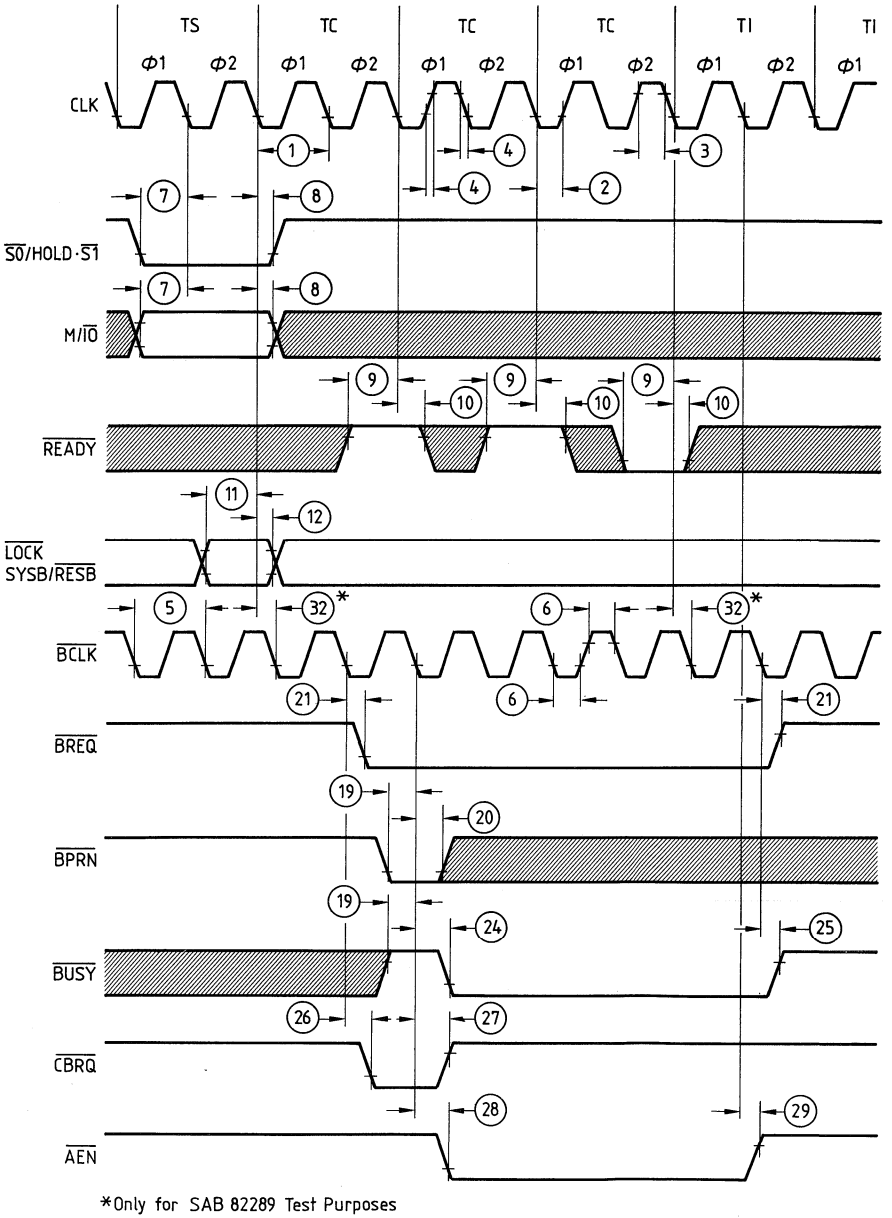
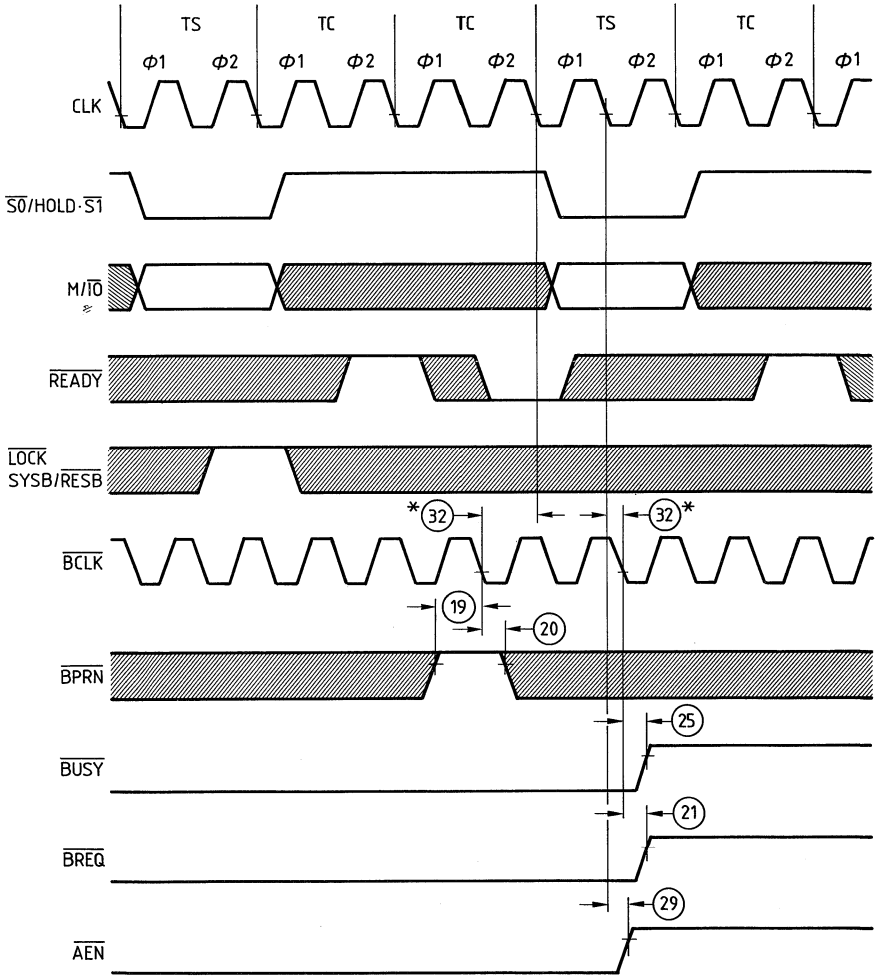


Figure 14
Multibus Release due to $\overline{\text{BPRN}}$ Inactive



*Only for SAB 82289 Test Purposes

Figure 15
Multibus Release due to $\overline{\text{CBRQ}}$ Active

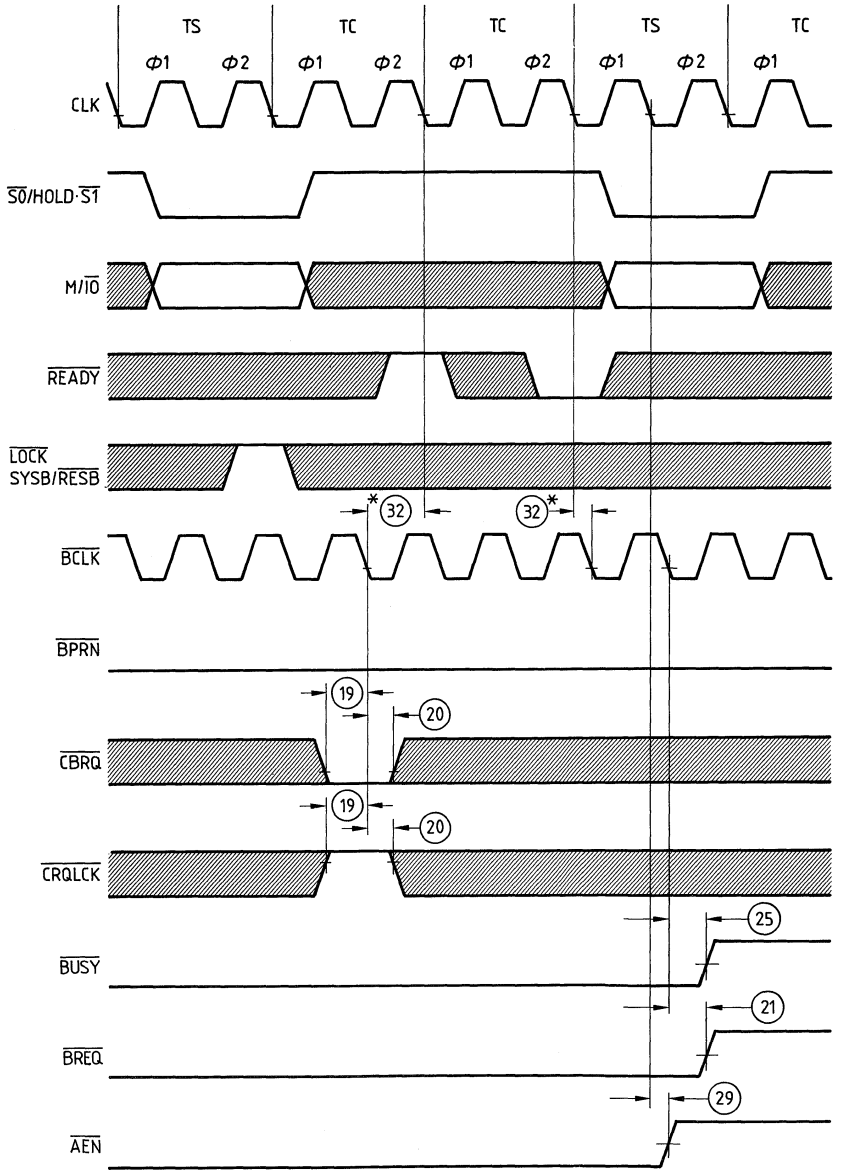
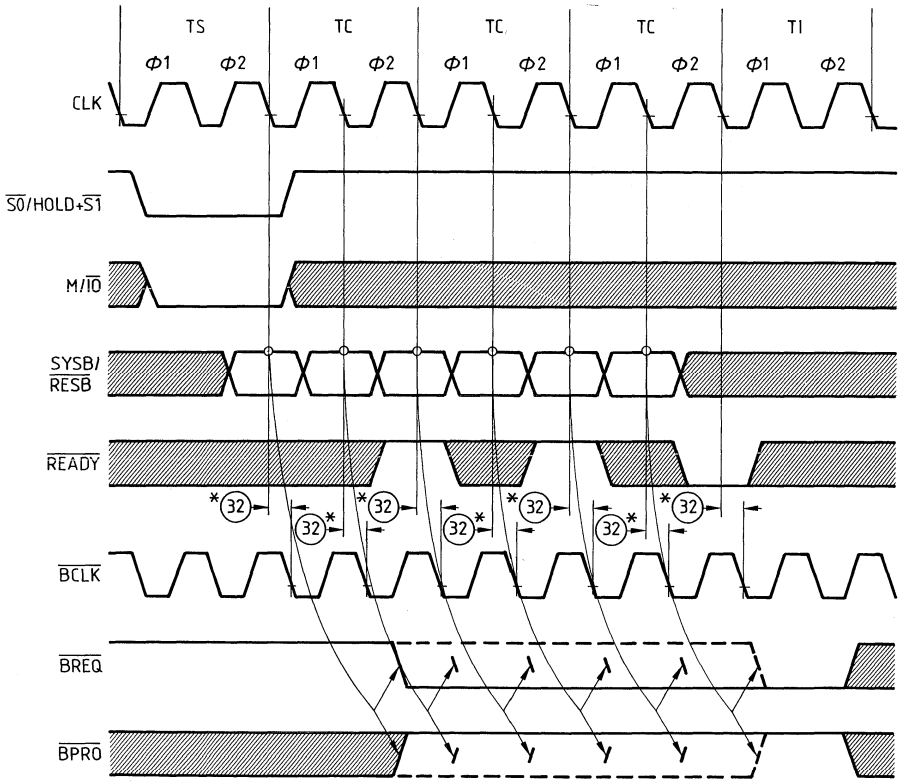


Figure 16
Multibus Acquisition during SAB 80286 INTA Cycles



*Only for SAB 82289 test purposes

Figure 17
$\overline{\text{BPRN}}$ to $\overline{\text{BPRO}}$ Timing Relationship

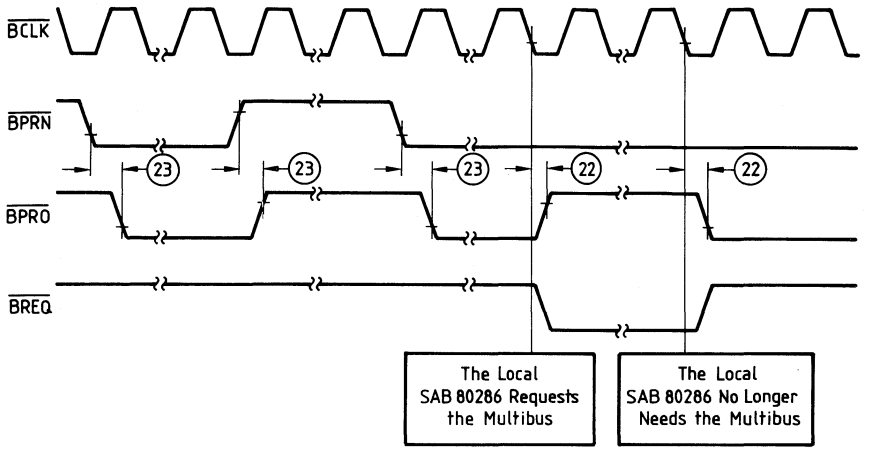


Figure 18
SAB 80286 $\overline{\text{LOCK}}$ and SAB 82289 $\overline{\text{LLOCK}}$ Relationship

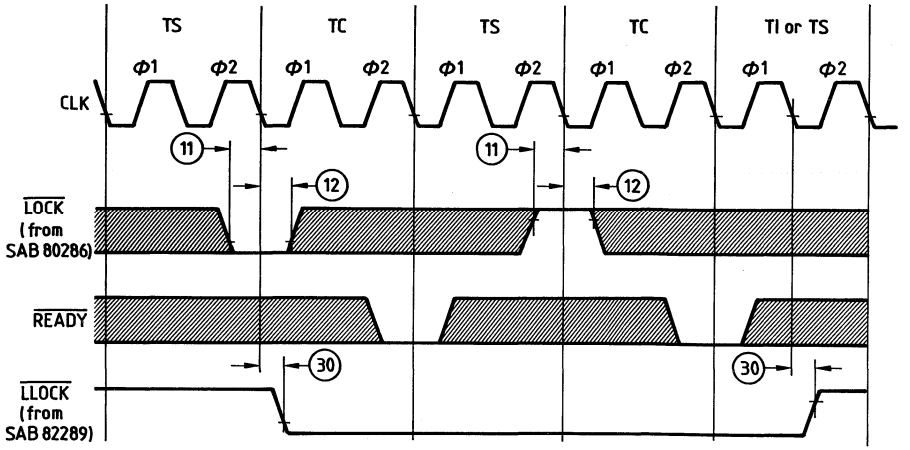
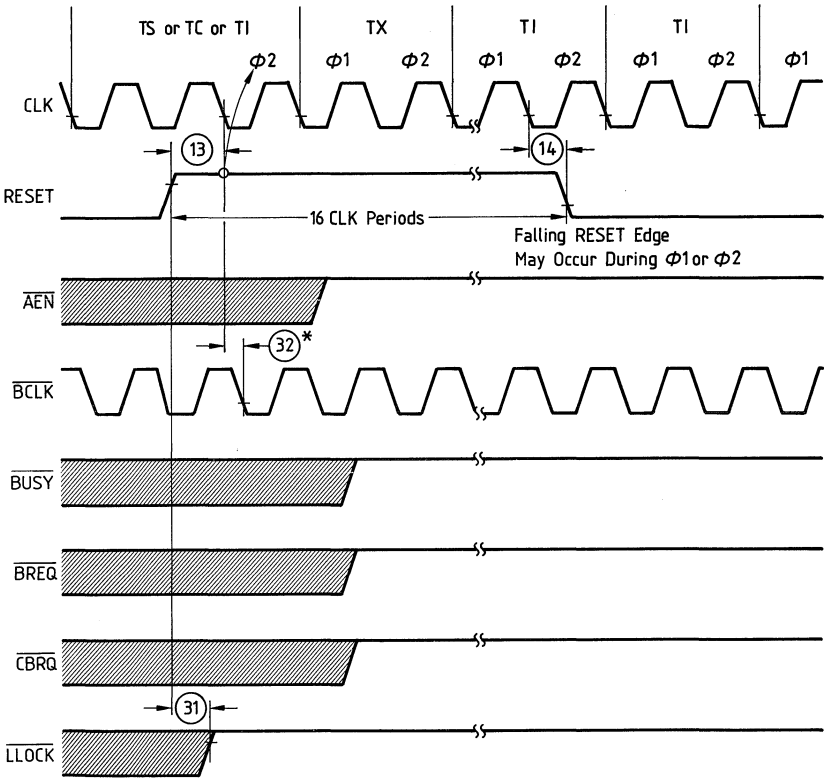
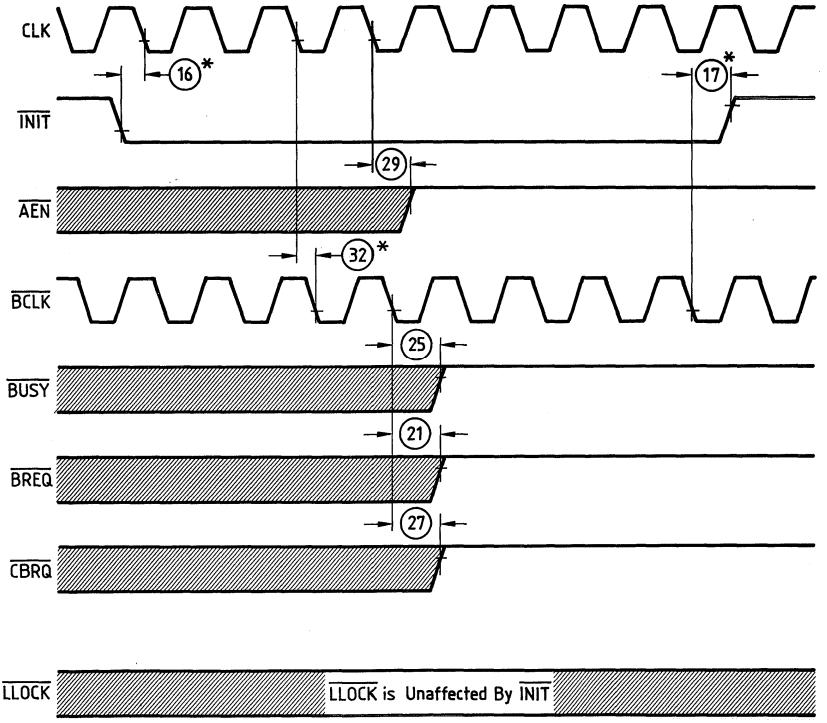


Figure 19
RESET Active Pulse



*For SAB 82289 Test Purposes Only.

Figure 20
$\overline{\text{INIT}}$ Active Pulse



*For SAB 82289 Test Purposes Only.

Figure 21
Programming the Always-Release/Common-Bus-Request-Release Option

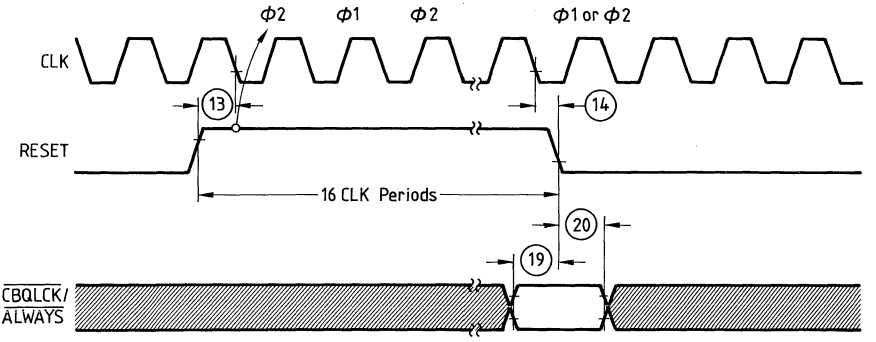
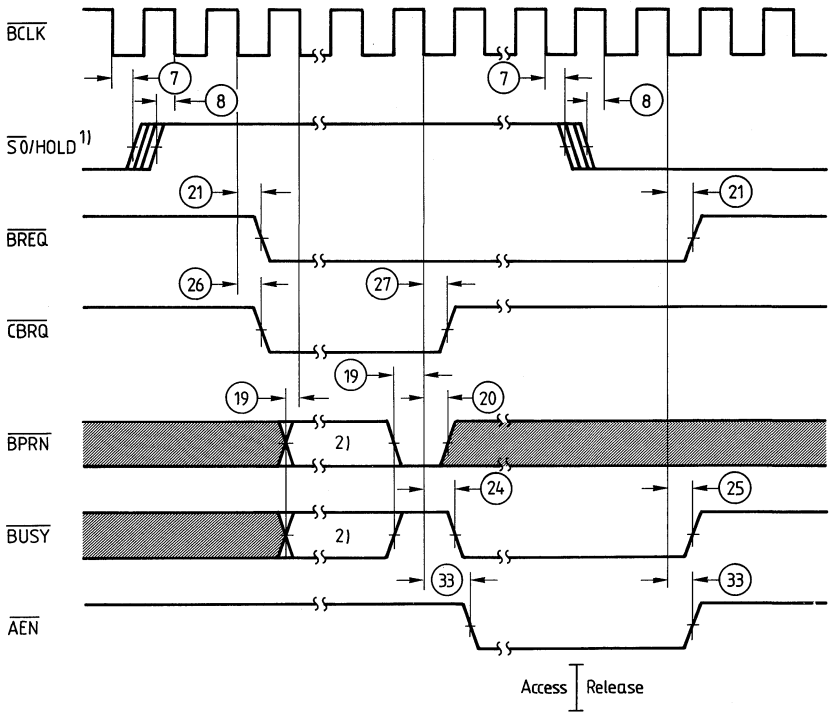


Figure 22
Multibus Arbitration Activated by HOLD Input

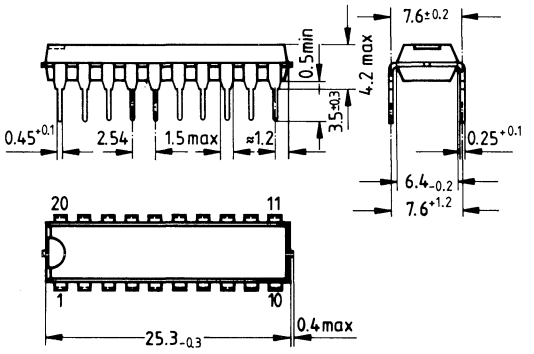


1) Used as HOLD input

2) Valid conditions are $\overline{\text{BPRN}}$ high or $\overline{\text{BUSY}}$ low. If one of the two conditions is fulfilled, the level of the other signal ($\overline{\text{BUSY}}$ or $\overline{\text{BPRN}}$) may be arbitrary

Package Outlines

20 Pin Plastic Package – Type P-DIP 20



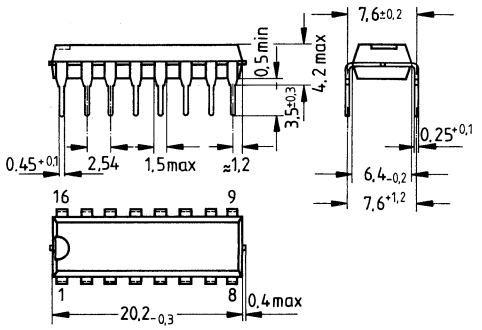
Dimensions in mm

Ordering Information

Type	Ordering code	Description
SAB 82289-P	Q67120-Y77	Bus Arbiter 16 MHz (plastic)
SAB 82289-6-P	Q67120-Y111	Bus Arbiter 12 MHz (plastic)

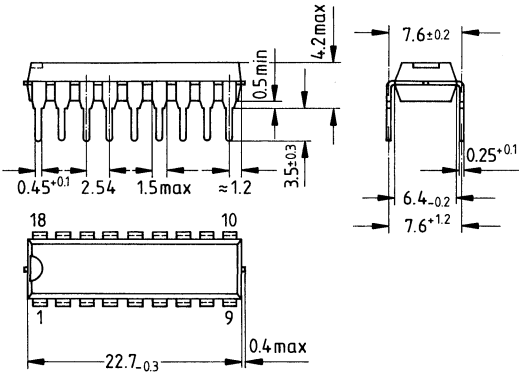
Summary of Package Outlines

Plastic Package, P-DIP-16
(dual-in-line package)
20A16 DIN 41870 T9



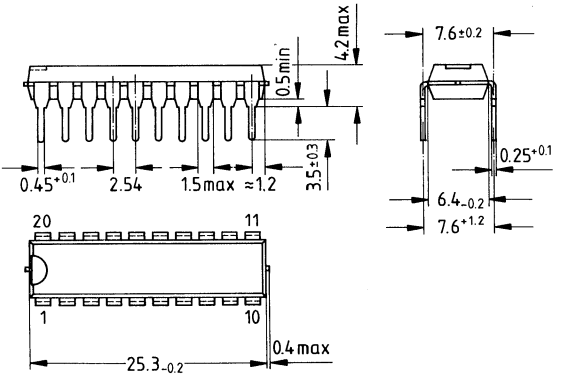
Dimensions in mm

Plastic Package, P-DIP-18
(dual-in-line package)
20A18 DIN 41870 T9



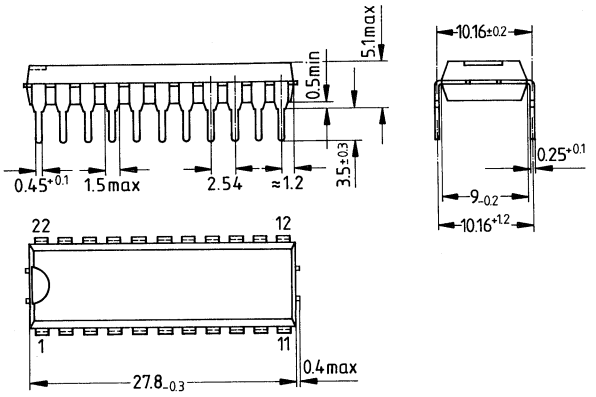
Dimensions in mm

Plastic Package, P-DIP-20
(dual-in-line package)
20A20 DIN 41870 T9



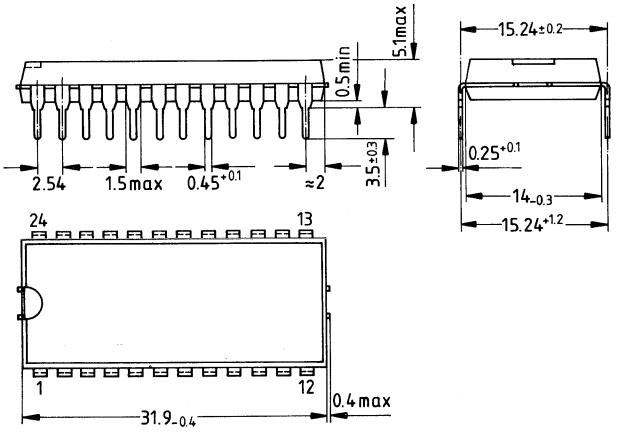
Dimensions in mm

Plastic Package, P-DIP-22
(dual-in-line package)
20D22 DIN 41870 T11



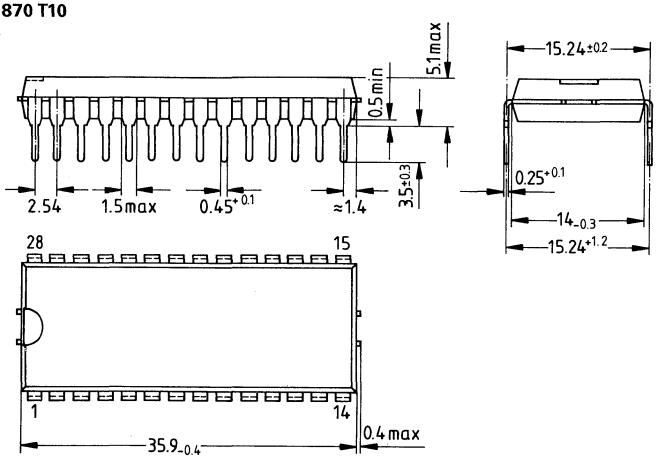
Dimensions in mm

Plastic Package, P-DIP-24
(dual-in-line package)
20B24 DIN 41870 T10



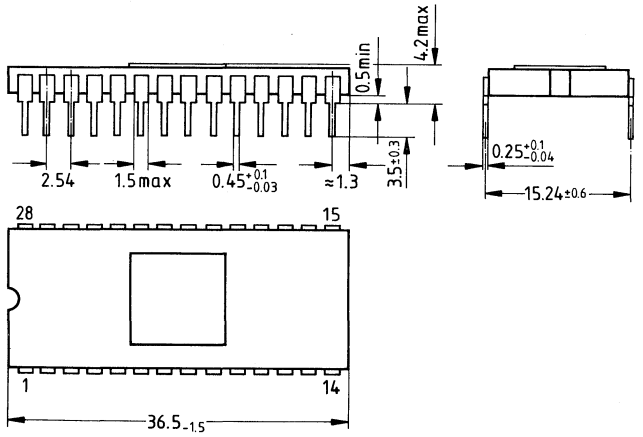
Dimensions in mm

Plastic Package, P-DIP-28
(dual-in-line package)
20B28 DIN 41870 T10



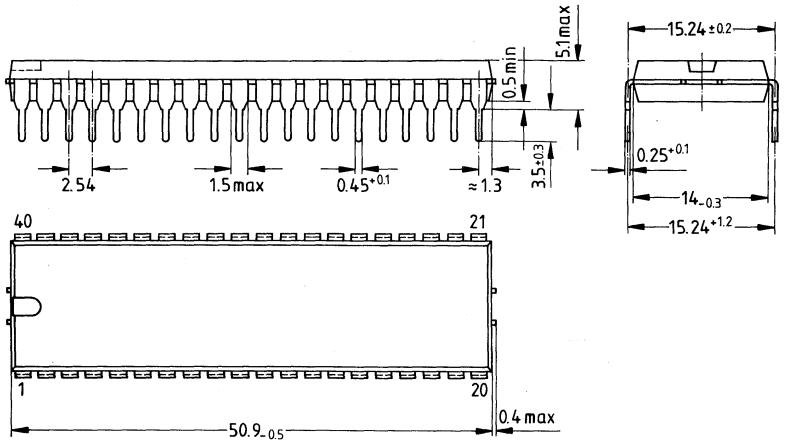
Dimensions in mm

Ceramic Package, C-DIP-28
(dual-in-line package)
20B28 DIN 41870 T10



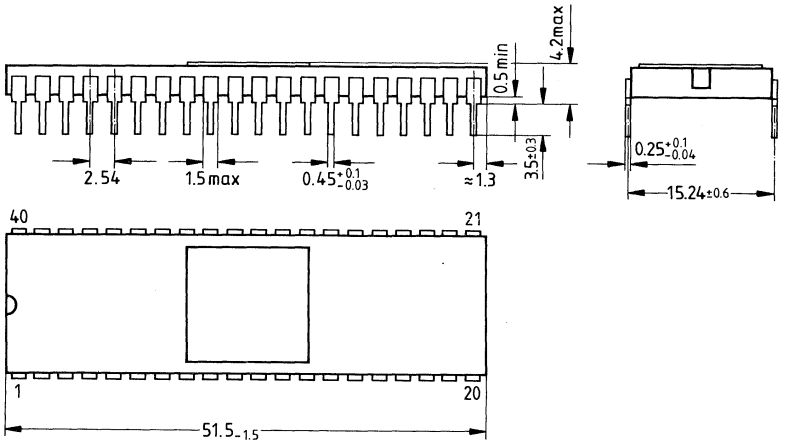
Dimensions in mm

Plastic Package, P-DIP-40
(dual-in-line package)
20B40 DIN 41870 T10



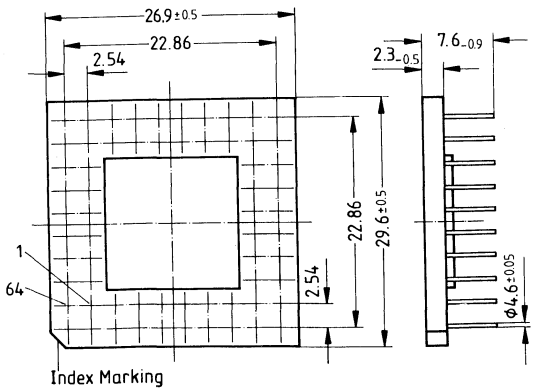
Dimensions in mm

Ceramic Package, C-DIP-40
(dual-in-line package)
20B40 DIN 41870 T10



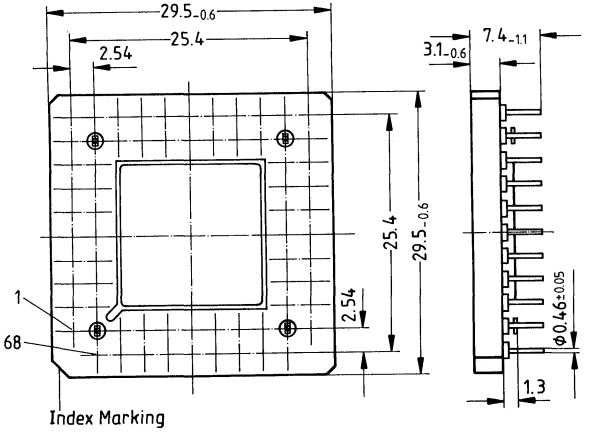
Dimensions in mm

Ceramic Package, C-PGA-64
(pin-grid-array)



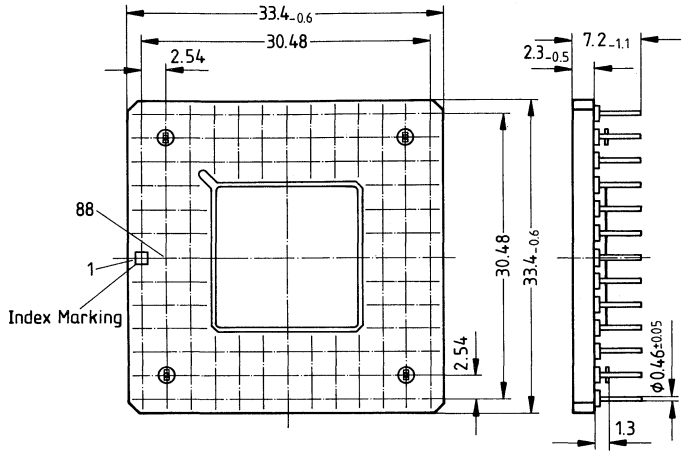
Dimensions in mm

Ceramic Package, C-PGA-68
(pin-grid-array)



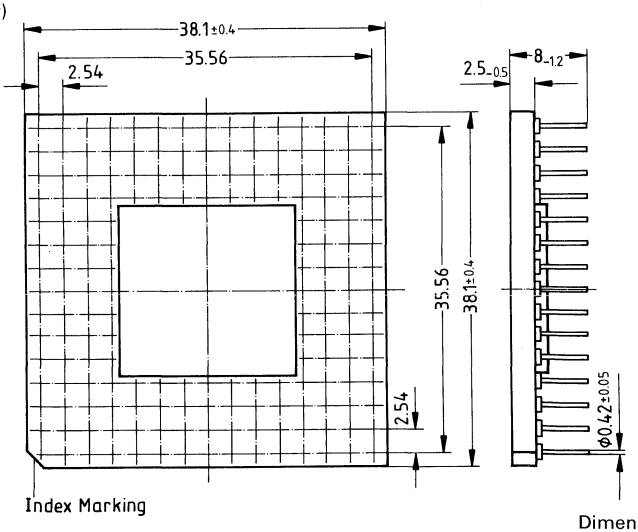
Dimensions in mm

Ceramic Package, C-PGA-88
(pin-grid-array)



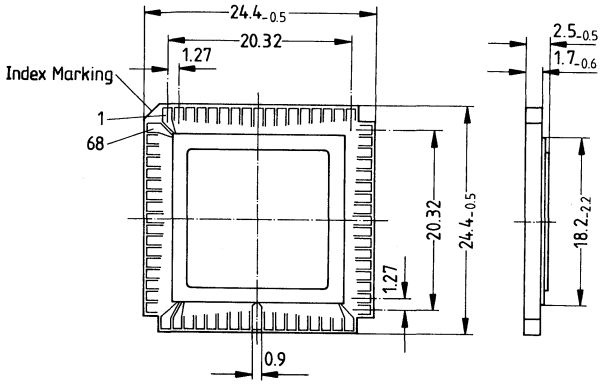
Dimensions in mm

Ceramic Package, C-PGA-145
(pin-grid-array)



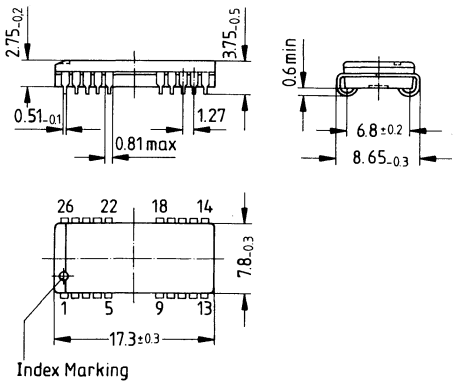
Dimensions in mm

Ceramic Package, C-CC-68
(chip-carrier)



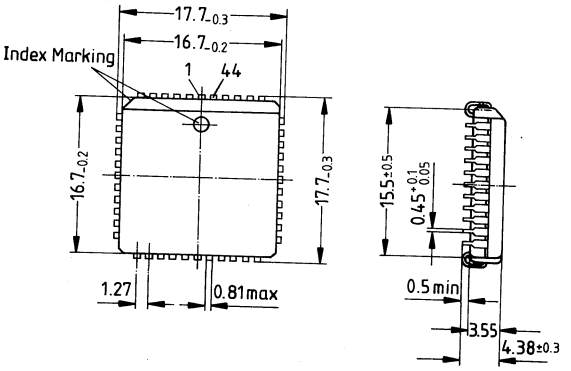
Dimensions in mm

Plastic Package, P-SOJ-26/20
(Plastic small outline J-lead) - **SMD**



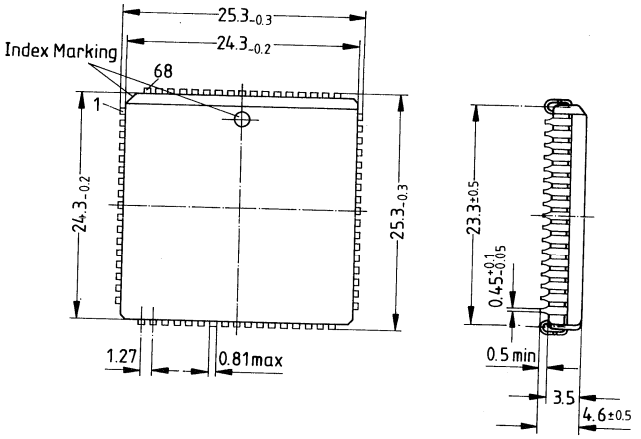
Dimensions in mm

Plastic Package, PL-CC-44
(plastic leaded - chip carrier) - **SMD**



Dimensions in mm

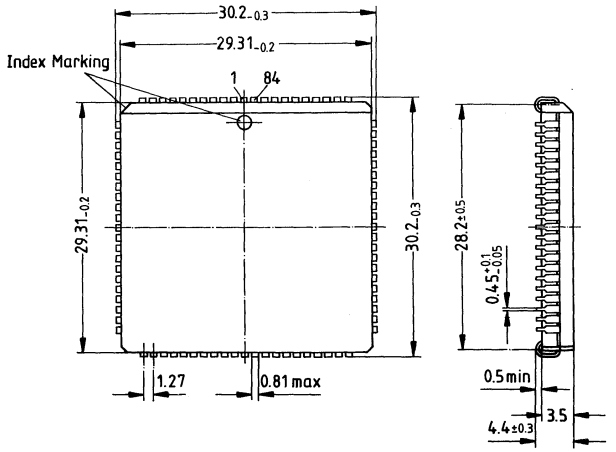
Plastic Package, PL-CC-68
(plastic leaded - chip carrier) - **SMD**



Dimensions in mm

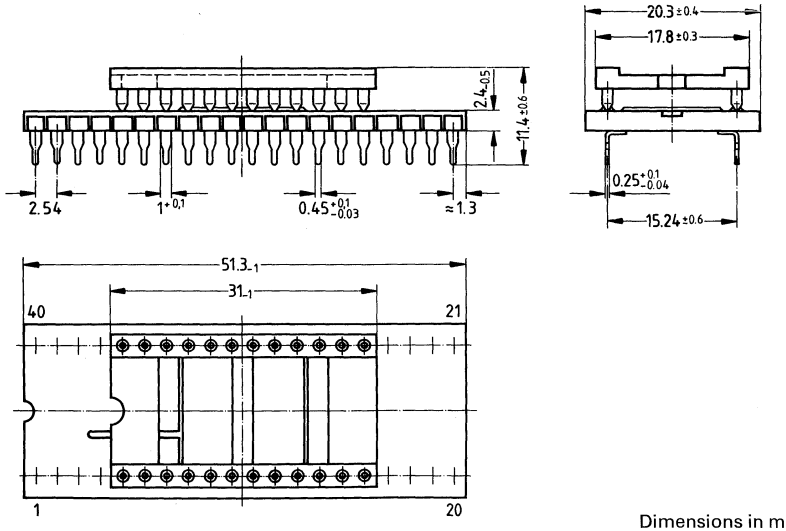
Package Outlines

Plastic Package, PL-CC-84
(plastic leaded - chip carrier) - **SMD**



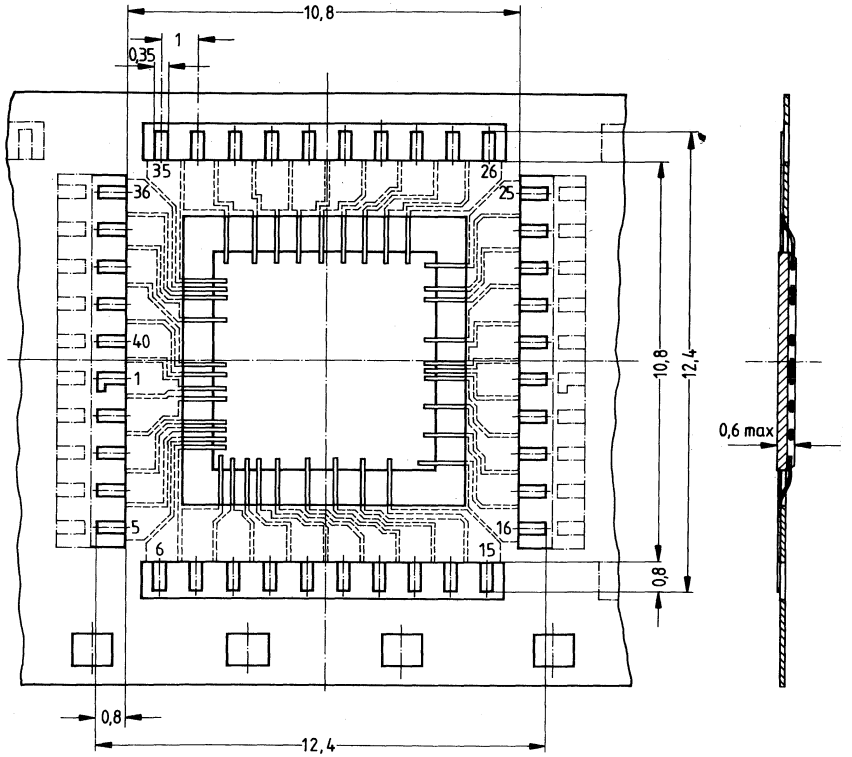
Dimensions in mm

Piggyback



Dimensions in mm

MIKROPACK
16 mm, 40 Pins - SMD



Dimensions in mm

Siemens Offices

Siemens AG, Bereich Bauelemente
Balanstraße 73, Postfach 80 17 09, **D-8000 München 80**
☎ (089) 41 44-0 Tx 52108-0 FAX (089) 41 44-26 89

Siemens Worldwide

Federal Republic of Germany and Berlin (West)

Siemens AG
Salzufer 6–8
1000 Berlin 10
☎ (030) 3939-1, Tx 1810-278
FAX (030) 3939-2630
Ttx 308190 = sieznb

Siemens AG
Lahnweg 10
Postfach 1115
4000 Düsseldorf 1
☎ (0211) 399-0, Tx 8581301
FAX (0211) 399-2506

Siemens AG
Rödelheimer Landstraße 5–9
Postfach 111733
6000 Frankfurt 1
☎ (069) 797-0, Tx 414131-0
FAX (069) 797-2253

Siemens AG
Lindenplatz 2
Postfach 105609
2000 Hamburg 1
☎ (040) 282-1, Tx 215584-0
FAX (040) 282-2210

Siemens AG
Am Maschpark 1
Postfach 5329
3000 Hannover 1
☎ (0511) 129-0, Tx 922333
FAX (0511) 129-2799

Siemens AG
Richard-Strauss-Straße 76
Postfach 202109
8000 München
☎ (089) 9221-4380
Tx 529421-19
FAX (089) 9221-4390
Ttx 8985061

Siemens AG
Von-der-Tann-Straße 30
Postfach 4844
8500 Nürnberg 1
☎ (0911) 654-0, Tx 622251
FAX (0911) 654-4064

Siemens AG
Geschwister-Scholl-Straße 24
Postfach 120
7000 Stuttgart 1
☎ (0711) 2076-0, Tx 723941
FAX (0711) 2076-3706

EUROPE

Austria
Siemens Aktiengesellschaft
Österreich
Postfach 326
A-1031 Wien
☎ (0222) 7293-0, Tx 1372-0

Belgium
Siemens S.A.
chaussée de Charleroi 116
B-1060 Bruxelles
☎ (02) 536-2111, Tx 21347

Denmark
Siemens A/S
Borupvang 3
DK-2750 Ballerup
☎ (02) 656565, Tx 35313

Finland
Siemens Osakeyhtiö
PL 8
SF-00101 Helsinki 10
☎ (0) 1626-1, Tx 124465

France
Siemens S.A.
B.P. 109
F-93203 Saint-Denis CEDEX 1
☎ (1) 49223100, Tx 620853

Great Britain
Siemens Ltd.
Siemens House
Windmill Road
GB-Sunbury-on-Thames
Middlesex TW 16 7HS
☎ (09327) 85691, Tx 8951091

Greece
Siemens AE
Paradissou & Artemidos
P.O.B. 61011
GR-15110 Amaroussin
☎ (01) 6864 111

Ireland
Siemens Ltd.
Unit 8–11 Slaney Road
Dublin Industrial Estate
Finglas Road
Dublin 11
☎ (01) 302855, Tx 32547

Italy
Siemens Elettra S.p.A.
Via Fabio Filzi, 29
Casella Postale 10388
I-20100 Milano
☎ (02) 67661, Tx 330261

Netherlands
Siemens Nederland N.V.
Postb. 16068
NL-2500 BB Den Haag
☎ (070) 782782, Tx 31373

Norway
Siemens A/S
Østre Aker vei 90
Postboks 10, Veitvet
N-0518 Oslo 5
☎ (02) 153090, Tx 78477

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